3.3-V CAN TRANSCEIVER

FEATURES

- **Bus-Pin Fault Protection Exceeds ±36 V**
- **Bus-Pin ESD Protection Exceeds 16-kV Human Body Model (HBM)**
- **Compatible With ISO 11898**
- **Signaling Rates(1) up to 1 Mbps**
- **Extended –7-V to 12-V Common-Mode Range**
- **High-Input Impedance Allows for 120 Nodes**
- **LVTTL I/Os Are 5-V Tolerant**
- **Adjustable Driver Transition Times for Improved Signal Quality**
- **Unpowered Node Does Not Disturb the Bus**
- **Low-Current Standby Mode . . . 200 μA Typical**
- **Power-Up/Down Glitch-Free Bus Inputs and Outputs**
  - **High Input Impedance With Low V_{CC}**
  - **Monolithic Output During Power Cycling**
- **Loopback for Diagnostic Functions Available**
- **DeviceNet™ Vendor ID #806**

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

APPLICATIONS

- **Down-Hole Drilling**
- **High Temperature Environments**
- **Industrial Automation**
  - **DeviceNet™ Data Buses**
  - **Smart Distributed Systems (SDS™)**
- **SAE J1939 Data Bus Interface**
- **NMEA 2000 Data Bus Interface**
- **ISO 11783 Data Bus Interface**
- **CAN Data Bus Interface**

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Extreme (–55°C/210°C) Temperature Range(1)**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**
- **Texas Instruments high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.**

DESCRIPTION/ORDERING INFORMATION

The SN65HVD233 is used in applications employing the controller area network (CAN) serial communication physical layer in accordance with the ISO 11898 standard, with the exception that the thermal shutdown is removed. As a CAN transceiver, the device provides transmit and receive capability between the differential CAN bus and a CAN controller, with signaling rates up to 1 Mbps.

Designed for operation in especially harsh environments, the device features cross wire, overvoltage, and loss-of-ground protection to ±36 V, with common-mode transient protection of ±100 V. This device operates over a –7-V to 12-V common-mode range with a maximum of 60 nodes on a bus.

If the common-mode range is restricted to the ISO 11898 standard range of –2 V to 7 V, up to 120 nodes may be connected on a bus. This transceiver interfaces the single-ended CAN controller with the differential CAN bus found in industrial, building automation, and automotive applications.

(1) Custom temperature ranges available

PRODUCT PREVIEW

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

R_S (pin 8) provides for three modes of operation: high-speed, slope control, or low-power standby mode. The high-speed mode of operation is selected by connecting R_S directly to ground, allowing the driver output transistors to switch on and off as fast as possible with no limitation on the rise and fall slope. The rise and fall slope can be adjusted by connecting a resistor to ground at R_S, since the slope is proportional to the pin's output current. Slope control is implemented with a resistor value of 10 kΩ to achieve a slew rate of ≈ 15 V/µs, and a value of 100 kΩ to achieve ≈ 2.0 V/µs slew rate. For more information about slope control, refer to the application information section.

The SN65HVD233 enters a low-current standby mode, during which the driver is switched off and the receiver remains active if a high logic level is applied to R_S. The local protocol controller reverses this low-current standby mode when it needs to transmit to the bus.

A logic high on the loopback (LBK, pin 5) of the SN65HVD233 places the bus output and bus input in a high-impedance state. The remaining circuit remains active and available for the driver to receiver loopback, self-diagnostic node functions without disturbing the bus.

PRODUCT PREVIEW

AVAILABLE OPTIONS

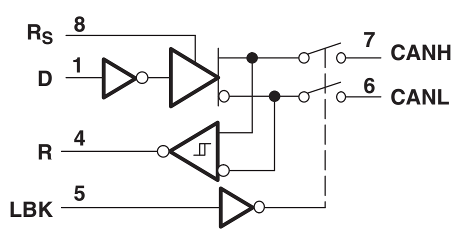
PART NUMBER	LOW-POWER MODE	SLOPE CONTROL	DIAGNOSTIC LOOPBACK	AUTOBAUD LOOPBACK
SN65HVD233SJD	200-µA standby mode	Adjustable	Yes	No
SN65HVD233SKGDA	200-µA standby mode	Adjustable	Yes	No

ORDERING INFORMATION(1)

PACKAGE (JD)(2)	TOP-SIDE MARKING
SN65HVD233SJD	SN65HVD233SJD
PACKAGE (BARE DIE) (2)	
SN65HVD233SKGDA	

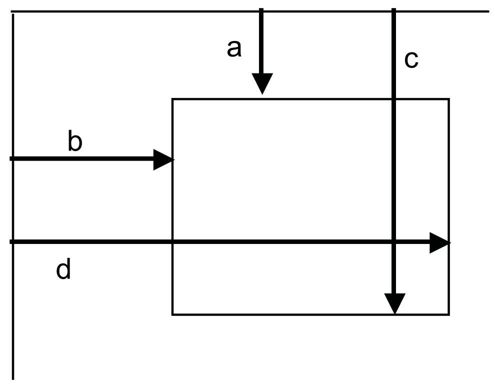
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTIONAL BLOCK DIAGRAM



BARE DIE INFORMATION

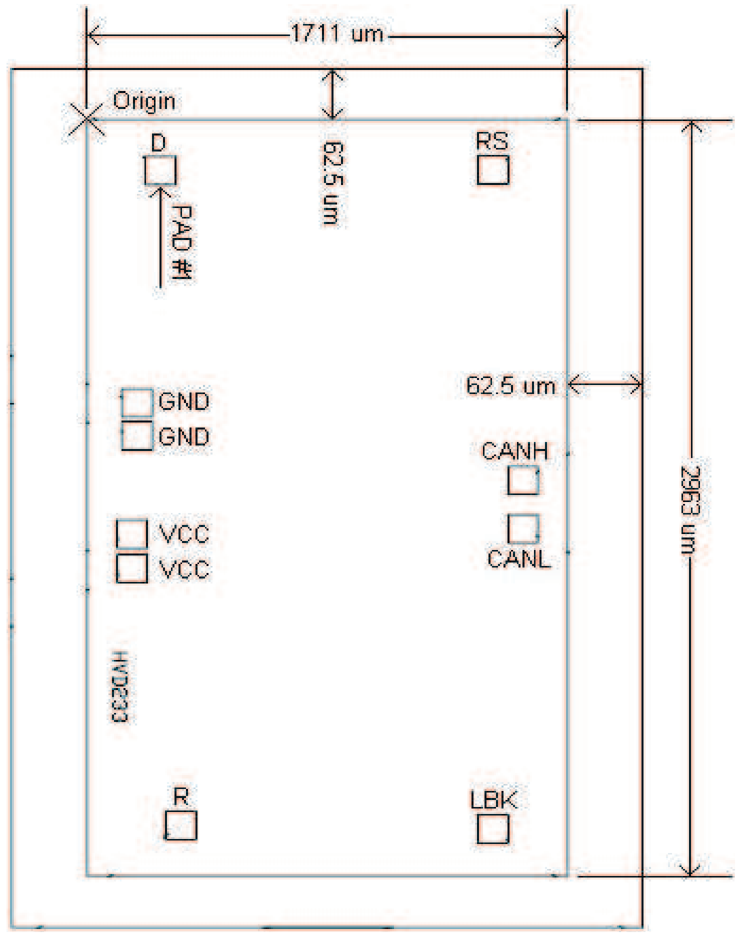
DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION
15 mm	Silicon with backgrind	GND	Al-Si-Cu (0.5%)



Bond Pad Coordinates in Microns - Rev A

DISCRIPTION	PAD NUMBER	a	b	c	d
D	1	86.40	157.85	203.40	274.85
GND	2	1035.05	69.75	1150.05	184.75
GND	3	1168.15	69.75	1283.15	184.75
VCC	4	1572.05	51.85	1687.05	166.85
VCC	5	1711.95	51.85	1826.95	166.85
R	6	2758.85	237.65	2873.85	352.65
LBK	7	2774.25	1429.985	2889.25	1544.95
CANL	8	1549.90	1544.95	1664.90	1659.95
CANH	9	1351.45	1544.95	1466.45	1659.95
RS	10	83.50	1429.95	198.50	1544.95

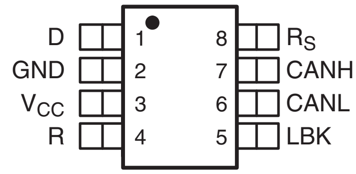
PRODUCT PREVIEW



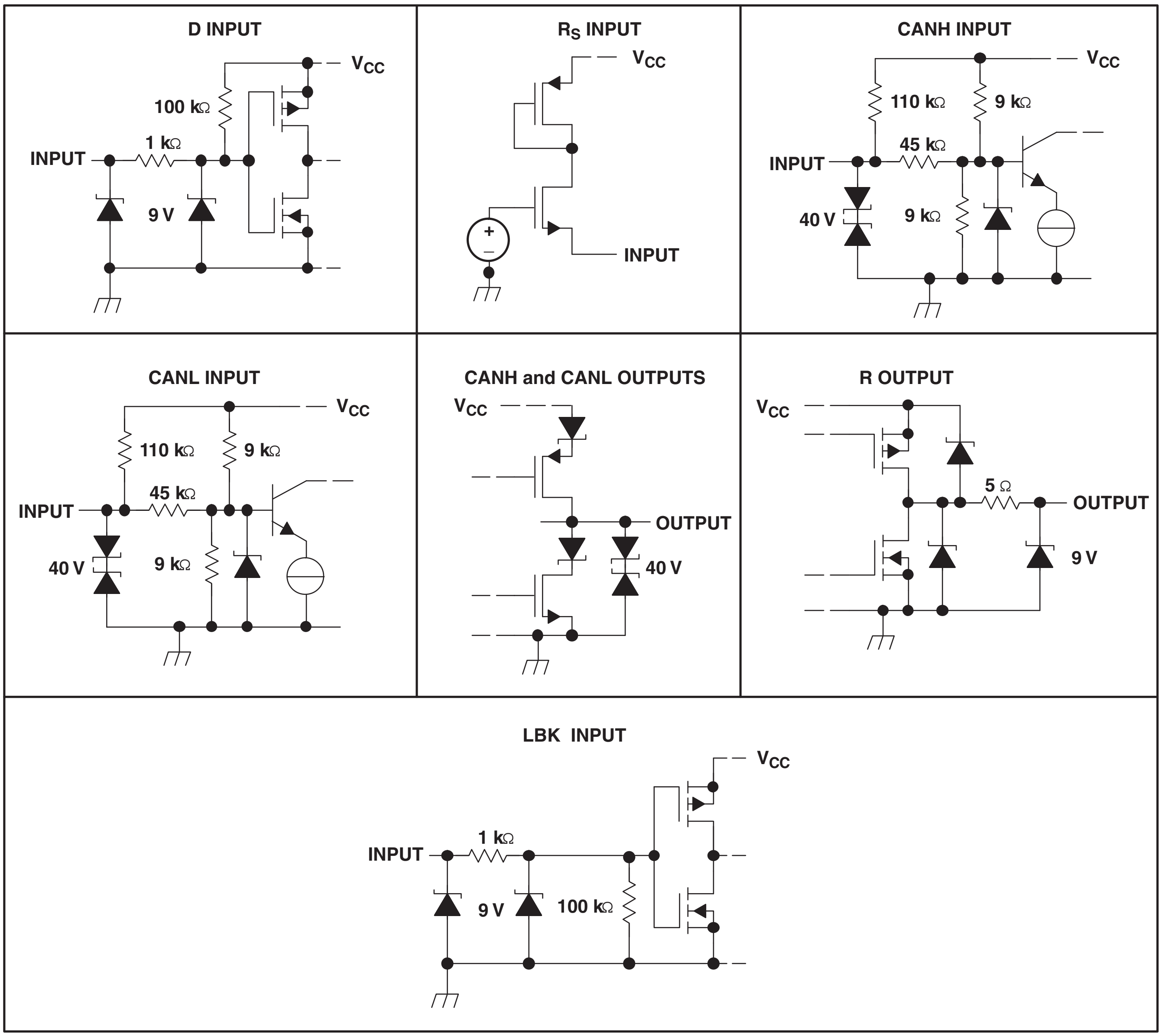
PRODUCT PREVIEW

DEVICE INFORMATION

JD PACKAGE
(TOP VIEW)



EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



PRODUCT PREVIEW

FUNCTION TABLES(1)

(1) H = high level, L = low level, Z = high impedance, X = irrelevant, ? = indeterminate

DRIVER					
INPUTS			OUTPUTS		
D	LBK	R_S	CANH	CANL	BUS STATE
X	X	>0.75 V_{CC}	Z	Z	Recessive
L	L or open	≤0.33 V_{CC}	H	L	Dominant
H or open	X		Z	Z	Recessive
X	H	≤0.33 V_{CC}	Z	Z	Recessive

RECEIVER				
INPUTS				OUTPUT
BUS STATE	$V_{ID} = V_{(CANH)} - V_{(CANL)}$	LBK	D	R
Dominant	$V_{ID} \geq 0.9$ V	L or open	X	L
Recessive	$V_{ID} \leq 0.5$ V or open	L or open	H or open	H
?	0.5 V < V_{ID} < 0.9 V	L or open	H or open	?
X	X	H	L	L
X	X		H	H

PRODUCT PREVIEW

ABSOLUTE MAXIMUM RATINGS[1] [2]

over operating free-air temperature range (unless otherwise noted)

				VALUE	UNIT
V_{CC}	Supply voltage range			–0.3 to 7	V
	Voltage range at any bus terminal (CANH or CANL)			–36 to 36	V
	Voltage input range, transient pulse (CANH and CANL) through 100 Ω (see Figure 8)			–100 to 100	V
V_I	Input voltage range (D, R, R_S, LBK)			–0.5 to 7	V
I_O	Receiver output current			–10 to 10	mA
	Electrostatic discharge	Human-Body Model (HBM)[3]	CANH, CANL, and GND	16	kV
			All pins	3	
		Charged-Device Mode (CDM)[4]	All pins	1	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

			T_A = –55°C to 210°C		UNIT
			MIN	MAX	
V_{CC}	Supply voltage		3	3.6	V
	Voltage at any bus terminal (separately or common mode)		–7	12	V
V_{IH}	High-level input voltage	D, LBK	2	5.5	V
V_{IL}	Low-level input voltage	D, LBK	0	0.8	V
V_{ID}	Differential input voltage		–6	6	V
	Resistance from R_S to ground		0	100	kΩ
$V_{I(Rs)}$	Input voltage at R_S for standby		0.75 V_{CC}	5.5	V
I_{OH}	High-level output current	Driver	–50		mA
		Receiver	–10		
I_{OL}	Low-level output current	Driver		50	mA
		Receiver		10	
T_J	Operating junction temperature			212	°C
T_A	Operating free-air temperature[1]		-55	210	°C

(1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

PRODUCT PREVIEW

DRIVER ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 210°C(1)			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{O(D)}$	Bus output voltage (dominant)	CANH	D = 0 V, R_S = 0 V, See Figure 2 and Figure 3	2.45		V_{CC}	2.45		V_{CC}	V
		CANL		0.5		1.25	0.5		1.25	
V_O	Bus output voltage (recessive)	CANH	D = 3 V, R_S = 0 V, See Figure 2 and Figure 3		2.3			2.3		V
		CANL			2.3			2.3		
$V_{OD(D)}$	Differential output voltage (Dominant)		D = 0 V, R_S = 0 V, See Figure 2 and Figure 3	1.5	2	3	1.4	1.75	3	V
			D = 0 V, R_S = 0 V, See Figure 3 and Figure 4	1.1	2	3	1.1	1.47	3	
V_{OD}	Differential output voltage (Recessive)		D = 3 V, R_S = 0 V, See Figure 2 and Figure 3	–120		12	–120		12	mV
			D = 3 V, R_S = 0 V, No load	–0.5		0.05	–0.5		1.2	V
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage		See Figure 10		1			1		V
I_{IH}	High-level input current	D, LBK	D = 2 V	–30		30	–30		30	µA
I_{IL}	Low-level input current	D, LBK	D = 0.8 V	–30		30	–30		30	µA
I_{OS}	Short-circuit output current		V_{CANH} = –7 V, CANL open, See Figure 13	–250			–250			mA
			V_{CANH} = 12 V, CANL open, See Figure 13			1			1	
			V_{CANL} = –7 V, CANH open, See Figure 13	–1			–1			
			V_{CANL} = 12 V, CANH open, See Figure 13			250			250	
C_O	Output capacitance		See receiver input capacitance							
$I_{IRs(s)}$	R_S input current for standby		R_S = 0.75 V_{CC}	–10			–10			µA
I_{CC}	Supply current	Standby	R_S = V_{CC}, D = V_{CC}, LBK = 0 V		200	600		400	600	µA
		Dominant	D = 0 V, No load, LBK = 0 V, R_S = 0 V			6			6	mA
		Recessive	D =t V_{CC}, No load, LBK = 0 V, R_S = 0 V			6			6	

(1) Minimum and maximum parameters are characterized for operation at T_A = 210°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.

PRODUCT PREVIEW

DRIVER SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 210°C (1)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	R_S = 0 V, See Figure 5		35	85		50		ns
		R_S with 10 kΩ to ground, See Figure 5		70	125		75		
		R_S with 100 kΩ to ground, See Figure 5		500	870		500		
t_{PHL}	Propagation delay time, high-to-low-level output	R_S = 0 V, See Figure 5		70	120		70		ns
		R_S with 10 kΩ to ground, See Figure 5		130	180		130		
		R_S with 100 kΩ to ground, See Figure 5		870	1200		870		
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)	R_S = 0 V, See Figure 5		35			9		ns
		R_S with 10 kΩ to ground, See Figure 5		60			35		
		R_S with 100 kΩ to ground, See Figure 5		370			475		
t_r	Differential output signal rise time	R_S = 0 V, See Figure 5	20		70	20		75	ns
t_f	Differential output signal fall time		18		70	20		75	
t_r	Differential output signal rise time	R_S with 10 kΩ to ground, See Figure 5	30		135	30		140	ns
t_f	Differential output signal fall time		30		135	30		140	
t_r	Differential output signal rise time	R_S with 100 kΩ to ground, See Figure 5	250		1400	250		1400	ns
t_f	Differential output signal fall time		350		1400	350		1400	
$t_{en(s)}$	Enable time from standby to dominant	See Figure 9		0.6	1.5		0.6	1.5	µs

(1) Minimum and maximum parameters are characterized for operation at T_A = 210°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.

Table 1. THERMAL CHARACTERISTICS

PARAMETERS		TEST CONDITIONS	MAX	UNIT
θ_{JA}	Junction-to-ambient thermal resistance (1)	Low-K (2) board, no air flow	83.4	°C/W
		High-K (3) board, no air flow	64.9	
θ_{JB}	Junction-to-board thermal resistance	High-K (3) board, no air flow	27.9	°C/W
θ_{JC}	Junction-to-case thermal resistance		6.49	°C/W
$P_{(AVG)}$	Average power dissipation	R_L = 60 Ω, R_S = 0 V, input to D a 1-MHz 50% duty cycle square wave, V_{CC} = 3.3 V, T_A = 25°C	114	mW

(1) See TI literature number SZZA003 for an explanation of this parameter.
(2) JESD51-3 low effective thermal conductivity test board for leaded surface-mount packages.
(3) JESD51-7 high effective thermal conductivity test board for leaded surface-mount packages.

PRODUCT PREVIEW

RECEIVER ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A = –55°C to 125°C MIN	TYP	MAX	T_A = 210°C(1) MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	LBK = 0 V, See Table 2			620	900		600	900	mV
V_{IT-}	Negative-going input threshold voltage	LBK = 0 V, See Table 2		500	715		500	725		mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	LBK = 0 V, See Table 2			100			140		mV
V_{OH}	High-level output voltage	I_O = –4 mA, See Figure 7		2.4			2.4			V
V_{OL}	Low-level output voltage	I_O = 4 mA, See Figure 7				0.4			0.4	V
I_I	Bus input current	CANH or CANL = 12 V	Other bus pin = 0 V, D = 3 V, LBK = 0 V, R_S = 0 V,	140		500	140		500	µA
		CANH or CANL = 12 V, V_{CC} = 0 V		200		600	200		800	
		CANH or CANL = –7 V		–610		–150	–610		–150	
		CANH or CANL = –7 V, V_{CC} = 0 V		–450		–130	–450		–130	
C_I	Input capacitance (CANH or CANL)	Pin to ground, $V_I = 0.4 \sin(4E6\pi t) + 0.5$ V, D = 3 V, LBK = 0 V			45			55		pF
C_{ID}	Differential input capacitance	Pin to pin, $V_I = 0.4 \sin(4E6\pi t) + 0.5$ V, D = 3 V, LBK = 0 V			15			15		pF
R_{ID}	Differential input resistance	D = 3 V, LBK = 0 V		40		110	40		110	kΩ
R_{IN}	Input resistance (CANH or CANL)	D = 3 V, LBK = 0 V		20		51	18		51	kΩ
I_{CC} Supply current	Standby	$R_S = V_{CC}$, $D = V_{CC}$, LBK = 0 V			200	600		400	600	µA
	Dominant	D = 0 V, No load, R_S = 0 V, LBK = 0 V				6			6	mA
	Recessive	$D = V_{CC}$, No load, R_S = 0 V, LBK = 0 V				6			6	mA

(1) Minimum and maximum parameters are characterized for operation at T_A = 210°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.

PRODUCT PREVIEW

RECEIVER SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 210°C(1)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 7		35	60		50	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output			35	60		45	60	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)			7			5		ns
t_r	Output signal rise time			2	6.5		6.5	8	ns
t_f	Output signal fall time			2	6.5		6.5	9	ns

(1) Minimum and maximum parameters are characterized for operation at T_A = 210°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.

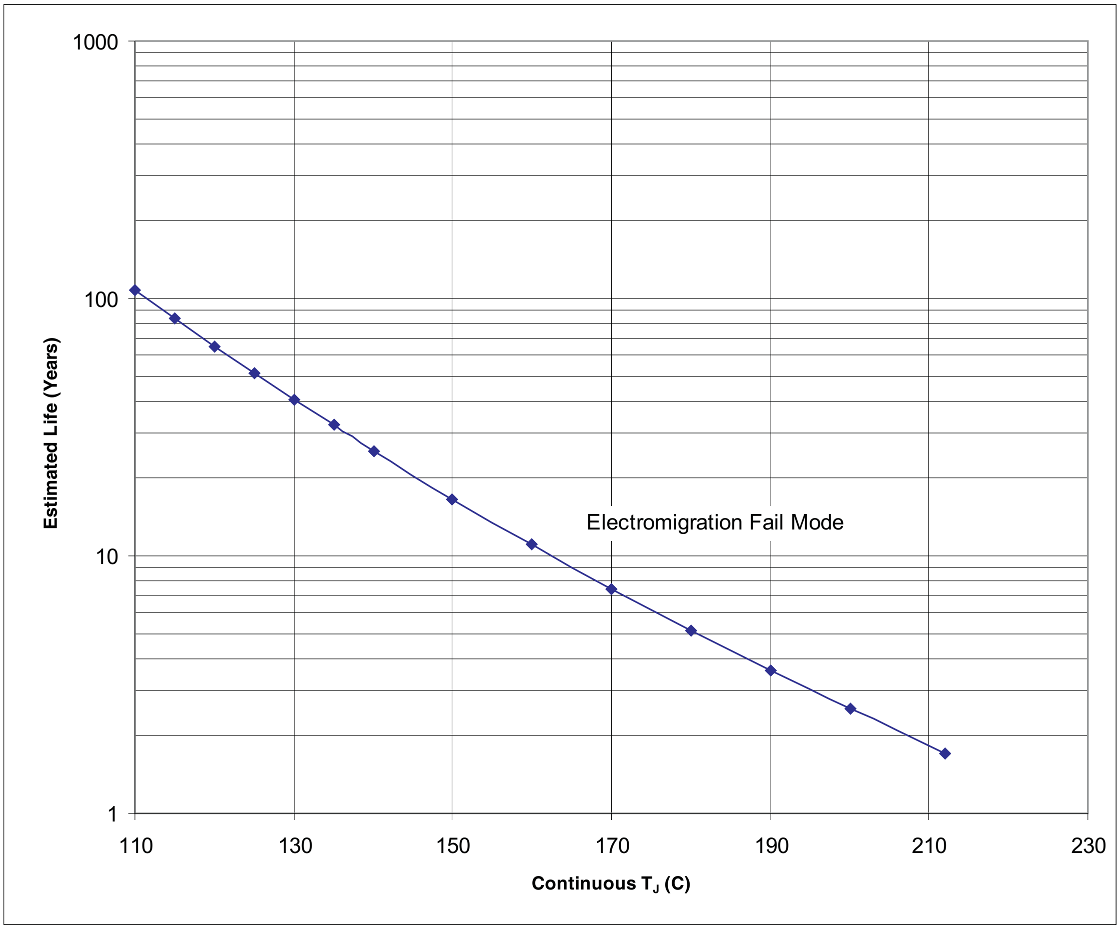
DEVICE SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 210°C(1)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_{(LBK)}$	Loopback delay, driver input to receiver output	See Figure 12		7.5	15		12	15	ns
$t_{(loop1)}$	Total loop delay, driver input to receiver output, recessive to dominant	R_S = 0 V, See Figure 11		70	135		90	135	ns
		R_S with 10 kΩ to ground, See Figure 11		105	190		115	190	
		R_S with 100 kΩ to ground, See Figure 11		535	1000		430	1000	
$t_{(loop2)}$	Total loop delay, driver input to receiver output, dominant to recessive	R_S = 0 V, See Figure 11		70	135		98	135	ns
		R_S with 10 kΩ to ground, See Figure 11		105	190		150	190	
		R_S with 100 kΩ to ground, See Figure 11		535	1100		880	1200	

(1) Minimum and maximum parameters are characterized for operation at T_A = 210°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.

PRODUCT PREVIEW



A. See data sheet for absolute maximum and minimum recommended operating conditions.

B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

Figure 1. SN65HVD233SJD / SN65HVD233SKGDA Operating Life Derating Chart

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

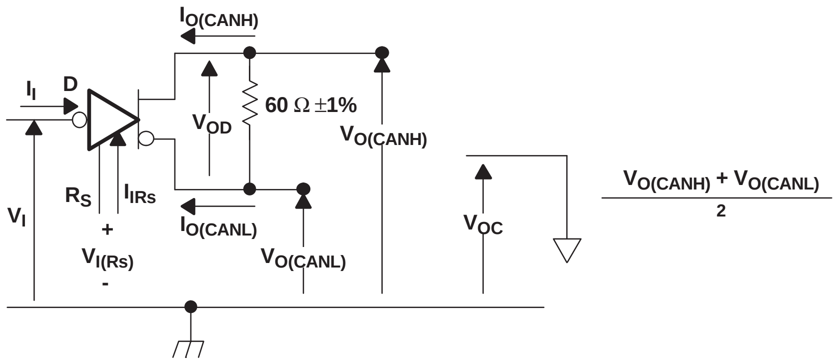


Figure 2. Driver Voltage, Current, and Test Definition

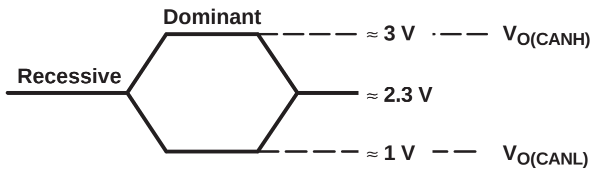


Figure 3. Bus Logic State Voltage Definitions

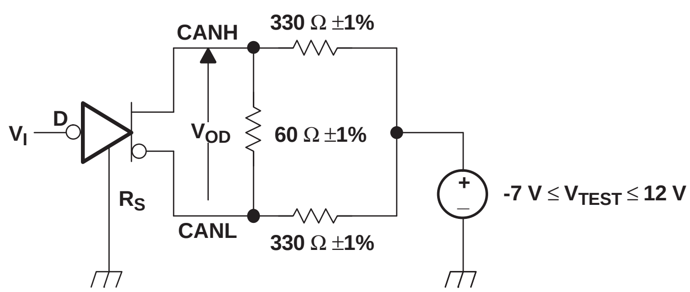
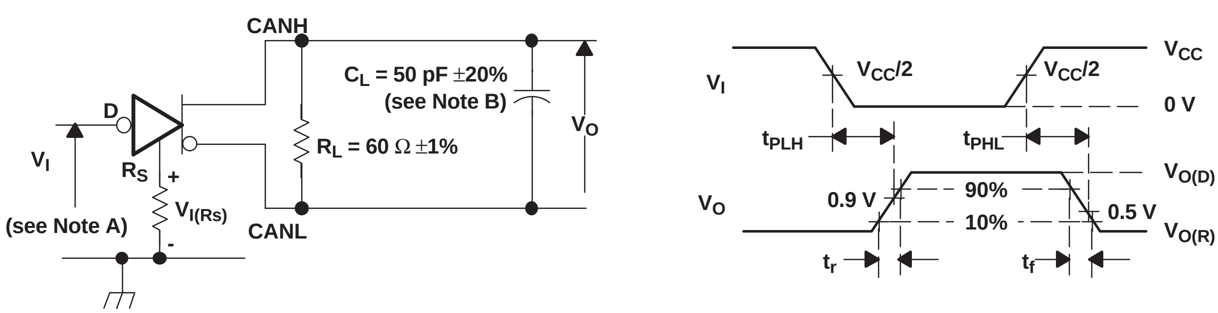


Figure 4. Driver V_{OD}



A. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes fixture and instrumentation capacitance.

Figure 5. Driver Test Circuit and Voltage Waveforms

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION (continued)

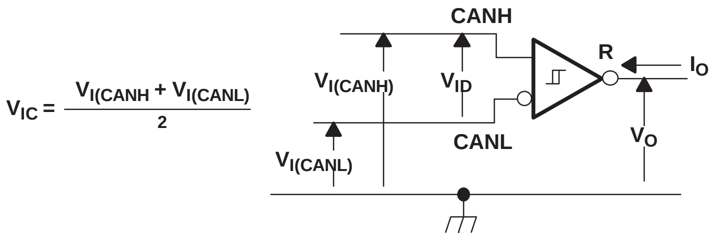
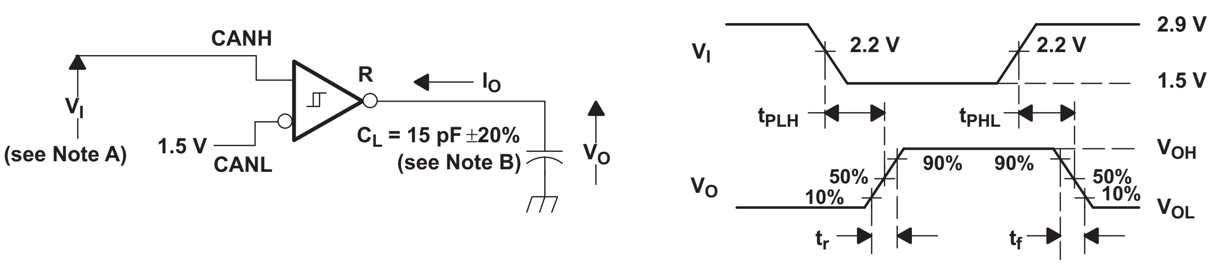


Figure 6. Receiver Voltage and Current Definitions



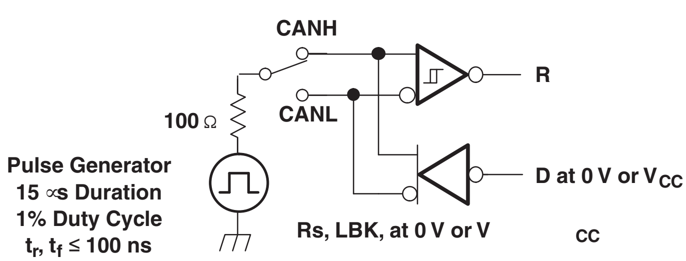
A. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50\ \Omega$.

B. C_L includes fixture and instrumentation capacitance.

Figure 7. Receiver Test Circuit and Voltage Waveforms

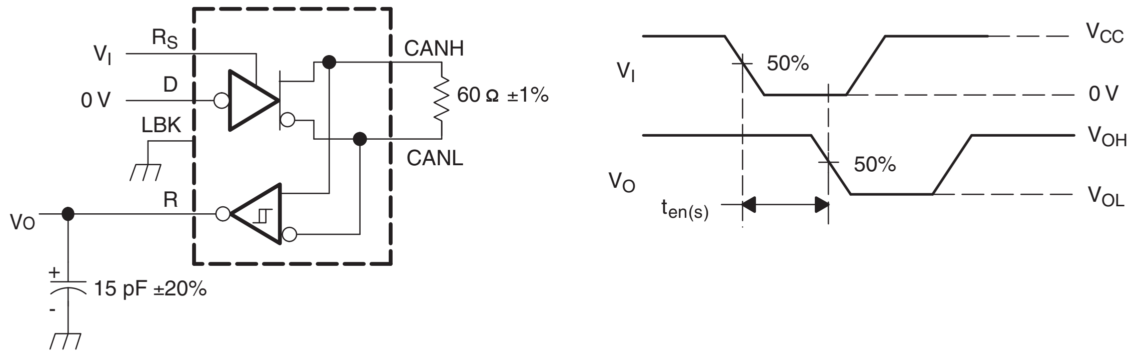
Table 2. Differential Input Voltage Threshold Test

INPUT		OUTPUT		MEASURED
V_{CANH}	V_{CANL}	R		$\lvert V_{ID}\rvert$
–6.1 V	–7 V	L	V_{OL}	900 mV
12 V	11.1 V	L		900 mV
–1 V	–7 V	L		6 V
12 V	6 V	L		6 V
–6.5 V	–7 V	H	V_{OH}	500 mV
12 V	11.5 V	H		500 mV
–7 V	–1 V	H		6 V
6 V	12 V	H		6 V
Open	Open	H		X



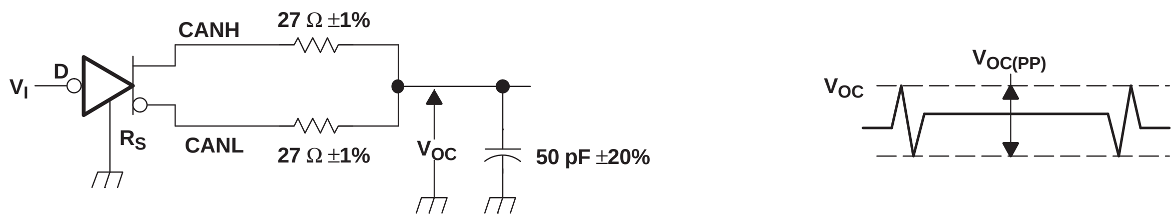
NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 8. Test Circuit, Transient Over Voltage Test



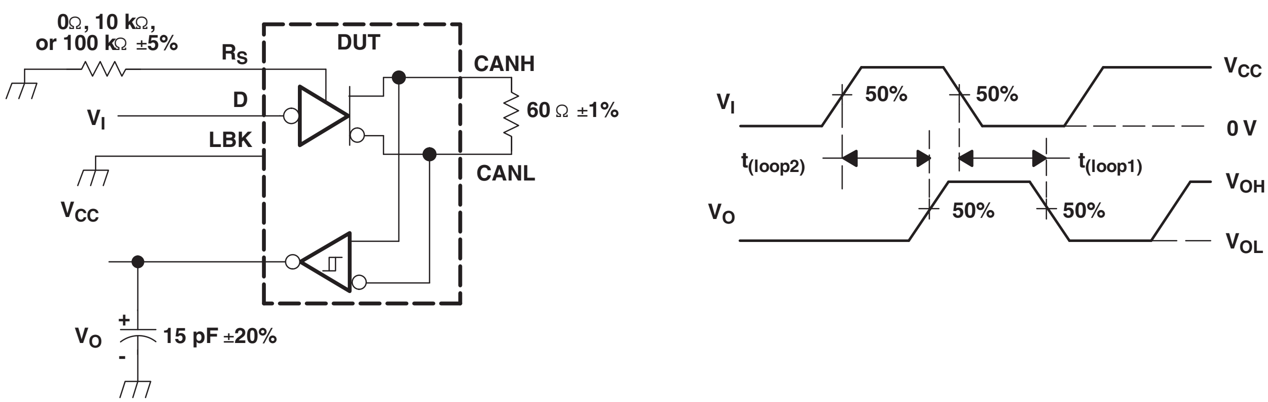
NOTE: All VI input pulses are supplied by a generator having the following characteristics:
t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 9. $t_{en(s)}$ Test Circuit and Voltage Waveforms



NOTE: All V_I input pulses are supplied by a generator having the following characteristics:
t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

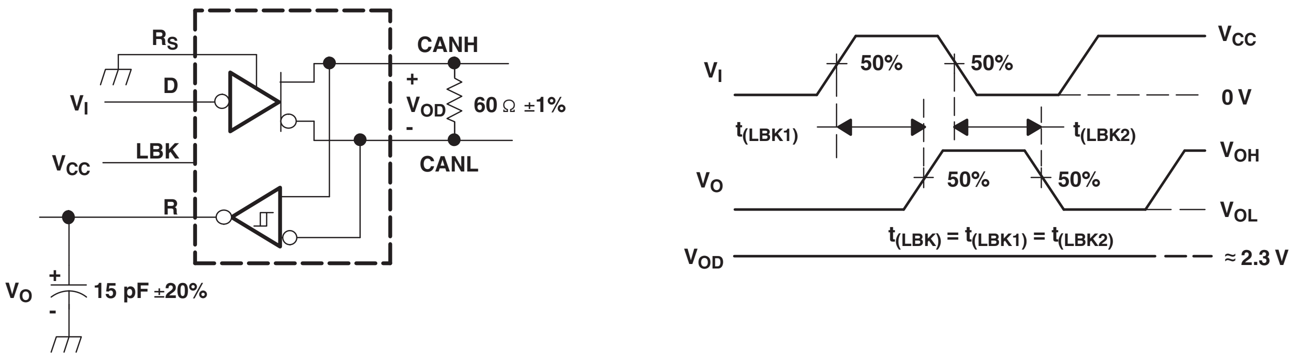
Figure 10. $V_{OC(pp)}$ Test Circuit and Voltage Waveforms



NOTE: All V_I input pulses are supplied by a generator having the following characteristics:
t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 11. $t_{(loop)}$ Test Circuit and Voltage Waveforms

PRODUCT PREVIEW



NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 12. $t_{(LBK)}$ Test Circuit and Voltage Waveforms

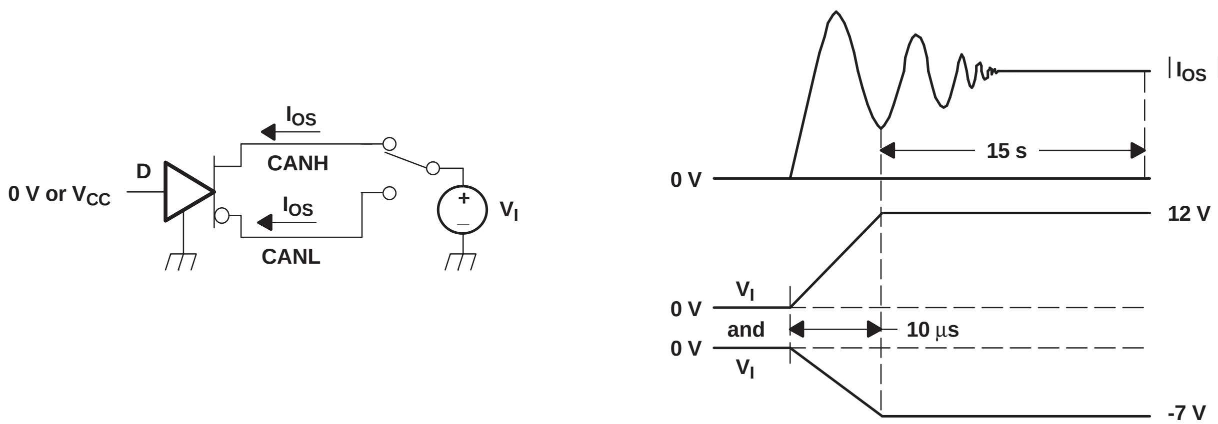
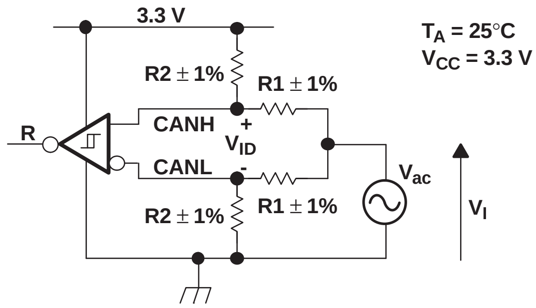
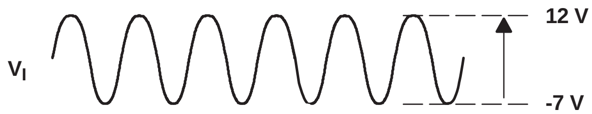


Figure 13. I_{OS} Test Circuit and Waveforms



The R Output State Does Not Change During Application of the Input Waveform.

V_{ID}	R1	R2
500 mV	50 Ω	280 Ω
900 mV	50 Ω	130 Ω



NOTE: All input pulses are supplied by a generator with f ≤ 1.5 MHz.

Figure 14. Common-Mode Voltage Rejection

PRODUCT PREVIEW

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

RECESSIVE-TO-DOMINANT LOOP TIME vs FREE-AIR TEMPERATURE

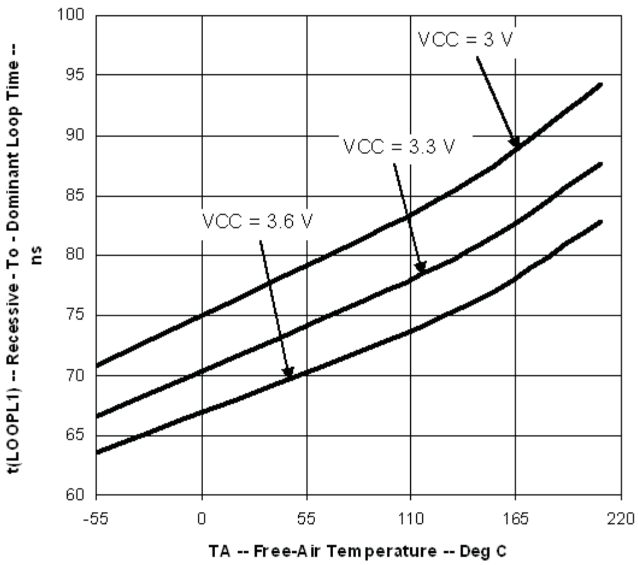


Figure 15.

DOMINANT-TO-RECESSIVE LOOP TIME vs FREE-AIR TEMPERATURE

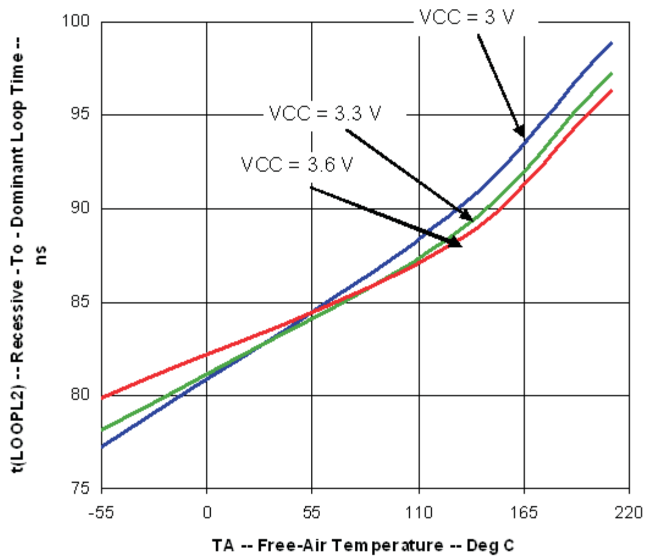


Figure 16.

SUPPLY CURRENT vs FREQUENCY

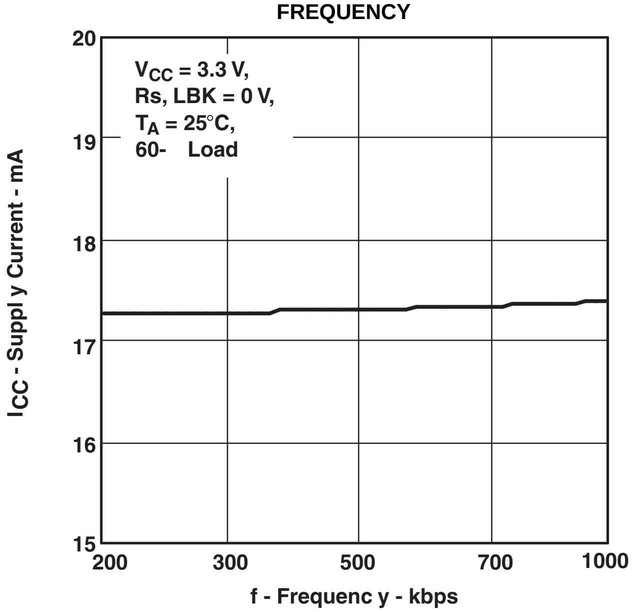


Figure 17.

DRIVER LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

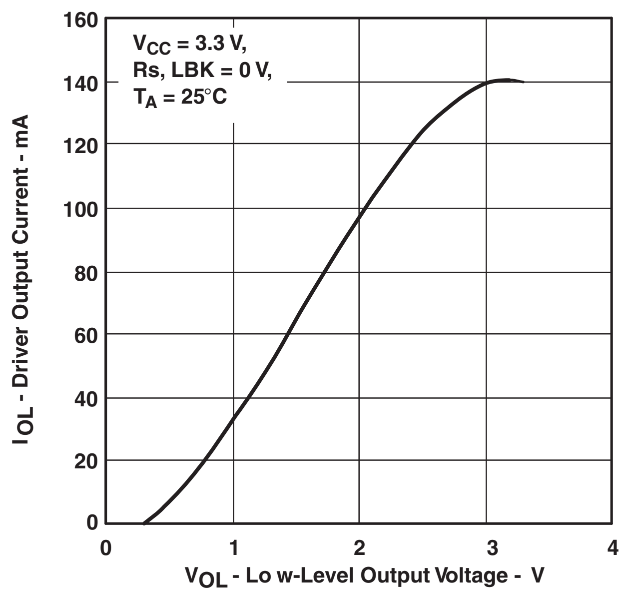


Figure 18.

TYPICAL CHARACTERISTICS (continued)

DRIVER HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

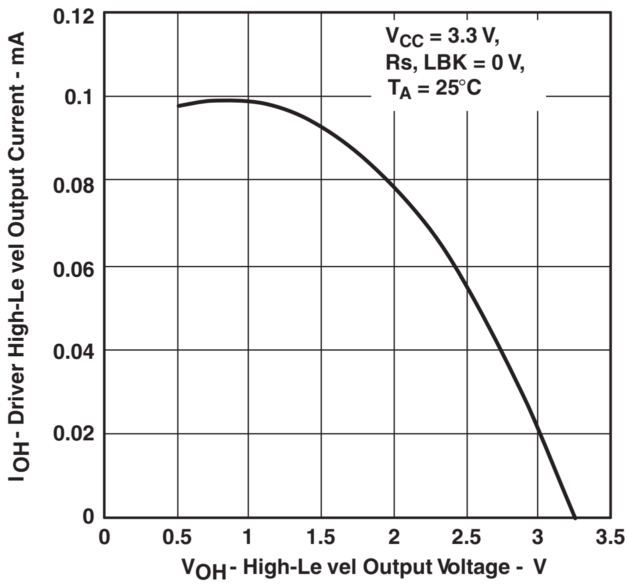


Figure 19.

DIFFERENTIAL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

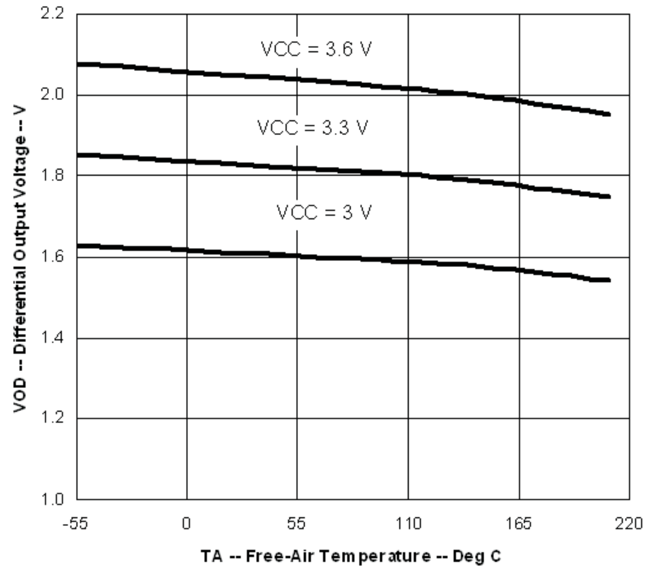


Figure 20.

RECEIVER LOW-TO-HIGH PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

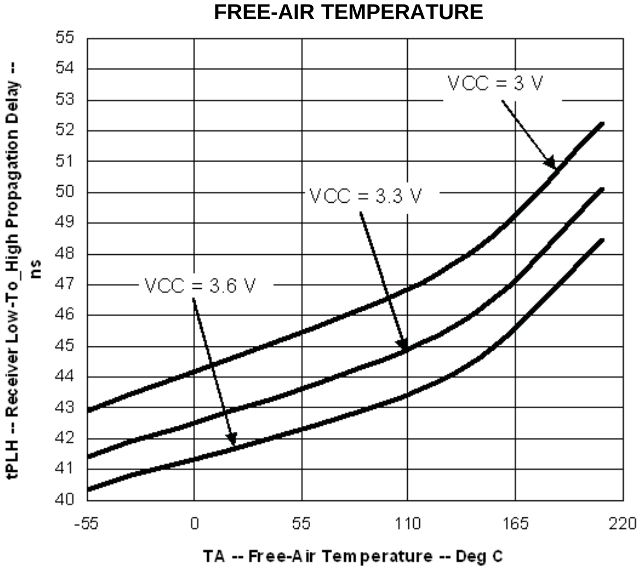


Figure 21.

RECEIVER HIGH-TO-LOW PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

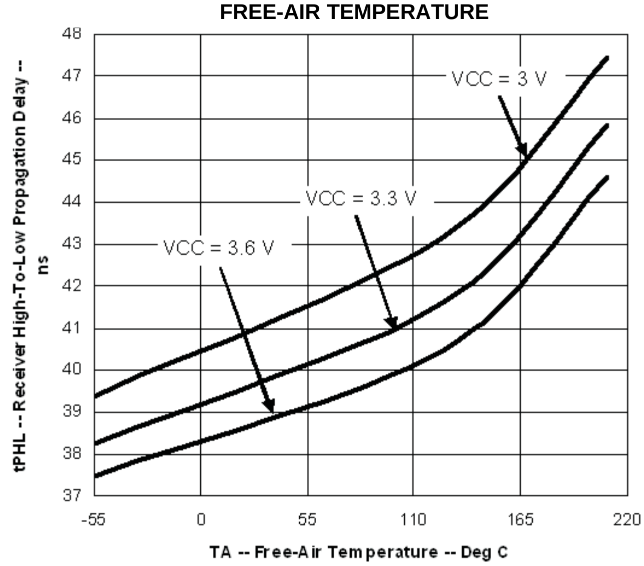


Figure 22.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

DRIVER LOW-TO-HIGH PROPAGATION DELAY vs FREE-AIR TEMPERATURE

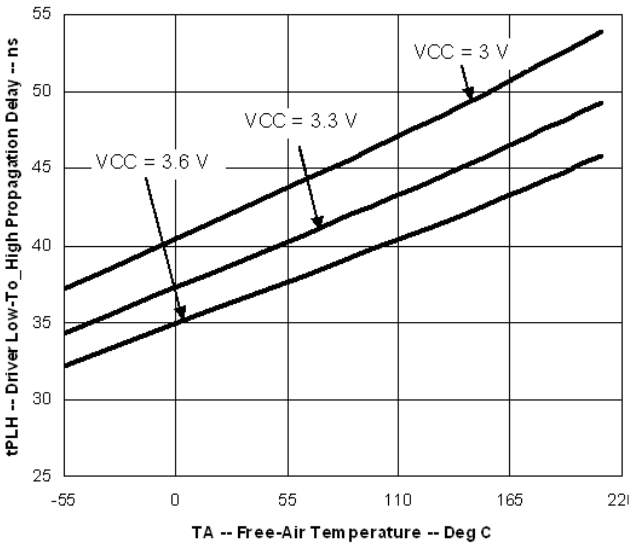


Figure 23.

DRIVER HIGH-TO-LOW PROPAGATION DELAY vs FREE-AIR TEMPERATURE

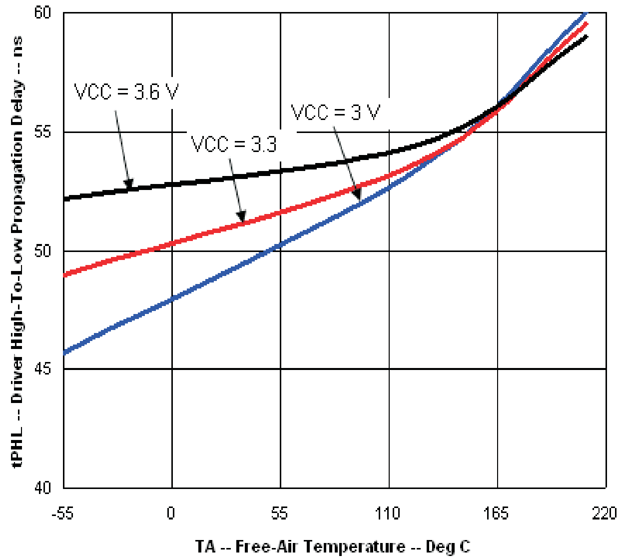


Figure 24.

DRIVER OUTPUT CURRENT vs SUPPLY VOLTAGE

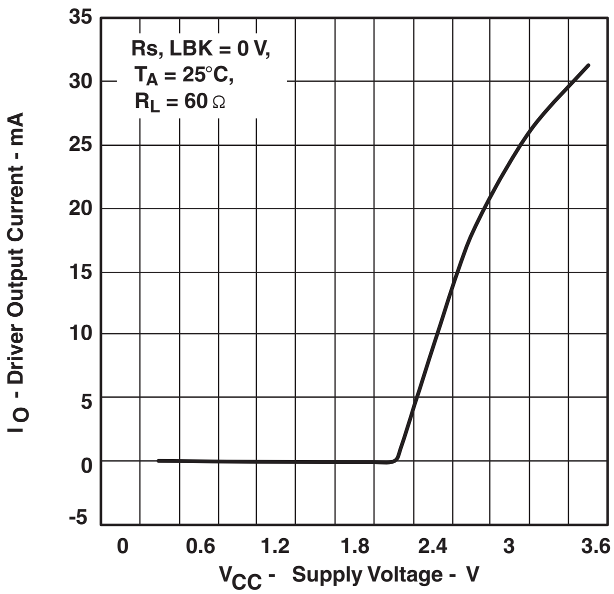


Figure 25.

PRODUCT PREVIEW

APPLICATION INFORMATION

Diagnostic Loopback

The loopback (LBK) function of the SN65HVD233 is enabled with a high-level input to pin 5. This forces the driver into a recessive state and redirects the data (D) input at pin 1 to the received-data (R) output at pin 4. This allows the host controller to input and read back a bit sequence to perform diagnostic routines without disturbing the CAN bus. A typical CAN bus application is displayed in Figure 26.

If the LBK pin is not used, it may be tied to ground (GND). However, it is pulled low internally (defaults to a low-level input) and may be left open if not in use.

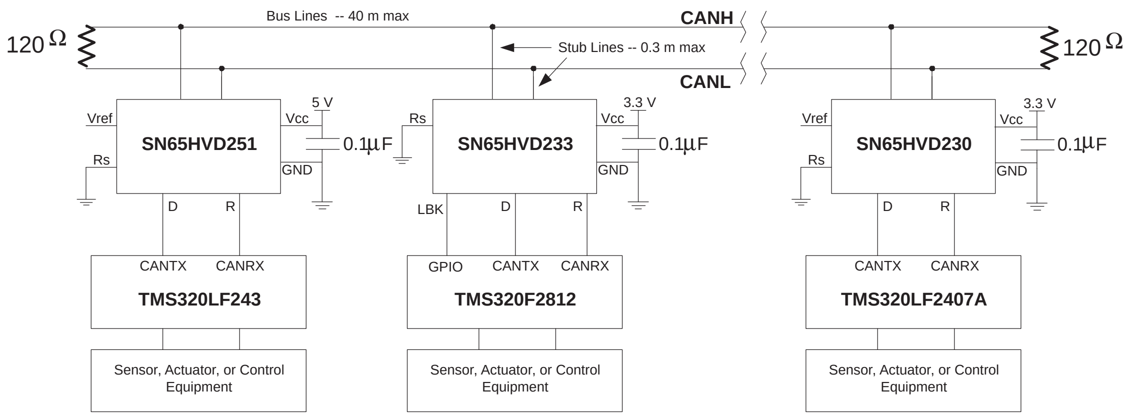


Figure 26. Typical SN65HVD233 Application

ISO 11898 Compliance of SN65HVD230 Family of 3.3-V CAN Transceivers

Introduction

Many users value the low power consumption of operating CAN transceivers from a 3.3-V supply. However, some are concerned about the interoperability with 5-V supplied transceivers on the same bus. This section analyzes this situation to address those concerns.

Differential Signal

CAN is a differential bus where complementary signals are sent over two wires, and the voltage difference between the two wires defines the logical state of the bus. The differential CAN receiver monitors this voltage difference and outputs the bus state with a single-ended output signal.

PRODUCT PREVIEW

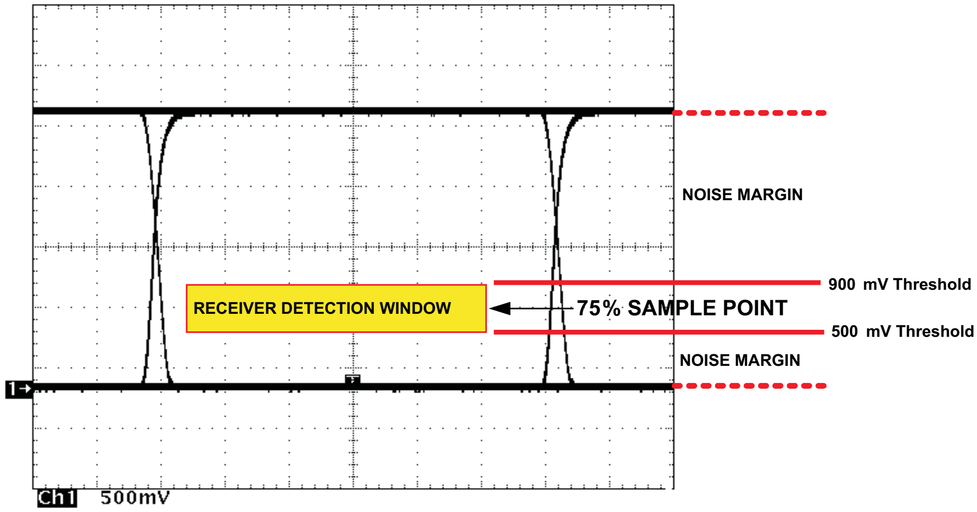


Figure 27. Typical SN65HVD230 Differential Output Voltage Waveform

The CAN driver creates the difference voltage between CANH and CANL in the dominant state. The dominant differential output of the SN65HVD230 is greater than 1.5 V and less than 3 V across a 60-Ω load. The minimum required by ISO 11898 is 1.5 V and the maximum is 3 V. These are the same limiting values for 5-V supplied CAN transceivers. The bus termination resistors drive the recessive bus state and not the CAN driver.

A CAN receiver is required to output a recessive state with less than 500 mV and a dominant state with more than 900-mV difference voltage on its bus inputs. The CAN receiver must do this with common-mode input voltages from –2 V to 7 V. The SN65HVD230 family receivers meet these same input specifications as 5-V supplied receivers.

Common-Mode Signal

A common-mode signal is an average voltage of the two signal wires that the differential receiver rejects. The common-mode signal comes from the CAN driver, ground noise, and coupled bus noise. Obviously, the supply voltage of the CAN transceiver has nothing to do with noise. The SN65HVD230 family driver lowers the common-mode output in a dominant bit by a couple hundred millivolts from that of most 5-V drivers. While this does not fully comply with ISO 11898, this small variation in the driver common-mode output is rejected by differential receivers and does not affect data, signal noise margins, or error rates.

Interoperability of 3.3-V CAN in 5-V CAN Systems

The 3.3-V–supplied SN65HVD23x family of CAN transceivers are electrically interchangeable with 5-V CAN transceivers. The differential output is the same. The recessive common-mode output is the same. The dominant common-mode output voltage is a couple hundred millivolts lower than 5-V–supplied drivers, while the receivers exhibit identical specifications as 5-V devices.

Electrical interoperability does not assure interchangeability however. Most implementers of CAN buses recognize that ISO 11898 does not sufficiently specify the electrical layer and that strict standard compliance alone does not ensure interchangeability. This comes only with thorough equipment testing.

Bus Cable

ISO 11898 specifies a maximum bus length of 40 m and maximum stub length of 0.3 m with a maximum of 30 nodes. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires a transceiver with high input impedance, such as the SN65HVD233.

The standard specifies the interconnect to be a single twisted-pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections.

Slope Control

The rise and fall slope of the SN65HVD233 driver output can be adjusted by connecting a resistor from R_s (pin 8) to ground (GND), or to a low-level input voltage (see Figure 28).

The slope of the driver output signal is proportional to the pin's output current. This slope control is implemented with an external resistor value of 10 kΩ to achieve a ≈15-V/µs slew rate, and up to 100 kΩ to achieve a ≈2.0- V/µs slew rate (see Figure 29). Typical driver output waveforms with slope control are displayed in Figure 30.

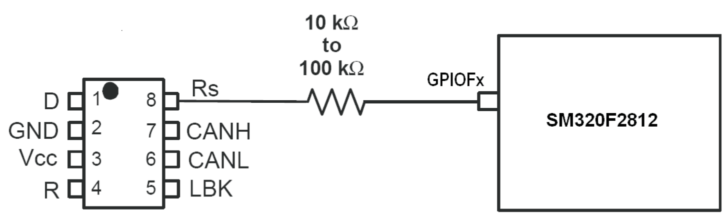


Figure 28. Slope Control/Standby Connection to DSP

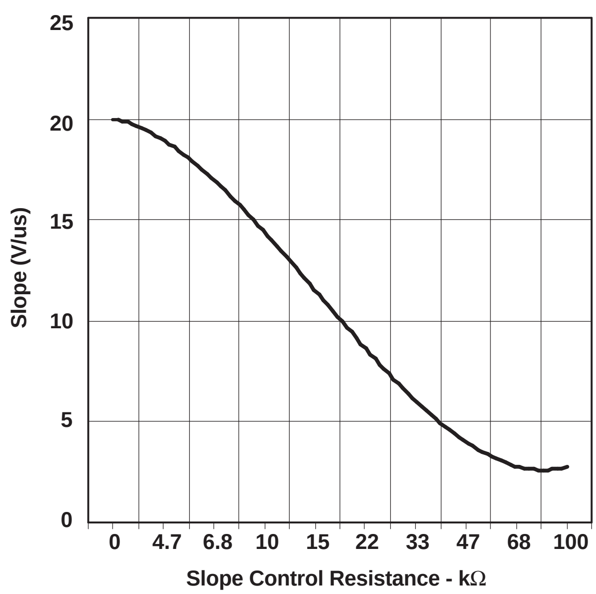


Figure 29. SN65HVD233 Driver Output Signal Slope vs Slope Control Resistance Value

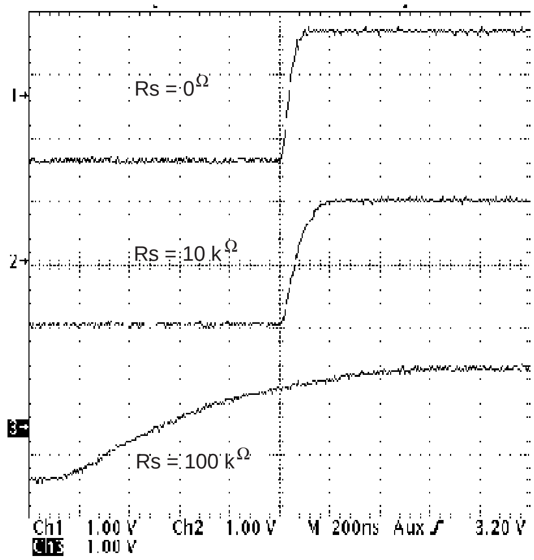


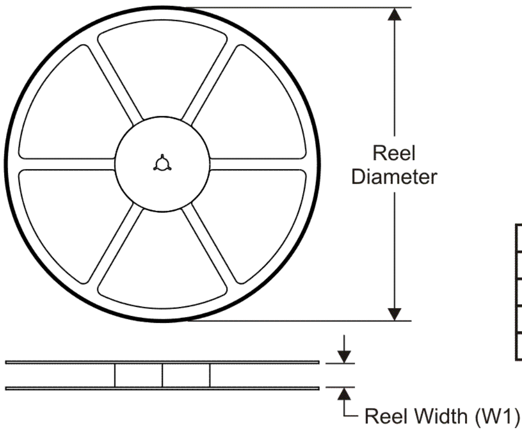
Figure 30. Typical SN65HVD233 250-kbps Output Pulse Waveforms With Slope Control

STANDBY

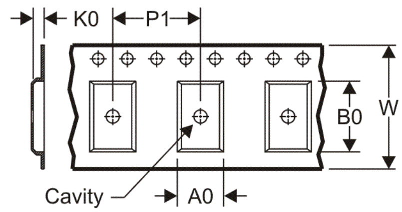
If a high-level input (>0.75 V_{CC}) is applied to R_s, the circuit enters a low-current, *listen-only* standby mode, during which the driver is switched off and the receiver remains active. The local controller can reverse this low-power standby mode when the rising edge of a dominant state (bus differential voltage >900 mV typical) occurs on the bus.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

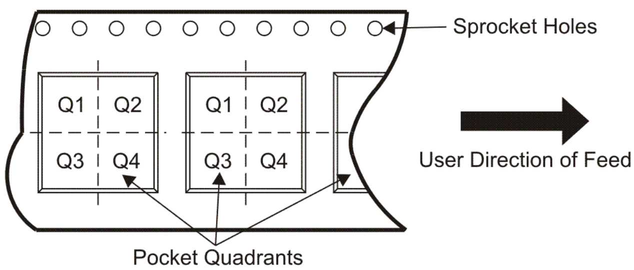


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

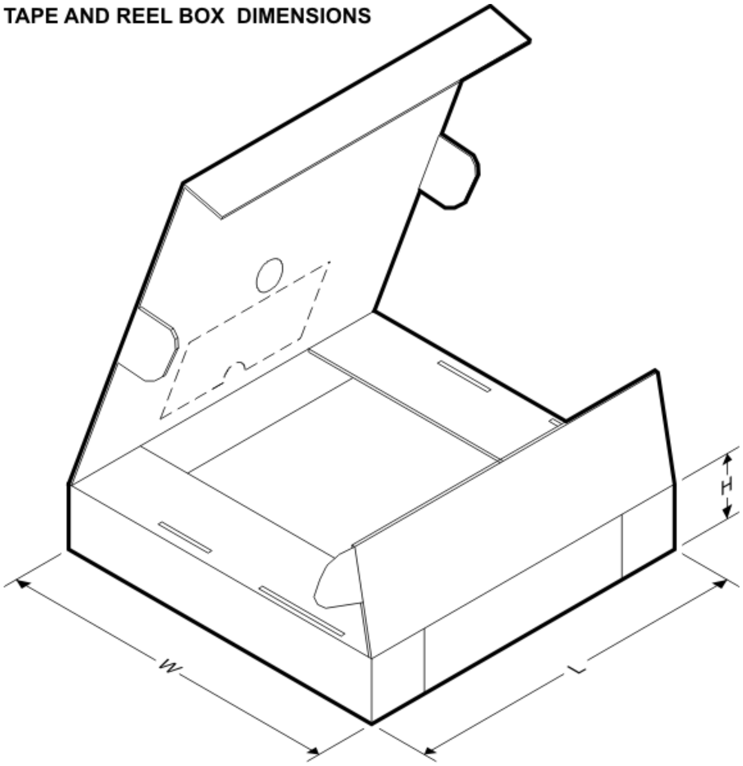
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD233DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD234DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD235DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD233DR	SOIC	D	8	2500	340.5	338.1	20.6
SN65HVD234DR	SOIC	D	8	2500	340.5	338.1	20.6
SN65HVD235DR	SOIC	D	8	2500	340.5	338.1	20.6