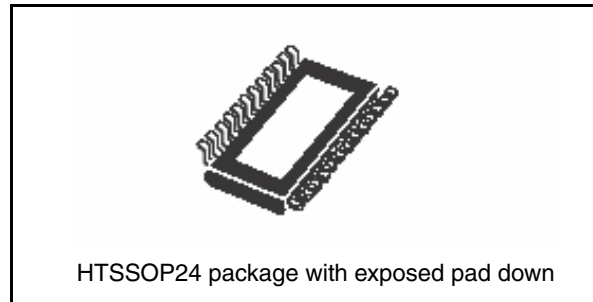


3 W + 3 W dual BTL class-D audio amplifier

Features

- 3.0 W + 3.0 W continuous output power
 $R_L = 4 \Omega$, THD = 10%, $V_{CC} = 5 \text{ V}$ (filterless)
- 2.8 W + 2.8 W continuous output power
 $R_L = 4 \Omega$, THD = 10%, $V_{CC} = 5 \text{ V}$ (with filter)
- Single supply voltage range 3.0 V to 5.5 V
- High efficiency ($\eta = 83\%$)
- Four selectable, fixed gain settings of 6 dB, 12 dB, 15.6 dB and 18 dB
- Differential inputs minimize common-mode noise
- Filterless operation
- Standby feature
- Short-circuit protection
- Thermal-overload protection
- Externally synchronizable



Description

The TDA7493 is a dual BTL class-D audio amplifier, specially designed for LCD TV, LCD monitors or small speakers on cradles with single-supply operation.

The filterless operation allows the external component count to be reduced.

The TDA7493 is assembled in the HTSSOP24 package. Thanks to the high-efficiency and to the exposed-pad-down (EPD) package no separate heatsink is required.

Table 1. Device summary

Order codes	Operating temperature range	Package	Packaging
TDA7493	0 to 70 °C	HTSSOP24 (EPD)	Tube
TDA749313TR	0 to 70 °C	HTSSOP24 (EPD)	Tape and reel

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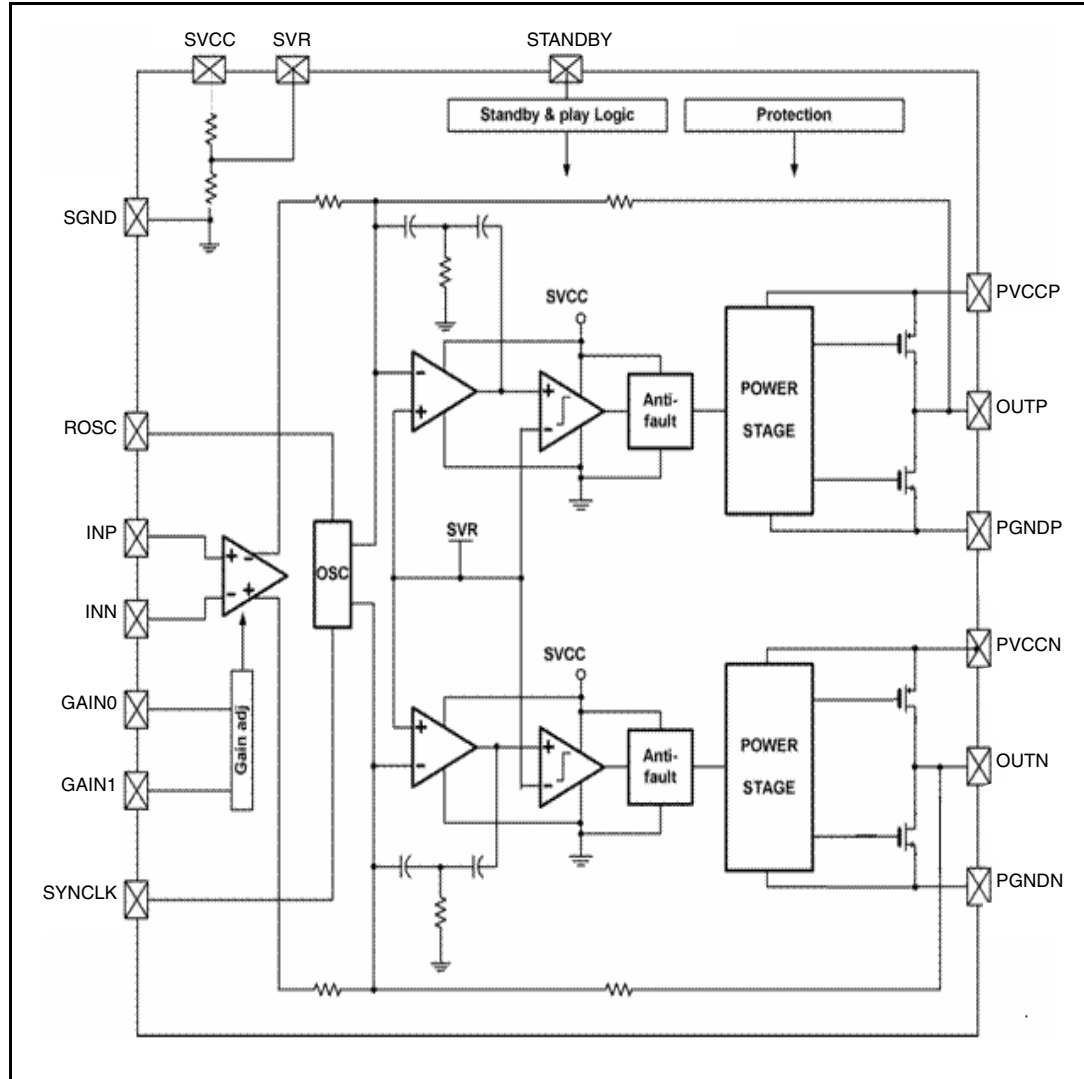
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1 Device block diagram

Figure 1 shows the block diagram of one of the two identical channels of the TDA7493.

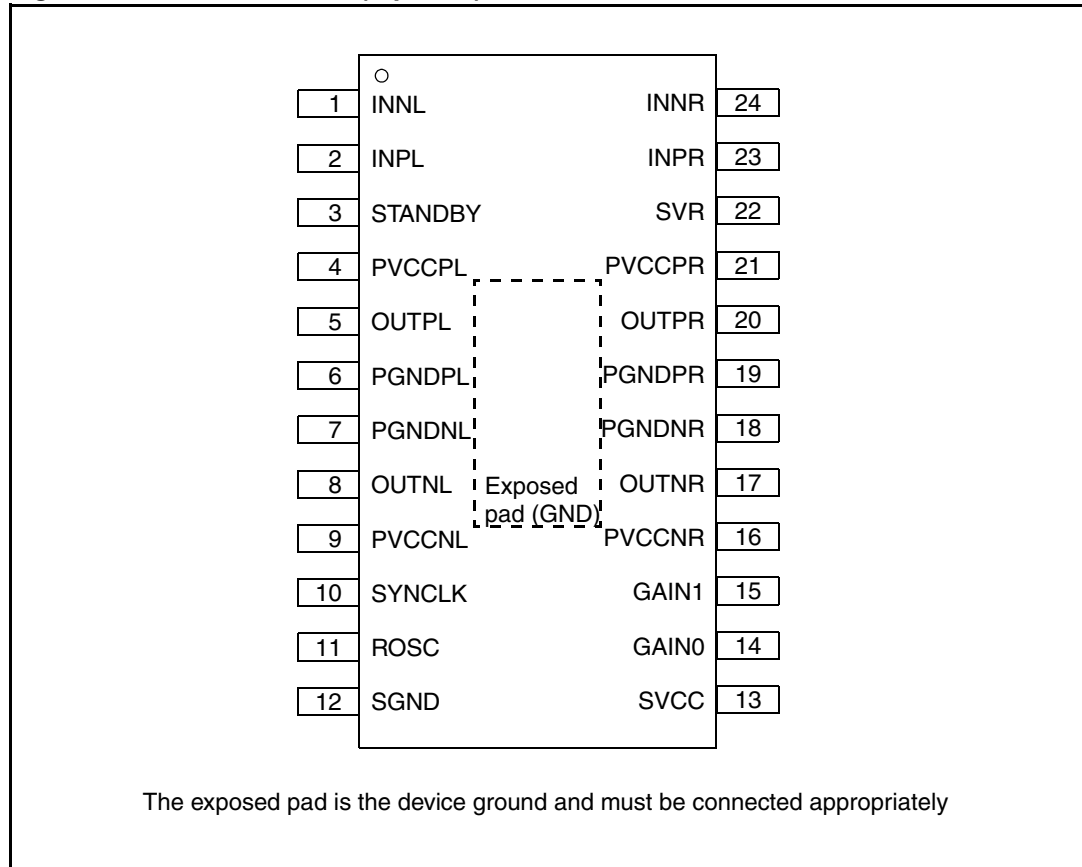
Figure 1. TDA7493 block diagram (only one of two channels shown)



2 Pin description

2.1 Pin-out

Figure 2. Pin connection (top view)



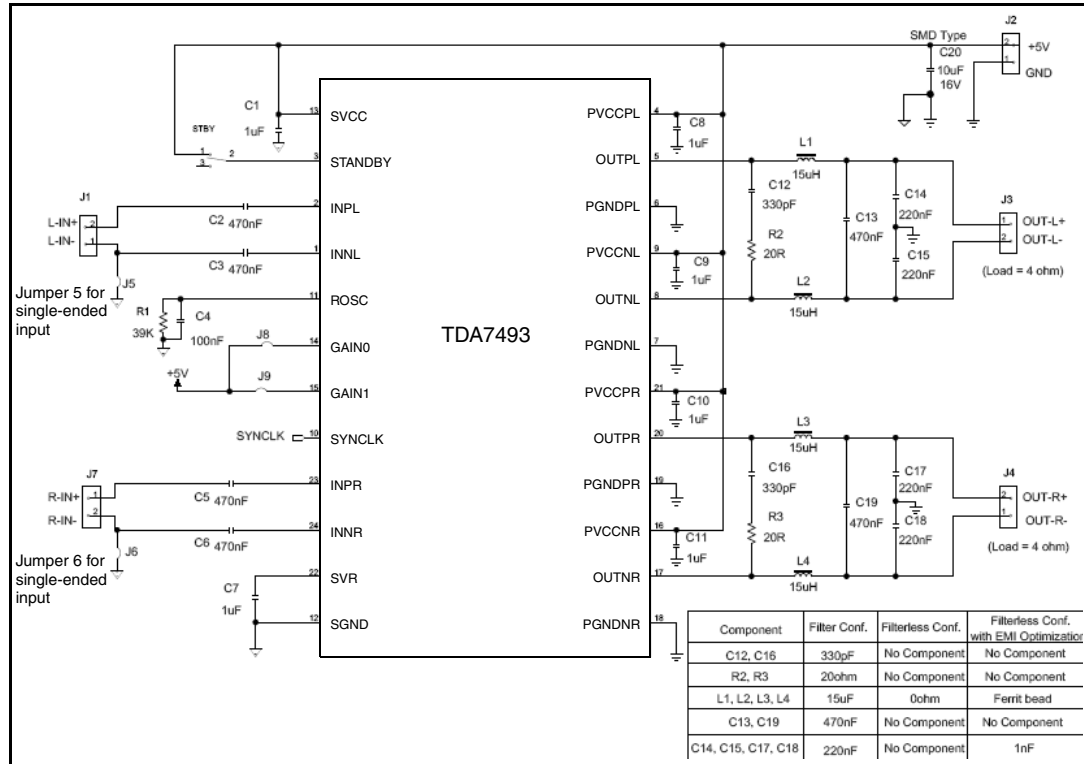
2.2 Pin list

Table 2. Pin list

Number	Name	Type	Description
1	INNLL	IN	Negative differential input of left channel
2	INPL	IN	Positive differential input of left channel
3	STANDBY	IN	Standby mode control (digital): 0: standby 1: play
4	PVCCPL	POWER	Power supply for positive branch in left channel
5	OUTPL	OUT	Positive PWM output for left channel
6	PGNDPL	POWER	Power stage ground for left channel
7	PGNDNL	POWER	Power stage ground for left channel
8	OUTNL	OUT	Negative PWM output for left channel
9	PVCCNL	POWER	Power supply for negative branch in left channel
10	SYNCLK	IN/OUT	Clock in/out for external oscillator
11	ROSC	OUT	Master oscillator frequency setting pin
12	SGND	POWER	Signal ground
13	SVCC	POWER	Signal power supply
14	GAIN0	IN	Gain setting input 1
15	GAIN1	IN	Gain setting input 2
16	PVCCNR	POWER	Power supply for negative branch in right channel
17	OUTNR	OUT	Negative PWM output for right channel
18	PGNDNR	POWER	Power stage ground for right channel
19	PGNDPR	POWER	Power stage ground for right channel
20	OUTPR	OUT	Positive PWM output for right channel
21	PVCCPR	POWER	Power supply for positive branch in right channel
22	SVR	OUTPUT	Supply voltage rejection
23	INPR	IN	Positive differential input of right channel
24	INNER	IN	Negative differential input of right channel

3 Application circuit

Figure 3. Typical application circuit



4 Electrical specifications

4.1 Absolute maximum ratings

Table 3. Absolute maximum rating

Symbol	Parameter	Negative value	Positive value	Unit
V_{CC}	DC supply on pins PVCCPL, PVCCPR, PVCCNL, PVCCNR, SVCC	-0.3	6	V
V_i	Input on pins STANDBY, INNL, INPL, INNR, INPR, GAIN0, GAIN1	-0.3	6	V
Top	Operating temperature	0	70	°C
Tstg, Tj	Storage and junction temperature	-40	150	°C

4.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
Rth j-case	Thermal resistance junction to case	-	2	3	°C/W
Rth j-amb	Thermal resistance junction to ambient (on recommended PCB) ⁽¹⁾	-	37	-	°C/W

1. FR4 with via holes, copper area 9 cm² as explained in [Chapter 8 on page 28](#).

4.3 Electrical characteristics

Refer to [Figure 3: Typical application circuit](#), $V_{CC} = 5$ V, R_L (load) = 4 Ω , $R_1 = 39$ k Ω , $C_4 = 100$ nF, $f = 1$ kHz, $G_V = 18$ dB, $T_{amb} = 25$ °C, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply range	-	3.0	-	5.5	V
I_q	Total quiescent current	No filter, no load	-	7	-	mA
V_{os}	Output offset voltage	$V_i = 0$, $G_v = 6$ dB, no load	-20	-	20	mV
P_o	Output power (filterless)	THD = 10%	-	3.0	-	W
		THD = 1%	-	2.4	-	W
P_o	Output power (with filter)	THD = 10%	-	2.8	-	W
		THD = 1%	-	2.2	-	W
P_d	Dissipated power	$P_o = 2.8$ W + 2.8 W, THD = 10%	-	1.1	-	W
η	Efficiency	$P_o = 2.8$ W + 2.8 W, $R_L = 4$ Ω	-	83	-	%

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit	
THD	Total harmonic distortion	$R_L = 4 \Omega, P_o = 0.5 W$	-	0.05	-	%	
T_j	Thermal shut-down junction temperature	-	-	150	-	$^{\circ}C$	
G_V	Closed loop gain	$GAIN0 = low$	$GAIN1 = low$	-	6.0	-	dB
			$GAIN1 = high$	-	12.0	-	
		$GAIN0 = high$	$GAIN1 = low$	-	15.6	-	
			$GAIN1 = high$	-	18.0	-	
G_V	Gain matching	-	-1	-	1	dB	
CT	Crosstalk	$f = 1 kHz$	-	60	-	dB	
e_N	Total output noise	A curve, $G_V = 18 dB$	-	50	-	μV	
		$f = 22 Hz$ to $22 kHz$, $G_V = 18 dB$	-	60	-	μV	
R_i	Input resistance	Differential Input	-	60	-	$k\Omega$	
SVRR	Supply voltage rejection ratio	$f_r = 100 Hz, V_r = 0.5 V,$ $C_{SVR} = 1 \mu F$	-	55	-	dB	
V_{OVP}	Overvoltage protection threshold	-	-	5.8	-	V	
t_r, t_f	Rising and falling time	-	-	10	-	ns	
R_{DSON}	Power transistor on resistance	High side	-	0.44	-	Ω	
		Low side	-	0.36	-		
f_{SW}	Switching frequency	Internal oscillator	-	315	-	kHz	
f_{SWR}	Output switching frequency range	With internal oscillator ⁽¹⁾	250	-	400	kHz	
		With external oscillator ⁽²⁾	250	-	400	kHz	
$I_{qSTANDBY}$	Quiescent current in standby	-	-	1	-	μA	
Function mode	Standby and play	STANDBY = high	Play			-	
		STANDBY = low	Standby				
Digital inputs	Digital input thresholds	High	$0.7 * V_{CC}$	-	-	V	
		Low	-	-	$0.3 * V_{CC}$	V	

1. $f_{SW} = 10^6 / (R_{OSC} * 64 + 840)$
 $f_{SYNC} = 2 * f_{SW}$ with $R1 = 39 k\Omega$ and f_{SW} in kHz

2. $f_{SW} = f_{SYNC} / 2$ with the frequency of external oscillator

5 Application information

5.1 Mode selection

Pin STANDBY selects the operating mode, namely standby or play.

- In standby mode, all the circuits are turned off and there is very low leakage current.
- In play mode, the amplifiers are powered up.

During the turn on/off sequence, there are four operational states: standby, pre-charge, mute and play. The pre-charge and mute states are two internal transient states to set up the normal operating condition and to reduce the speaker pop noise.

Table 6. Mode selection

Logic level on pin STANDBY	Mode
0	Standby
1	Play

Note: An internal pull-down resistor on pin STANDBY ensures that the default mode is standby.

5.2 Gain setting

The close loop gain is set by pins GAIN0 and GAIN1 as shown below in [Table 7](#). The gain setting is implemented by changing the feedback resistors of the amplifiers.

Table 7. Gain selection

Logic level on pin GAIN0	Logic level on pin GAIN1	Gv (nominal)
0	0	6.0 dB
0	1	12.0 dB
1	0	15.6 dB
1	1	18.0 dB

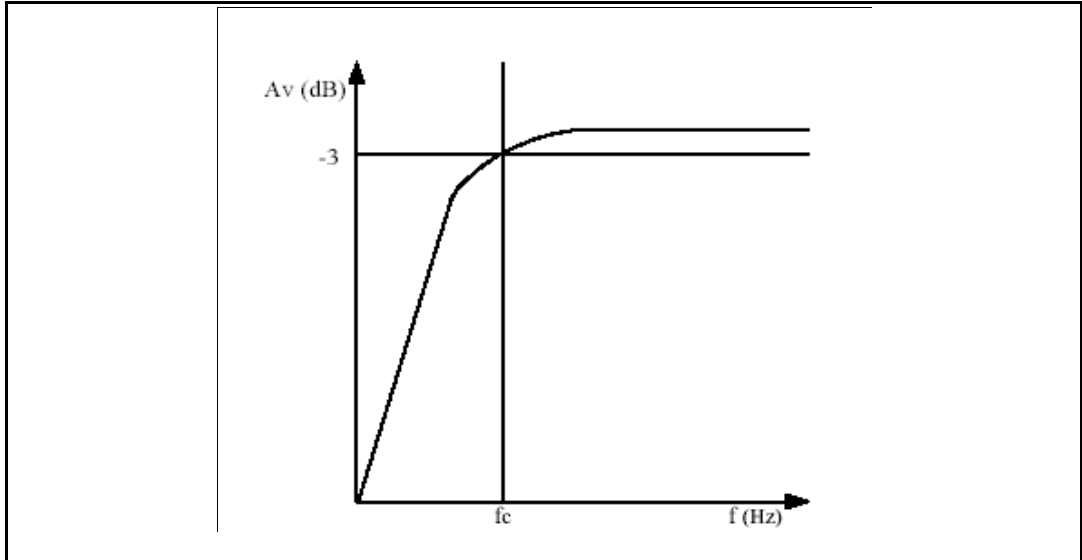
Note: Internal pull-down resistors on pins GAIN0 and GAIN1 ensure that the default gain is 6 dB.

5.3 Input resistance and capacitance

The input impedance is set by an internal resistor, R_i , of value 60 k Ω . An input coupling capacitor (C_i) is required on each input line. These two components together form a high-pass filter whose cutoff frequency is:

$$f_C = 1 / (2 * \pi * R_i * C_i)$$

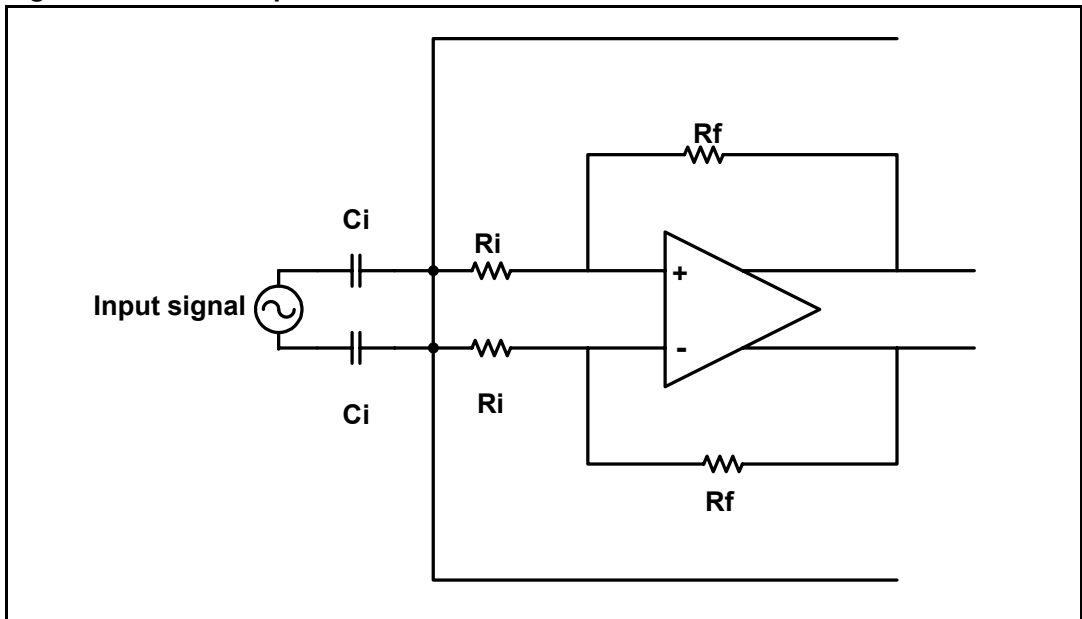
Figure 4. Input high-pass RC filter



The value of C_i is chosen depending on the application and the speaker system. For a cut-off frequency less than 20 Hz, the input capacitors could be 470 nF each.

If a polarized capacitor is used, it is important to connect the positive side of the capacitor to the terminal with higher DC voltage. The DC voltage on the input pins is $V_{CC} / 2$.

Figure 5. Device input structure

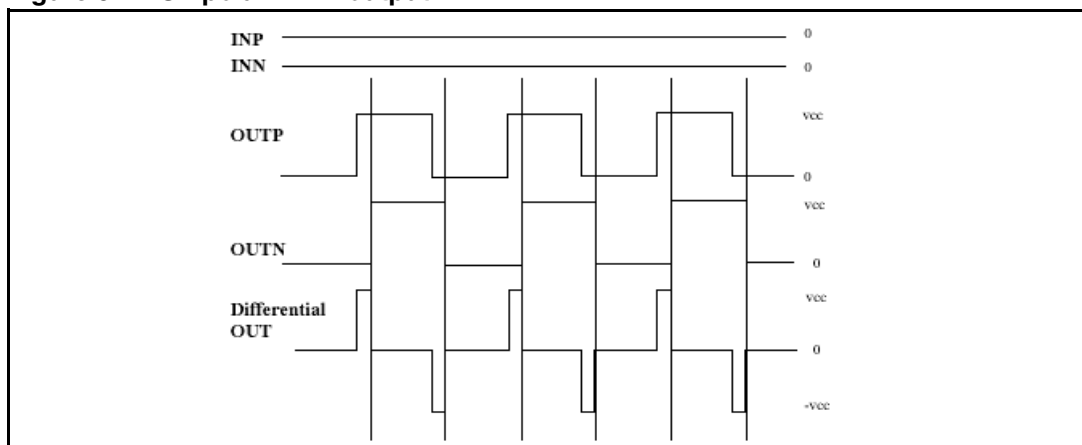


5.4 Filterless modulation

The modulation scheme of BTL is called unipolar PWM output. The differential output voltage changes between zero and $+V_{CC}$ or between zero and $-V_{CC}$, as opposed to the traditional bipolar PWM output between $+V_{CC}$ and $-V_{CC}$. The other advantage of this scheme effectively doubles the switching frequency of the differential output waveform. Signals on OUTP and OUTN are in the same phase when the input is zero, thus the current is greatly reduced and the loss in the load is small. A tiny delay between OUTP and OUTN is introduced to avoid high transient currents which could occur if both outputs switch simultaneously.

TDA7493 can be used without a filter between the PWM output and the speaker since the switching frequency of the output is beyond the audible range. The audio signal can be recovered by the inherent inductance of the speaker and natural filter of the human ear.

Figure 6. Unipolar PWM output

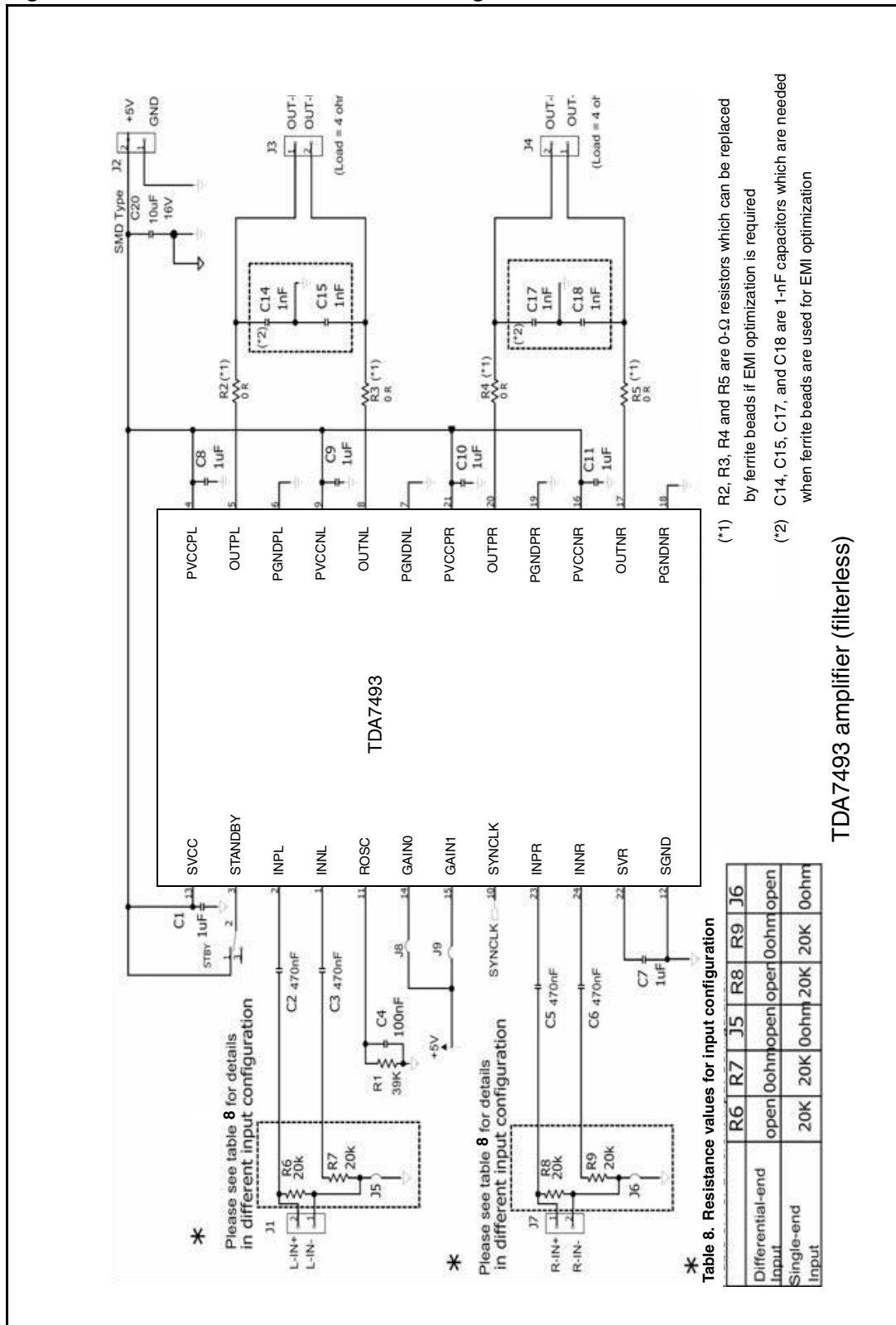


The filterless configuration is usable in applications where the speaker connections to the amplifier are shorter than 50 cm. In comparison to the low-pass Butterworth filter configuration, the filterless configuration gives rise to higher EMI. This can be reduced, if necessary, by inserting a ferrite bead filters close to the device.

Use a ferrite which exhibits high impedance at around 1 MHz and negligible impedance in the audio band.

It is recommended to use an EMI filter if the speaker cable is longer than 50 cm.

Figure 7. Schematic for the filterless configuration



5.5 Internal clock and external clock

The clock of the class-D amplifier can be generated internally or it can be synchronous with the external clock. If two or more class-D amplifiers are used in the same system, it is better to have all devices working at the same frequency. This is realized by using one TDA7493 as clock master and the others as slaves. All SYNCLK pins are connected together as shown in *Figure 8*.

In master mode or with a single TDA7493, the output switching frequency is controlled by the resistor connected to pin ROOSC. The switching frequency is:

$$f_{SW} = 10^6 / (R_{OSC} * 64 + 840)$$

where R_{OSC} is in $k\Omega$ and f_{SW} is in kHz.

In this configuration pin SYNCLK is an output whose frequency is also determined by R_{OSC} :

$$f_{SYNCLK} = 10^6 / (R_{OSC} * 32 + 420) = 2 * f_{SW}$$

Note: R_{OSC} should be lower than 60 $k\Omega$ in master mode to avoid operating in error mode.

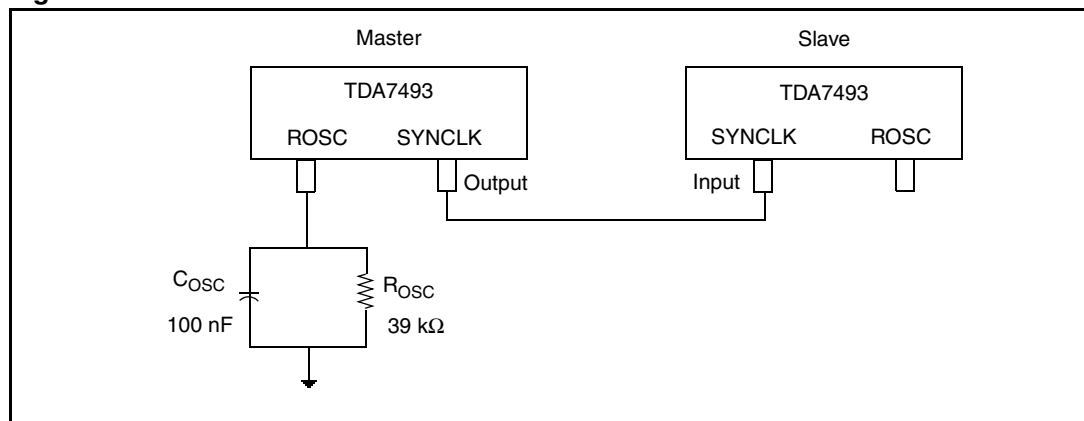
In slave mode, pin ROOSC can be floating to force pin SYNCLK as input in order to accept the master clock. The switching frequency in this mode is:

$$f_{SW} = f_{SYNCLK} / 2$$

Table 9. Master and slave mode

Mode	Pin ROOSC	Pin SYNCLK
Master	$R_{OSC} < 60\ k\Omega$	Output
Slave	Floating	Input

Figure 8. Master and slave modes



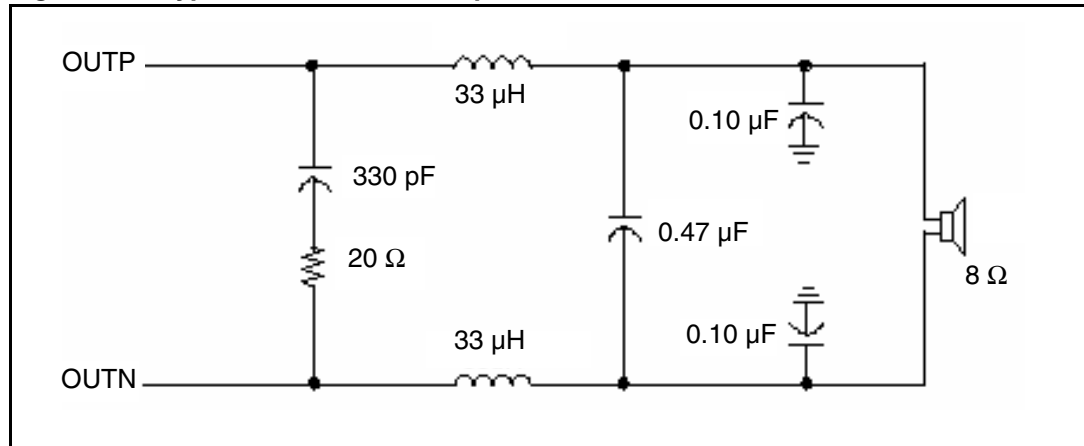
5.6 Output low-pass filter

To avoid EMI problems, a low-pass filter can be inserted before the speaker. The cut-off frequency of the filter should be higher than 22 kHz and much lower than the switching frequency.

The component values of the filter vary according to the speaker impedance.

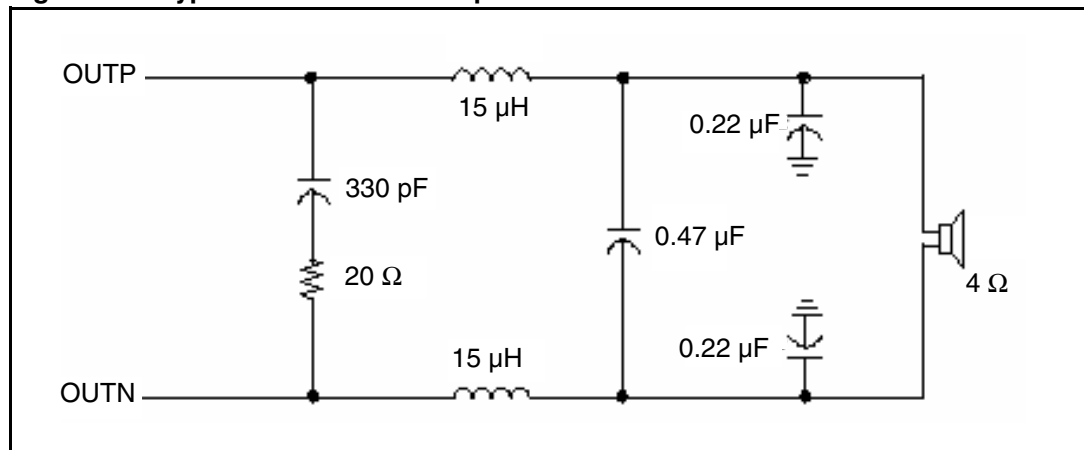
A typical LC output filter for a speaker impedance of 8 Ω and with a cut-off frequency of 27 kHz is shown in [Figure 9](#).

Figure 9. Typical LC filter for 8 Ω speaker



A similar filter for a speaker impedance of 4 Ω and also with a cut-off frequency of 27 kHz is shown in [Figure 10](#).

Figure 10. Typical LC filter for 4 Ω speaker



5.7 Protection function

The TDA7493 has four types of protection: overvoltage (OV), undervoltage (UV), thermal (OT) and short circuit (SC):

- overvoltage protection (OVP) for the supply $V_{CC} > 6\text{ V}$
- undervoltage protection (UVP) for the supply $V_{CC} < 3\text{ V}$
- thermal protection (OTP) for the junction temperature $T_j > 155\text{ °C}$
- short-circuit protection (SCP) across the load (tested at $V_{CC} = 5.0\text{ V}$).

When any of the above protection becomes active, the output goes to a high-impedance state. The device remains in this state until the condition is cleared or rectified, when the circuit restarts again.

5.8 Differential input

The TDA7493 can be used with either differential or single-ended inputs. In either case, the device must be AC coupled to the audio source.

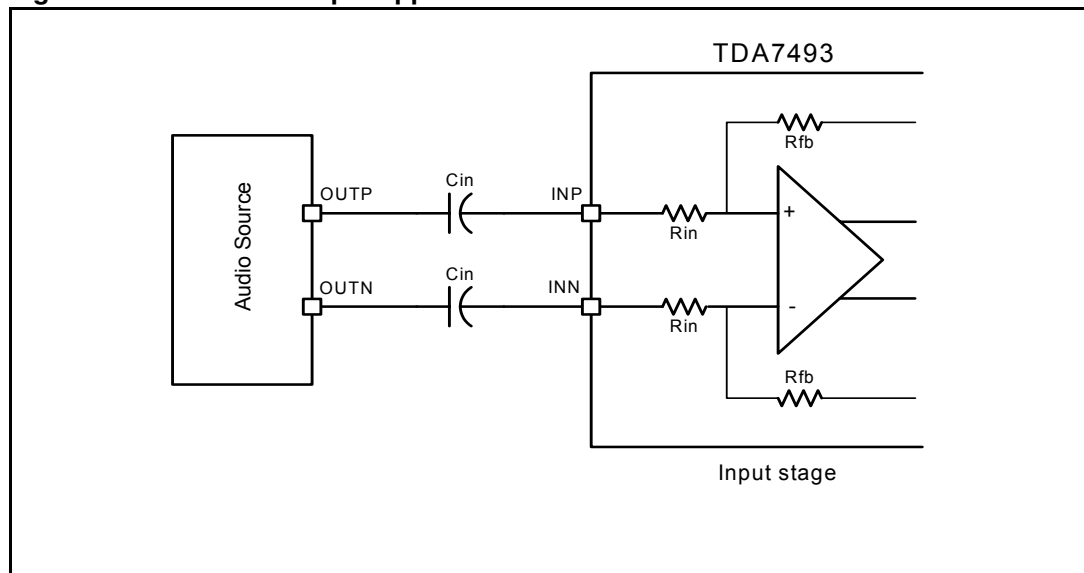
To use the device with a differential source, connect the positive lead from the audio source to the INP input and the negative lead to the INN input as shown in [Figure 11](#). The differential input stage of the amplifier minimizes the common mode noise effectively.

In the differential input application:

- input impedance is given by $2 * R_{in}$,
- cut-off frequency of the input filter is given by $f_c = 1 / (2 * \pi * C_{in} / 2 * 2 * R_{in}) = 1 / (2 * \pi * C_{in} * R_{in})$.

Typically, $R_{in} = 30\text{ k}\Omega$ and $C_{in} > 330\text{ nF}$ to get a cut-off frequency less than 20 Hz.

Figure 11. Differential input application

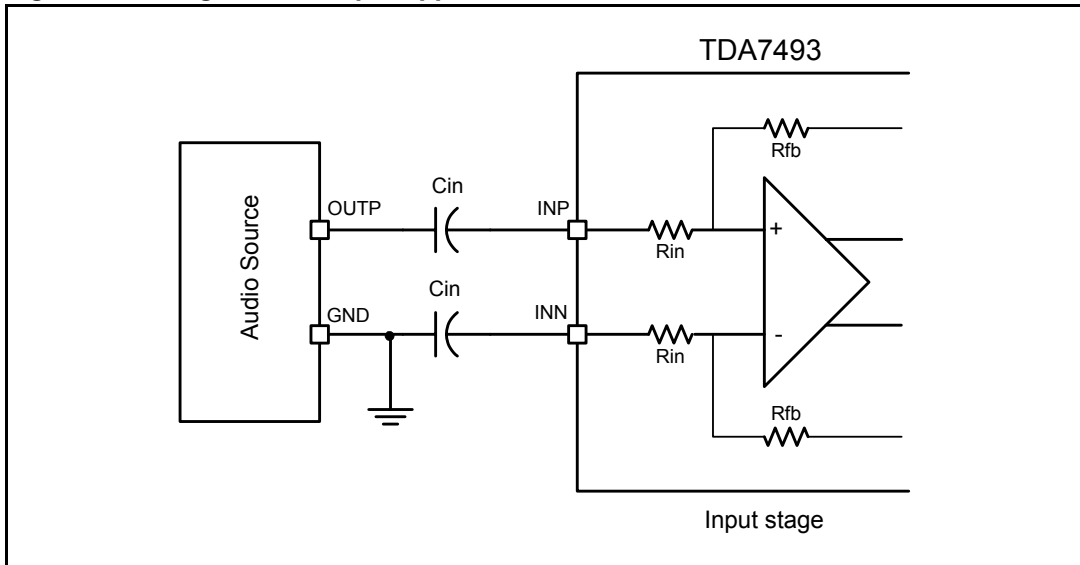


5.8.1 Single-ended input application

To use the device with a single-ended source, one input is AC connected to ground (via a capacitor) and the other input is connected to the audio source. This is designed as a fully differential input. The input scheme is shown in *Figure 12*.

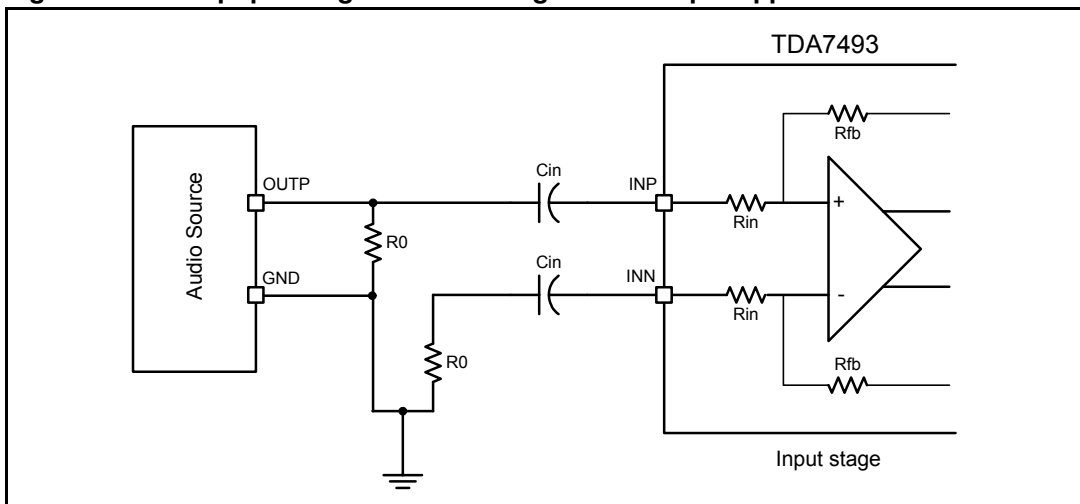
However, to avoid the start-up pop noise, it is important to equalize, as much as possible, the charging currents in the positive and negative inputs. Any imbalance in these charging currents will be amplified and result in the familiar turn-on pop.

Figure 12. Single-ended input application



Since the input charging currents in the circuit of *Figure 12* can be different it is necessary to add two resistors, R_0 , as shown in the circuit of *Figure 13*. In this way the currents in the two branches of the differential input are better balanced and this can lead to the elimination of the turn-on pop noise.

Figure 13. Anti-pop configuration for single-ended input application

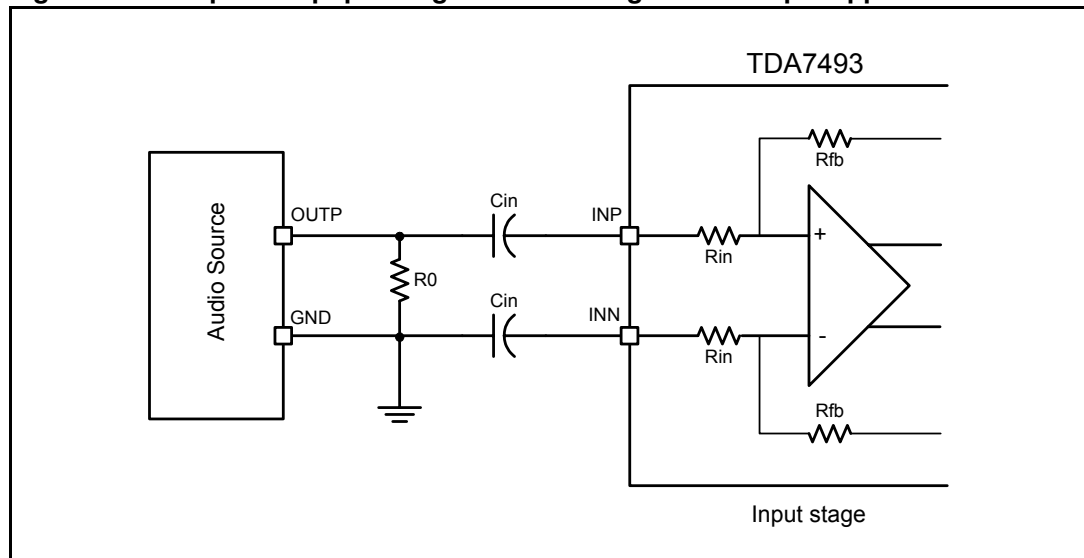


The disadvantages of the anti-pop configuration are given below:

- The input impedance or the load of audio source is no longer $2 * R_{in}$ as in the case of differential input configuration but R_0 . It means the load effect should be considered during the application design. At this point, bigger R_0 is better because of the lower load effect.
- The input signal is also equivalent to $V_{in_actual} = V_{in} * 2 * R_{in} * (R_{in} + R_{fb} + R_0) / (2 * R_{in} * (R_{in} + R_{fb} + R_0) + R_{fb} * R_0)$, not the original V_{in} which means the actual gain is reduced.
When $R_{in} = 30 \text{ k}\Omega$, $R_{fb} = 30 \text{ k}\Omega$ and $R_0 = 20 \text{ k}\Omega$, the gain is reduced by 1 dB.
When $R_{in} = 30 \text{ k}\Omega$, $R_{fb} = 120 \text{ k}\Omega$ and $R_0 = 20 \text{ k}\Omega$, the gain is reduced by 1.84 dB. In this case, smaller R_0 is better.

If the pop noise is not critical, the anti-pop configuration can be simplified as shown in [Figure 14](#). The suggested value of the resistor R_0 is $20 \text{ k}\Omega$.

Figure 14. Simple anti-pop configuration for single-ended input application



6 Electrical characterization curves

6.1 For the configuration with LC filter

- Test setup as given in [Figure 3 on page 8](#)
- Test conditions $V_{CC} = 5\text{ V}$, $C_{20} = 10\ \mu\text{F}$, $R_L = 4\ \Omega$, LC filter $15\ \mu\text{H}$, $470\ \text{nF}$

Figure 15. THD vs output power at 1 kHz

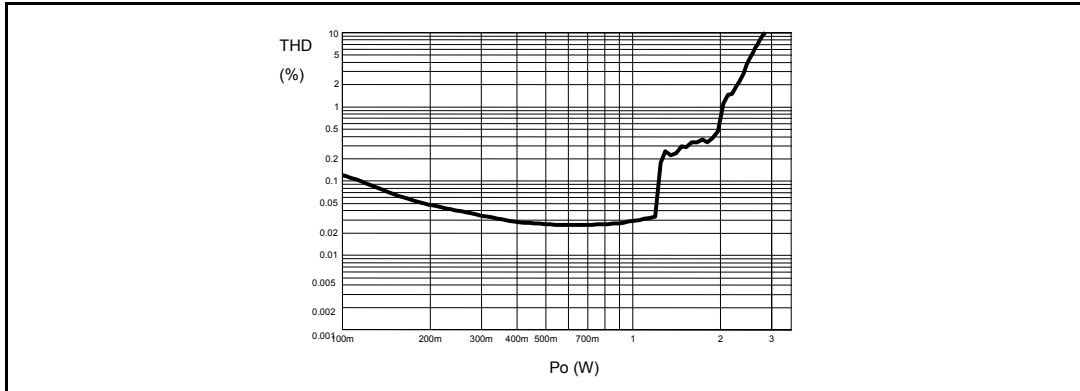


Figure 16. THD vs output power at 100 Hz

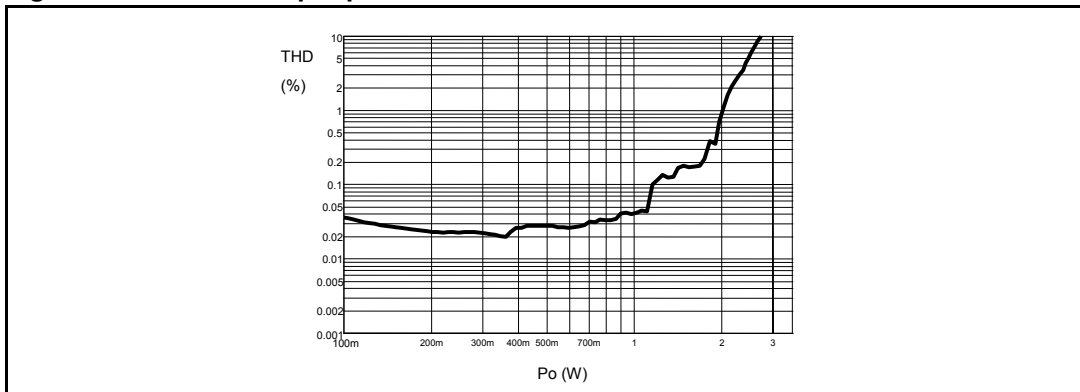


Figure 17. THD vs frequency at 100 mW

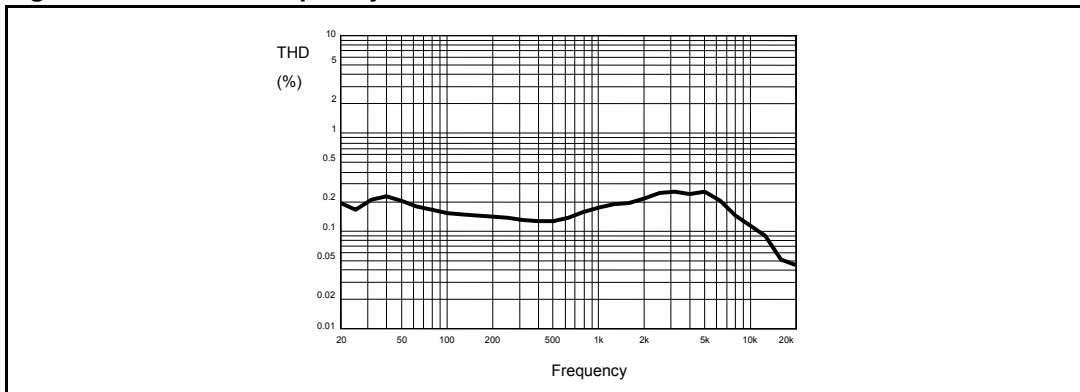


Figure 18. THD vs frequency at 1 W

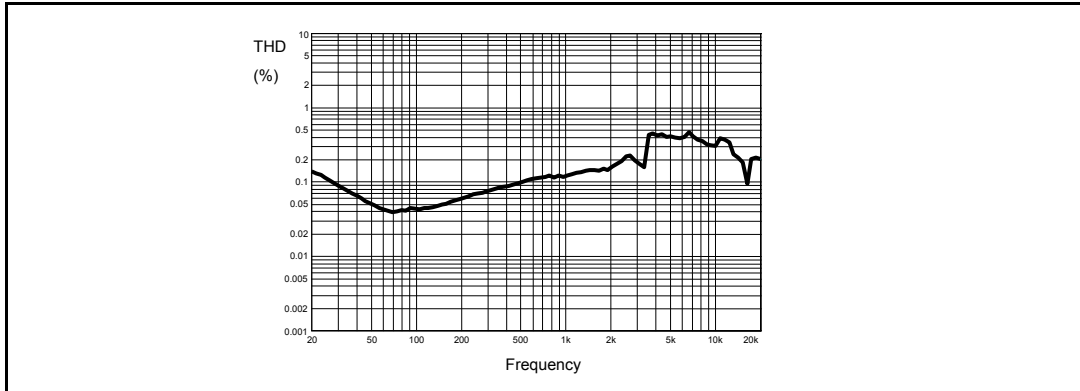


Figure 19. Output frequency response at 1 W

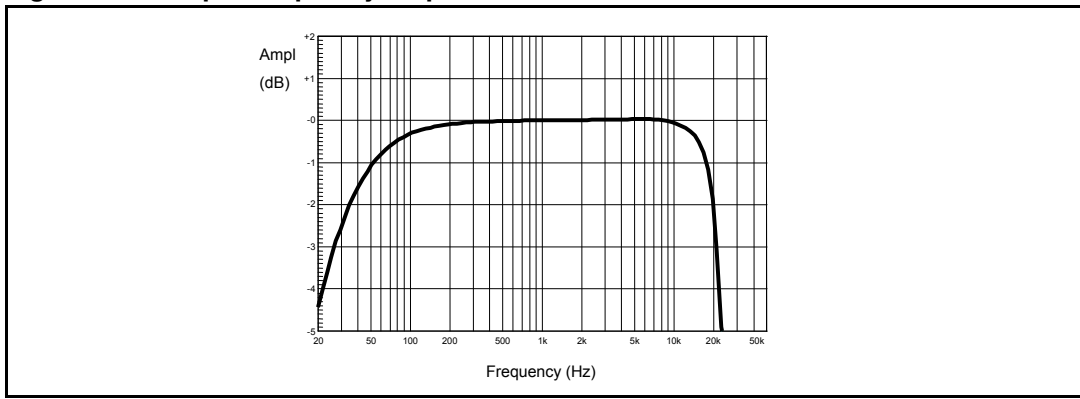


Figure 20. Crosstalk vs frequency at 1 W

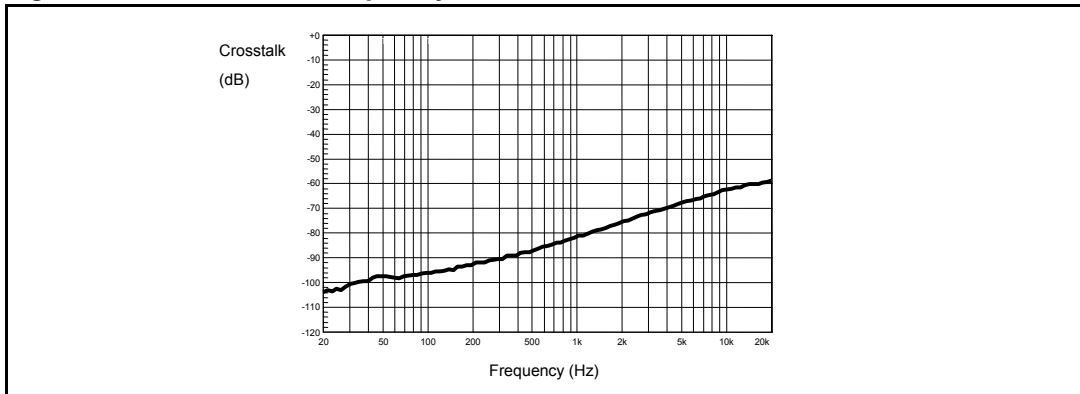


Figure 21. FFT (0 dB)

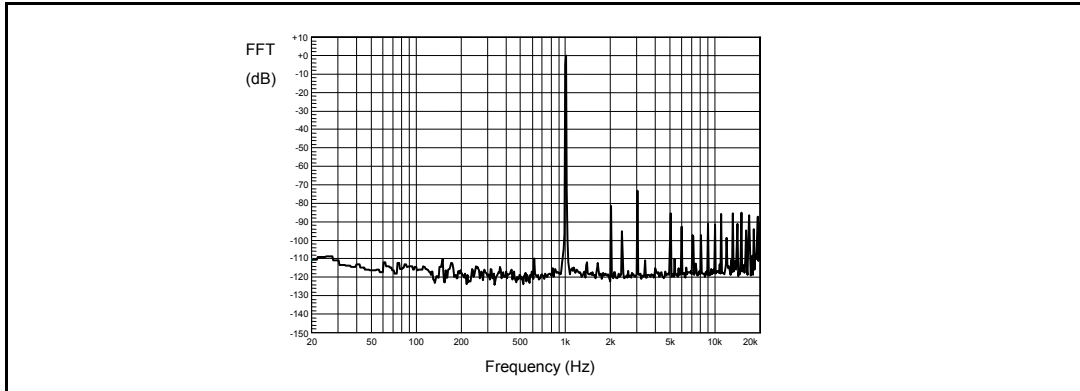
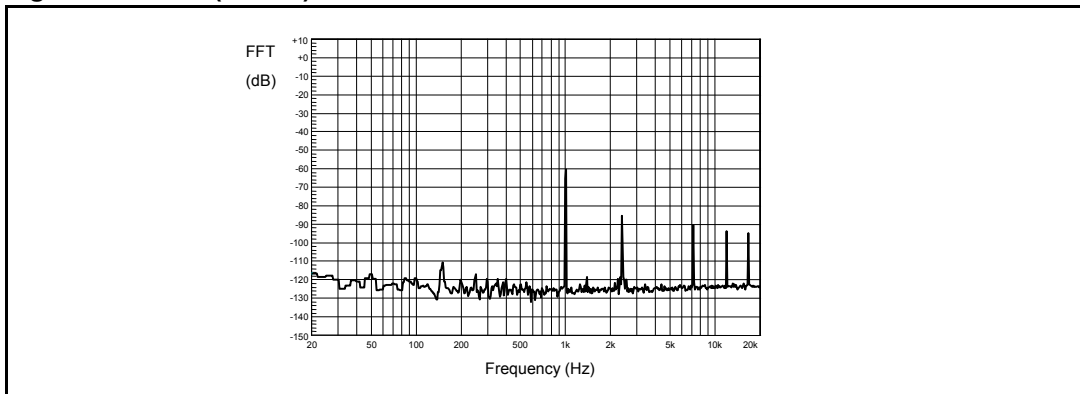


Figure 22. FFT (-60 dB)



6.2 For the configuration without filter

- Test setup as given in [Figure 7 on page 14](#)
- Test conditions $V_{CC} = 5\text{ V}$, $C_{20} = 10\ \mu\text{F}$, $R_L = 4\ \Omega + 270\ \mu\text{H}$, no LC filter

Figure 23. THD vs output power at 1 kHz

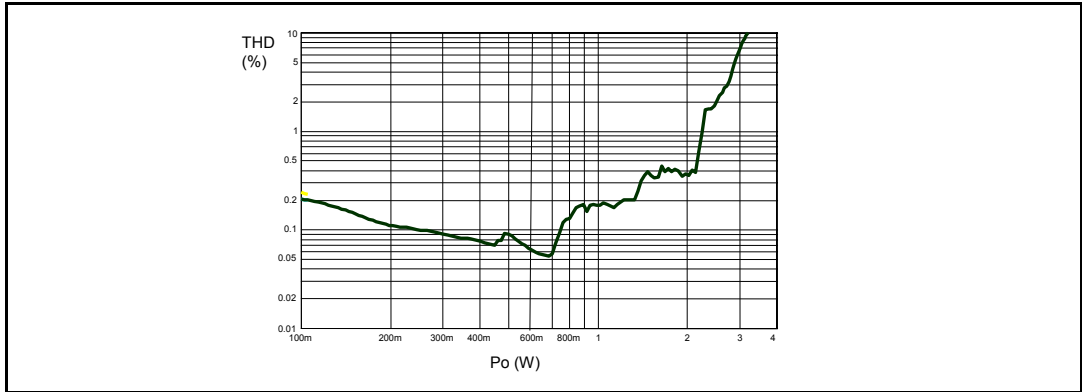


Figure 24. THD vs output power at 100 Hz

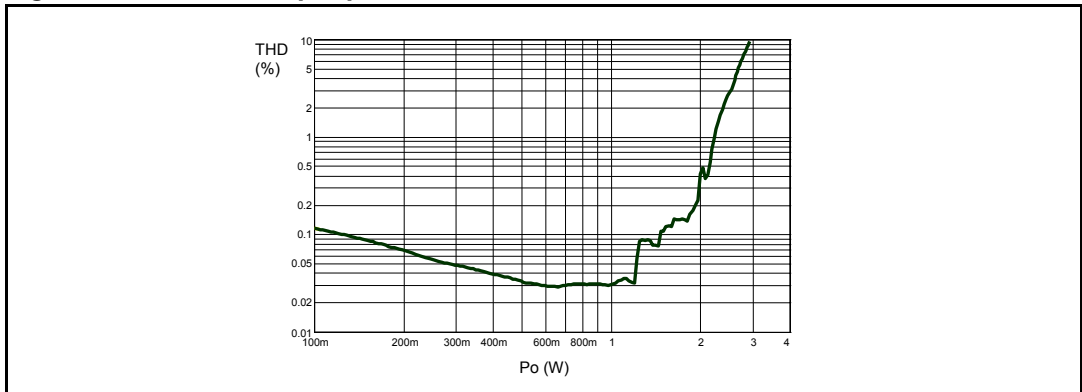


Figure 25. THD vs frequency at 100 mW

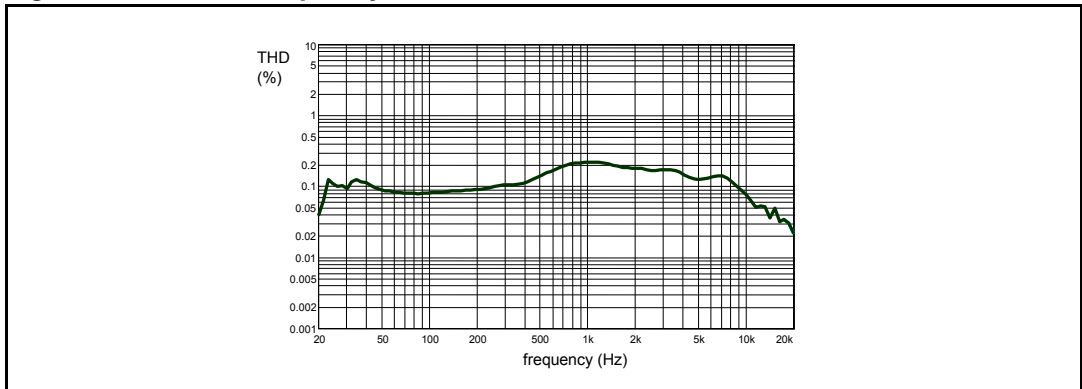


Figure 26. THD vs frequency at 1 W

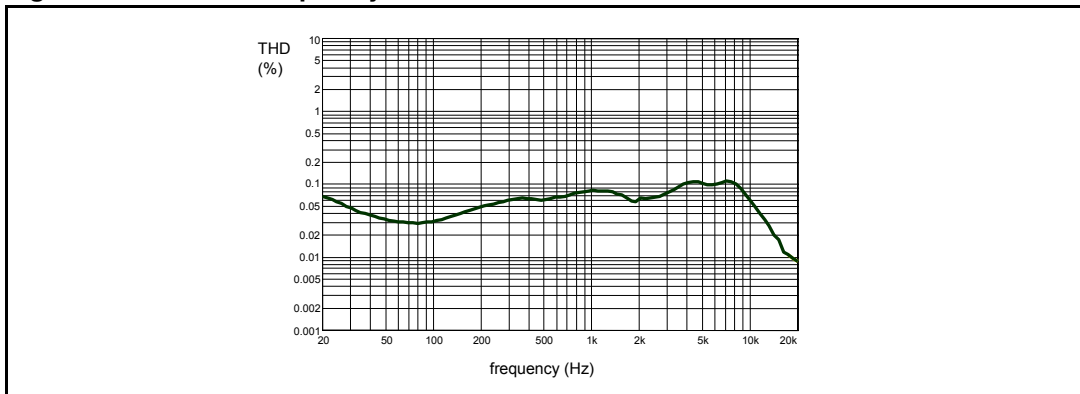


Figure 27. Frequency response at 1 W

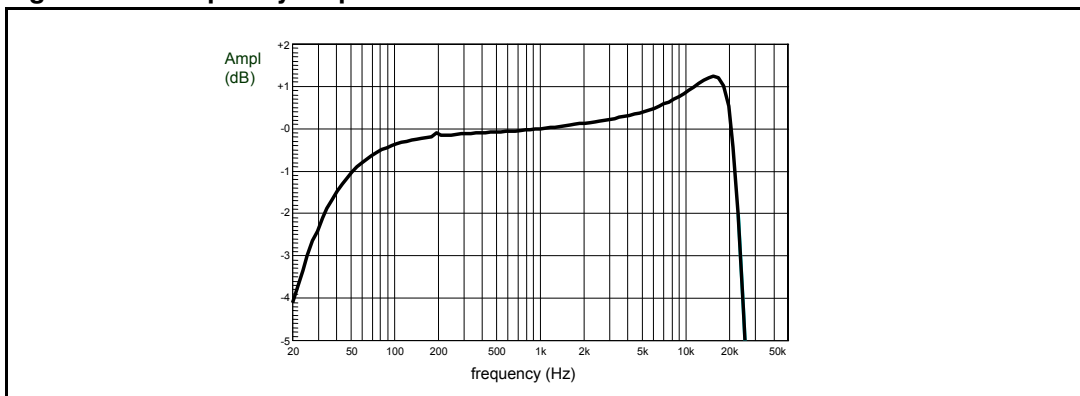


Figure 28. Crosstalk vs frequency at 1 W

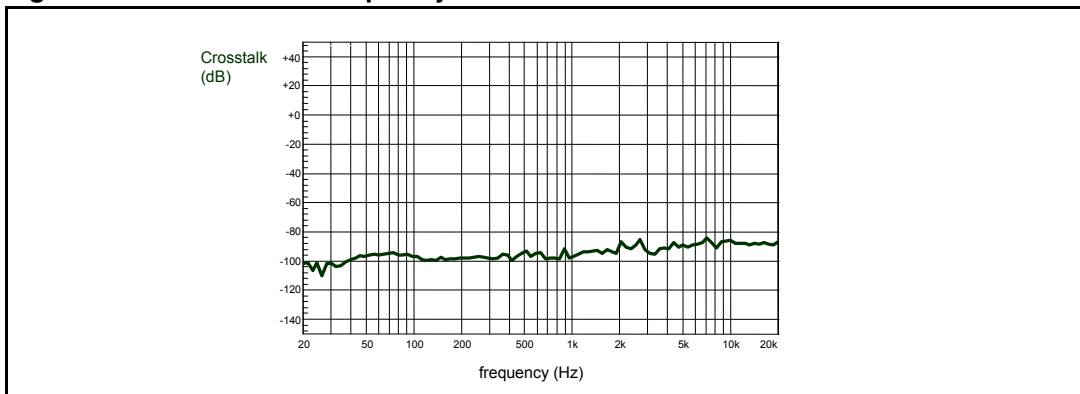


Figure 29. FFT (0 dB)

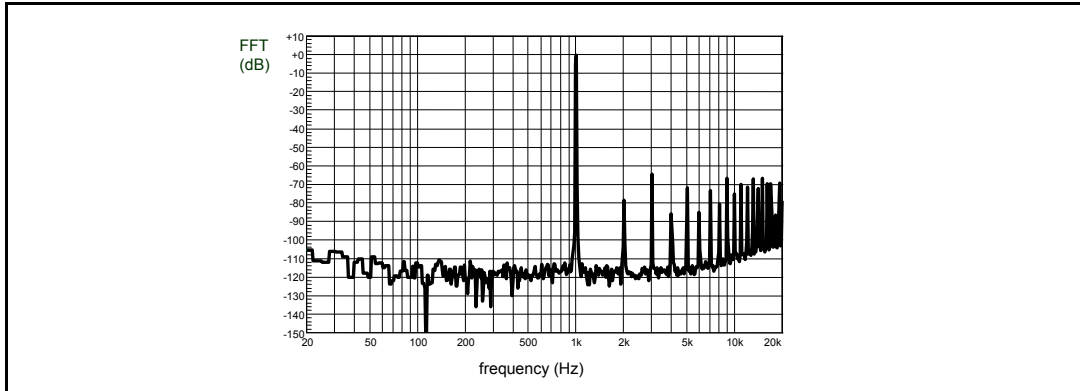
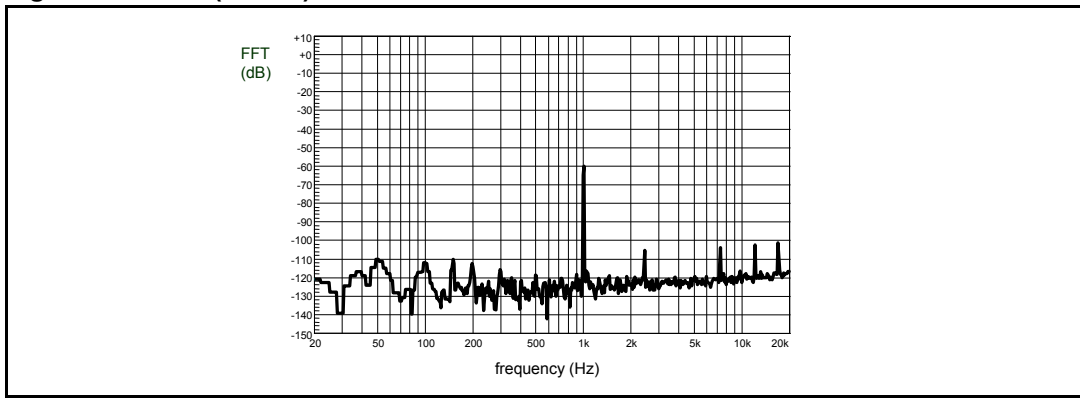


Figure 30. FFT (-60 dB)



7 Package mechanical data

The TDA7493 comes in a 24-pin HTSSOP exposed-pad-down package. The outline is shown in [Figure 31](#) and the dimensions are given in [Table 10](#).

The package code is YO and the JEDEC/EIAJ reference number is JEDEC MO-153-ADT.

Figure 31. HTSSOP24 EPD outline

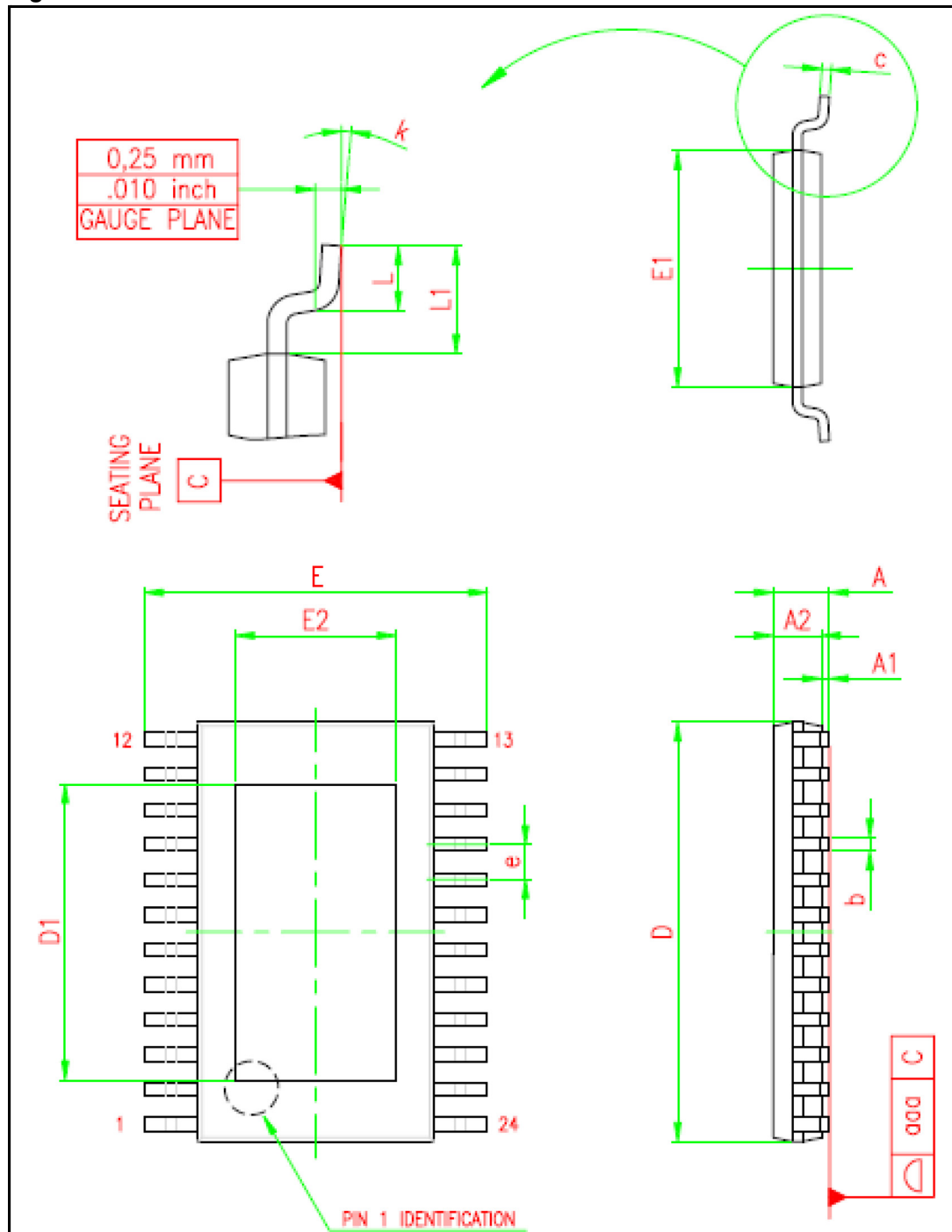


Table 10. HTSSOP24 EPD dimensions

Reference	mm			inch			Notes
	Min	Typ	Max	Min	Typ	Max	
A	-	-	1.20	-	-	0.047	-
A1	-	-	0.15	-	-	0.006	-
A2	0.80	1.00	1.05	0.031	0.039	0.041	-
b	0.19	-	0.30	0.007	-	0.012	-
c	0.09	-	0.20	0.004	-	0.008	-
D	7.70	7.80	7.90	0.303	0.307	0.311	(1)
D1	4.80	5.00	5.2	0.189	0.197	0.205	-
E	6.20	6.40	6.60	0.244	0.252	0.260	-
E1	4.30	4.40	4.50	0.169	0.173	0.177	(2)
E2	3.00	3.20	3.40	0.118	0.126	0.134	-
e	-	0.65	-	-	0.026	-	-
L	0.45	0.60	0.75	0.018	0.024	0.030	-
L1	-	1.00	-	-	0.039	-	-
aaa	-	-	0.10	-	-	0.004	-
k	0	-	8	0	-	8	degrees

1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm (0.006 inch) per side.

2. Dimension E1 does not include interlead flash or protrusions. Interlead flash or protrusions does not exceed 0.25mm (0.010 inch) per side.

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

8 Heatsink provision

With the exposed-pad packages, it is possible to use the printed circuit board as a heatsink. Using a PCB copper ground area of $3 \times 3 \text{ cm}^2$ with 16 via holes to make contact with the exposed pad, a thermal resistance of $37 \text{ }^\circ\text{C/W}$ can be achieved.

The amount of power dissipated within the device depends primarily on the supply voltage, load impedance and output modulation level. The maximum estimated power dissipation for the TDA7493 is around 1.1 W.

With the suggested copper area of 9 cm^2 , a maximum junction temperature increase of less than $40 \text{ }^\circ\text{C}$ above ambient can be expected, thus giving a maximum junction temperature, T_j , of approximately $90 \text{ }^\circ\text{C}$ in consumer environments where $50 \text{ }^\circ\text{C}$ is specified as the maximum ambient temperature. This provides a comfortable safety margin to the thermal protection threshold at $T_j = 150 \text{ }^\circ\text{C}$.

9 Revision history

Table 11. Document revision history

Date	Revision	Changes
02-Apr-2008	1	Initial release.
16-Sep-2008	2	Updated application schematic on page 8 Updated Table 5: Electrical characteristics on page 9 Updated schematic of input structure on page 12 Updated Schematic for the filterless configuration on page 14 Updated section 5.8: Differential input on page 17 .
01-Dec-2008	3	Added test voltage note to SC protection in section 5.7: Protection function on page 17 .
14-Dec-2008	4	Replaced 2.8 W with 3 W in title on page 1 Added new feature of 3.0 W on on page 1 Updated description for pin STANDBY in Table 2: Pin list on page 7 Added output power for filterless config to Table 5: Electrical characteristics on page 9 Updated values for digital input thresholds in Table 5: Electrical characteristics on page 9 Updated text for environmentally-friendly packaging on page 27 .
14-Oct-2009	5	Updated minimum operating voltage on page 1 and on page 9 Updated formula for f_{SW} on page 10 and on page 15 .

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