TH8056

Enhanced Single Wire CAN Transceiver

Features

- Fully compliant to GMW3089 V2.4 and J2411 Single Wire CAN specification for Class B in-vehicle communications
- Only 60 µA worst case sleep mode current independent from CAN voltage range
- Operating voltage range 5V to 26.5V
- Up to 40 kbps bus speed
- Up to 100 kbps high-speed transmission mode
- Logic inputs compatible with 3.3V and 5V supply systems
- Control pin for external voltage regulators
- Low RFI due to output wave shaping in normal and high voltage wake up mode
- Fully integrated receiver filter
- Bus terminals proof against short-circuits and transients in automotive environment
- Loss of ground protection, very low leakage current (typ. 20µA at 26.5V and 125°C)
- Protection against load dump, jump start
- Thermal overload and short circuit protection
- Under voltage lockout
- Bus dominant time-out feature
- Pb-Free 14-pin thermally enhanced and 8-pin SOIC package

Ordering Information

Part No.	*Temperature Range*	*Package*	*Revision*
TH8056 KDC A	-40 to 125 °C	SOIC14	A
TH8056 KDC A8	-40 to 125 °C	SOIC8	A

General Description

The TH8056 is a physical layer device for a single wire data link capable of operating with various CSMA/CR protocols such as the Bosch Controller Area Network (CAN) version 2.0. This serial data link network is intended for use in applications where a high data rate is not required and a lower data rate can achieve cost reductions in both the physical media components and the microprocessor and/or dedicated logic devices that use the network.

The network shall be able to operate in either the normal data rate mode or the high-speed data download mode for assembly line and service data transfer operations. The high-speed mode is only intended to be operational when the bus is attached to an off-board service node. This node shall provide temporary bus electrical loads which facilitate higher speed operation.

The bit rate for normal communications is typically 33.33kbit/s, for high-speed transmissions as described above a typical bit rate of 83.33kbit/s is recommended. The TH8056 is designed in accordance with the Single Wire CAN Physical Layer Specification GMW3089 V2.4 and supports many additional features like under-voltage lock-out, time-out for faulty blocked input signals, output blanking time in case of bus ringing and a very low sleep mode current.

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1. Functional Diagram

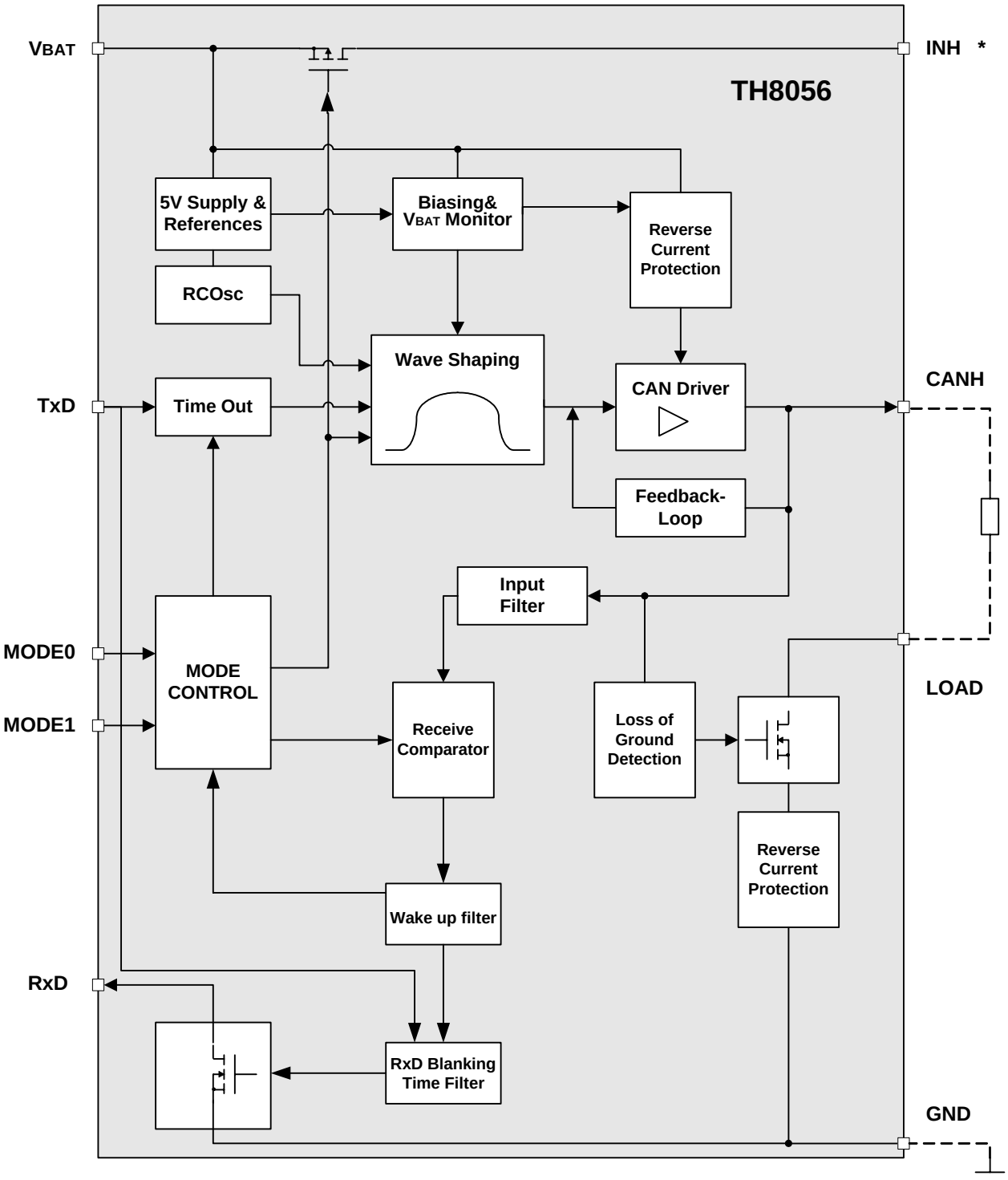


Figure 1 - Block Diagram

* INH terminal is present on TH8056 KDC A only

2. Electrical Specification

All voltages are referenced to ground (GND). Positive currents flow into the IC.
The absolute maximum ratings (in accordance with IEC 134) given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device.

2.1 Operating Conditions

Parameter	Symbol	Min	Max	Unit
Battery voltage	V_{BAT}	5.0	18	V
Operating ambient temperature for TH8056 KDC A	T_A	-40	125	°C
Junction temperature	T_J	-40	150	°C

2.2 Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
Supply Voltage	V_{BAT}		-0.3	18	V
Short-term supply voltage	$V_{BAT.ld}$	Load dump; t<500ms		40	V
		Jump start; t<1min		26.5	
Transient supply voltage	$V_{BAT.tr1}$	ISO 7637/1 pulse 1[1]	-50		V
Transient supply voltage	$V_{BAT..tr2}$	ISO 7637/1 pulses 2[1]		100	V
Transient supply voltage	$V_{BAT..tr3}$	ISO 7637/1 pulses 3A, 3B	-200	200	V
CANH voltage	V_{CANH}	V_{BAT} <= 26.5V	-20	40	V
		V_{BAT} = 0	-40	40	
Transient bus voltage	$V_{CANH..tr1}$	ISO 7637/1 pulse 1 [2]	-50		V
Transient bus voltage	$V_{CANH.tr2}$	ISO 7637/1 pulses 2 [2]		100	V
Transient bus voltage	$V_{CANH.tr3}$	ISO 7637/1 pulses 3A, 3B [2]	-200	200	V
DC voltage on pin LOAD	V_{LOAD}	via R_T > 2kΩ	-40	40	V
DC voltage on pins TxD, MODE1, MODE0,RxD,	V_{DC}		-0.3	7	V
ESD capability of any pin (Human Body Model)	ESD_{HBM}	Human body model, equivalent to discharge 100pF with 1.5kΩ,	-2	2	kV
Maximum latch – up free current at any Pin	I_{LATCH}		-500	500	mA
Thermal impedance [3]	Θ_{JA}	in free air, SOIC14		70	K/W
		in free air, SOIC8		150	
Storage temperature	T_{stg}		-55	150	°C
Junction temperature	T_{vj}		-40	150	°C

[1] ISO 7637 test pulses are applied to VBAT via a reverse polarity diode and >1uF blocking capacitor .
[2] ISO 7637 test pulses are applied to CANH via a coupling capacitance of 1 nF.
[3] The application board shall be realized with a ground copper foil area >150mm2 (low conductance board in accordance to JEDEC51-7)

2.3 Static Characteristics

Unless otherwise specified all values in the following tables are valid for V_{BAT} = 5V to 26.5V and T_{AMB}=-40°C to 125°C. All voltages are referenced to ground (GND), positive currents flow into the IC.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
PIN VBAT						
Operating supply voltage	V_{BAT}		6	12	18	V
Low battery operating supply voltage	V_{BAT_L}	except high-speed/sleep mode	5		6	V
Short duration Operating supply voltage	V_{BAT_JS}	T<1min, T_{amb} < 85°C (except high-speed mode)	18		26.5	V
Under-voltage lock-out	V_{BATuv}		4.0		4.8	V
Supply current, recessive, all active modes	I_{BAT}	V_{BAT} = 18V , TxD open		5	8	mA
Normal mode supply current, dominant	I_{BATN} [2]	V_{BAT} = 26.5V MODE0=MODE1=H TxD=L, R_{load} = 200Ω		30	35	mA
High-speed mode supply current, dominant	I_{BATH} [2]	V_{BAT} = 16V MODE0=H,MODE1=L,TxD=L, R_{load} = 75Ω		60	75	mA
Wake-up mode supply current, dominant	I_{BATW} [2]	V_{BAT} = 26.5V MODE0=L,MODE1=H, TxD=L, R_{load} = 200Ω		60	75	mA
Sleep mode supply current	I_{BATS}	V_{BAT} =13V, T_{amb} < 85°C		40	60	µA
PIN CANH						
Bus output voltage, low battery	V_{oh_l}	R_L > 200Ω, Normal, high-speed mode, 5V < V_{BAT} < 6V	3.4		5.1	V
Bus output voltage	V_{oh}	R_L > 200Ω, Normal mode, 6V < V_{BAT} < 26.5V	4.4		5.1	V
Bus output voltage, high-speed mode	V_{oh}	R_L > 75Ω, high-speed mode, 8V < V_{BAT} < 16V	4.2		5.1	V
Fixed Wake-up Output High Voltage	$V_{ohWuFix}$	Wake-up mode, R_L > 200Ω, 11.2V < V_{BAT} < 26.5V	9.9		12.5	V
Offset Wake-up Output High Voltage	$V_{ohWuOffset}$	Wake-up mode, R_L > 200Ω, 5V < V_{BAT} < 11.2V	V_{BAT} – 1.5		V_{BAT}	V
Recessive state output voltage	V_{ol}	Recessive state or sleep mode, R_{load} = 6.5 kΩ,	-0.2		0.20	V
Bus short circuit current	$-I_{CAN\_SHORT}$	V_{CANH} = 0V, V_{BAT} = 26.5V, TxD = 0V	50		350	mA
Bus leakage current during loss of ground	I_{LKN_CAN}[1]	Loss of ground, V_{CANH} = 0V	-50		10	µA
Bus leakage current, bus positive	I_{LKP_CAN}	TxD high;	-10		10	µA
Bus input threshold	V_{ih}	Normal, high-speed mode	2.0	2.1	2.2	V
Bus input threshold low battery	V_{ihlb}	Normal mode 5V<V_{BAT}<6V	1.6	1.7	2.2	V
Fixed Wake-up Input High Voltage Threshold	$V_{ihWuFix}$[2]	Sleep mode, V_{BAT} > 11.2V	6.6		7.9	V
Offset Wake-up Input High Voltage Threshold	$V_{ihWuOffset}$[2]	Sleep mode	V_{BAT}-4.3		V_{BAT}-3.25	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
PIN LOAD						
Voltage on switched ground pin	V_{LOAD}	I_{LOAD} = 1mA, all active modes and sleep mode			0.1	V
Voltage on switched ground pin	V_{LOAD_LOB}	I_{LOAD} = 7mA , V_{BAT} = 0V			1	V
Load resistance during loss of battery	R_{LOAD_LOB}	V_{BAT} = 0	R_{LOAD} -10%		R_{LOAD} +35%	Ω
PIN TXD,MODE0,MODE1						
High level input voltage	V_{ih}		2.0			V
Low level input voltage	V_{il}				0.65	V
TxD pull-up current	$-I_{IL\_TXD}$	TxD = L, MODE0 and 1 = H	20		50	µA
MODE pull-down resistor	R_{MODE_pd}		20		50	kΩ
PIN RXD						
Low level output voltage	V_{ol_rxd}	I_{RxD} = 2mA			0.4	V
High level output leakage	I_{ih_rxd}	V_{RxD} = 5V	-10		10	µA
RxD output current	I_{rxd}	V_{RxD} = 5V			70	mA
PIN INH						
High level output voltage	V_{oh_INH}	I_{INH} = -180µA	V_S -0.8V	V_S-0.5V		V
Leakage current	I_{INH_lk}	Mode0/1 = L ,V_{INH} = 0V	-5		5	µA
Over-temperature Protection						
Thermal shutdown	T_{sd} [2]		155		180	°C
Thermal recovery	T_{rec} [2]		126		150	°C

[1] Leakage current in case of loss of ground is the sum of both currents I_{LKN_CAN} and I_{LKN_LOAD} .
[2] Thresholds are not tested in production, but characterized and guaranteed by design

2.4 Dynamic Characteristics

Unless otherwise specified all values in the following table are valid for V_{BAT} = 5V to 26.5V and T_{AMB}= -40°C to 125°C.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Transmit delay in normal and wake-up mode, rising edge	t_{Tr} [1]	min and max loads acc. To 2.5 Bus loading requirements	2		6.3	µs
Transmit delay in wake-up mode to V_{ihWU}, rising edge	t_{TWUr} [2]	min and max loads acc. To 2.5 Bus loading requirements	3		18	µs
Transmit delay in normal mode, falling edge	t_{Tf} [3]	min and max loads acc. To 2.5 Bus loading requirements	1.8		10	µs
Transmit delay in wake-up mode, falling edge	t_{TWU1f} [3]	min and max loads acc. To 2.5 Bus loading requirements	3		13.7	µs
Transmit delay in high-speed mode, rising edge	t_{THSr} [4]	min and max loads acc. To 2.5 Bus loading requirements	0.1		1.5	µs
Transmit delay in high-speed mode, falling edge	t_{THSf}[5]	min and max loads acc. To 2.5 Bus loading requirements	0.04		3	µs
Receive delay , all active modes	t_{DR} [6]	CANH high to low transition	0.2		1	µs
Receive delay , all active modes	t_{RD} [6]	CANH low to high transition	0.2		1	µs
Input minimum pulse length, all active modes	t_{mpDR} [6]	CANH high to low transition	0.1		1	µs
Input minimum pulse length, all active modes	t_{mpRD} [6]	CANH low to high transition	0.1		1	µs
Wake-up filter time delay	t_{WUF}	See diagrams, Figure 3	10		70	µs
Receive blanking time after TxD L-H transition	t_{rb}	See diagrams, Figure 4	0.5		6	µs
TxD time-out reaction time	t_{tout}	All active modes	10		30	ms
Delay from Normal to High-speed/HVWU Mode	t_{dnhs}				30	ms
Delay from High-speed /HVWU to Normal Mode	t_{dhsn}				30	ms
Delay from Normal Mode to Standby	t_{dsby}	V_{BAT} = 6V to 26.5V			500	µs
Delay from Standby to Sleep Mode	t_{dsleep}	V_{BAT} = 6V to 26.5V	100		500	ms
Delay from Sleep to normal Mode	t_{dsnwu}	V_{BAT} = 6V to 26.5V			50	ms

[1] The maximum signal delay time for a bus rising edge is measured from $V_{cmos\ il}$ on the TxD input pin to the V_{ihMax} + $V_{g\ off}$ max level on CANH at maximum network time constant , minimum signal delay time for a bus rising edge is measured from $V_{cmos\ ih}$ on the TxD input pin to 1V on CANH at minimum network time constant .These definitions are valid in both normal and HVWU mode

[2] The maximum signal delay time for a bus rising edge in HVWU mode is measured from $V_{cmos\ il}$ on the TxD input pin to the $V_{ihWUMax}$ + $V_{g\ off}$ max level on CANH at maximum network time constant, minimum signal delay time for a bus rising edge is measured from $V_{cmos\ ih}$ on the TxD input pin to 1V on CANH at minimum network time constant

[3] Maximum signal delay time for a bus falling edge is measured from $V_{cmos\ ih}$ on the TxD input pin to 1V on CANH at maximum network time constant, minimum signal delay time for a bus falling edge is measured from $V_{cmos\ ih}$ on the TxD input pin to the V_{ihMax} + $V_{g\ off}$ max level on CANH. These definitions are valid in both normal and HVWU mode.

[4] The signal delay time in high-speed mode for a bus rising edge is measured from $V_{cmos\ il}$ on the TxD input pin to the V_{ihMax} + $V_{g\ off}$ max level on CANH at maximum high-speed network time constant.

[5] The signal delay time in high-speed mode for a bus falling edge is measured from $V_{cmos\ ih}$ on the TxD input pin to 1V on CANH at maximum high-speed network time constant

[6] Receive delay time is measured from the rising / falling edge crossing of the nominal Vih value on CANH to the falling (Vcmos_il_max) / rising (Vcmos_ih_min) edge of RxD. This parameter is tested by applying a square wave signal to CANH. The minimum slew rate for the bus rising and falling edges is 50V/us. The low level on bus is always 0V. For normal mode and high-speed mode testing the high level on bus is 4V. For HVWU mode testing the high level on bus is Vbat – 2V.

2.5 Bus loading requirements

Parameter	Symbol	Min	Typ	Max	Unit
Number of system nodes		2		32	
Network distance between any two ECU nodes	Bus length			60	M
Node Series Inductor Resistance (if required)	R_{ind}			3.5	Ohm
Ground Offset Voltage	V_{goff}			1.3	V
Ground Offset Voltage, low battery	V_{gofflb}		0.1 V_{BAT}	0.6	V
Device Capacitance (unit load)	C_{ul}	135	150	300	pF
Network Total Capacitance	C_{tl}	396		19000	pF
Device Resistance (unit load)	R_{ul}	6435	6490	6665	Ohm
Device Resistance (min load)	R_{min}	2000			Ohm
Network Total Resistance	R_{tl}	200		3332	Ohm
High-Speed Mode Network Resistance to GND	R_{load}	75		135	Ohm
Network Time Constant [1]	τ	1		4	µs
Network Time Constant, high-speed mode [1]	τ			1.5	µs

[1] The network time constant incorporates the bus wiring capacitance. The minimum value is selected to limit radiated emissions. The maximum value is selected to ensure proper communication under all communication modes. Not all combinations of R and C are possible. The following load conditions are used for the measurement of the dynamic characteristics:

Normal and high volt. Wake-up mode		High-speed mode
min.load/min tau	3.3KΩ/ 540pF	Additional 140Ω tool resistance to ground in parallel
min.load/max tau	3.3KΩ/ 1.2nF	
max.load/min tau	200Ω/ 5nF	Additional 120Ω tool resistance to ground in parallel
max.load/max tau	200Ω/ 20nF	

2.6 Timing Diagrams

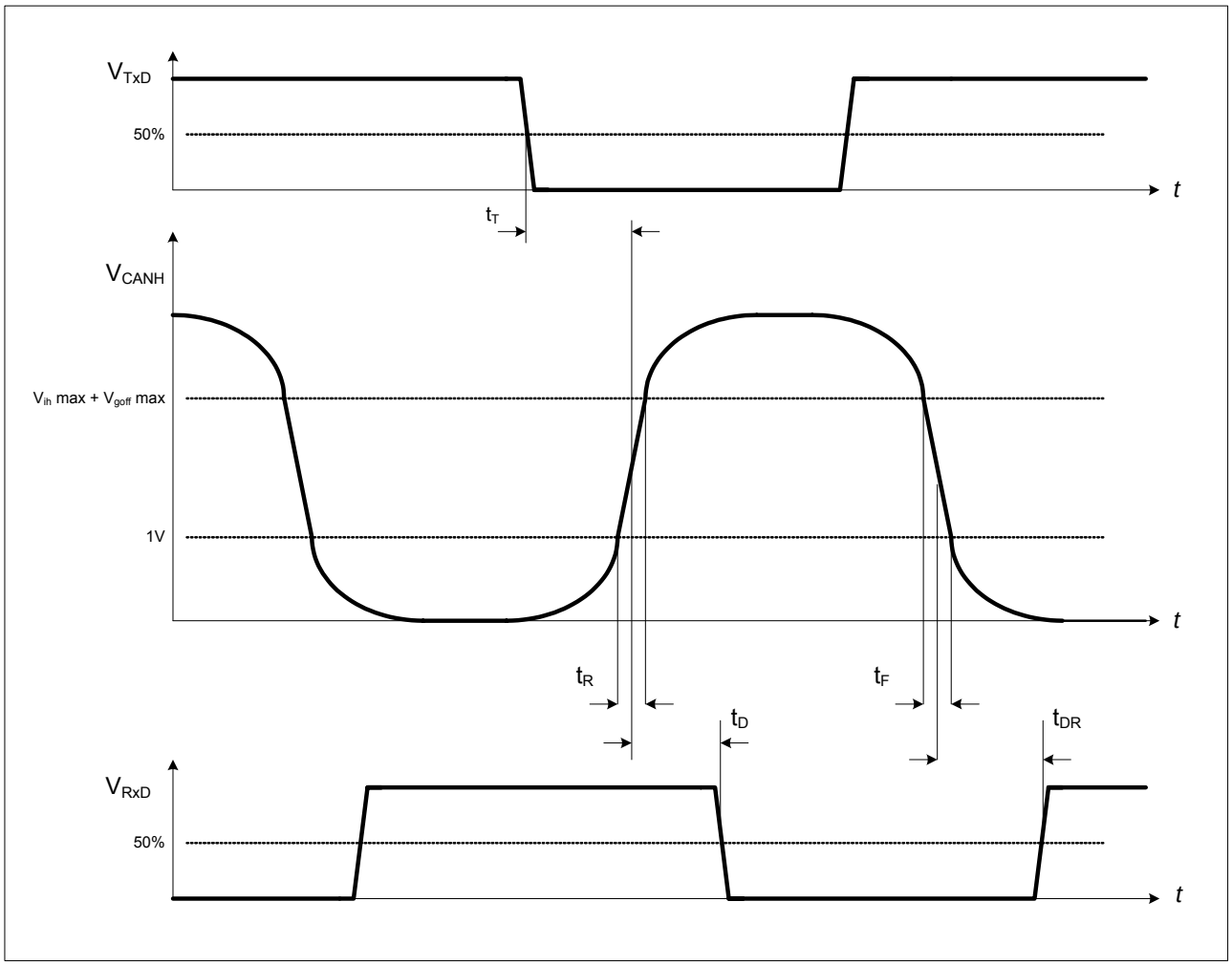


Figure 2 – Input / Output Timing

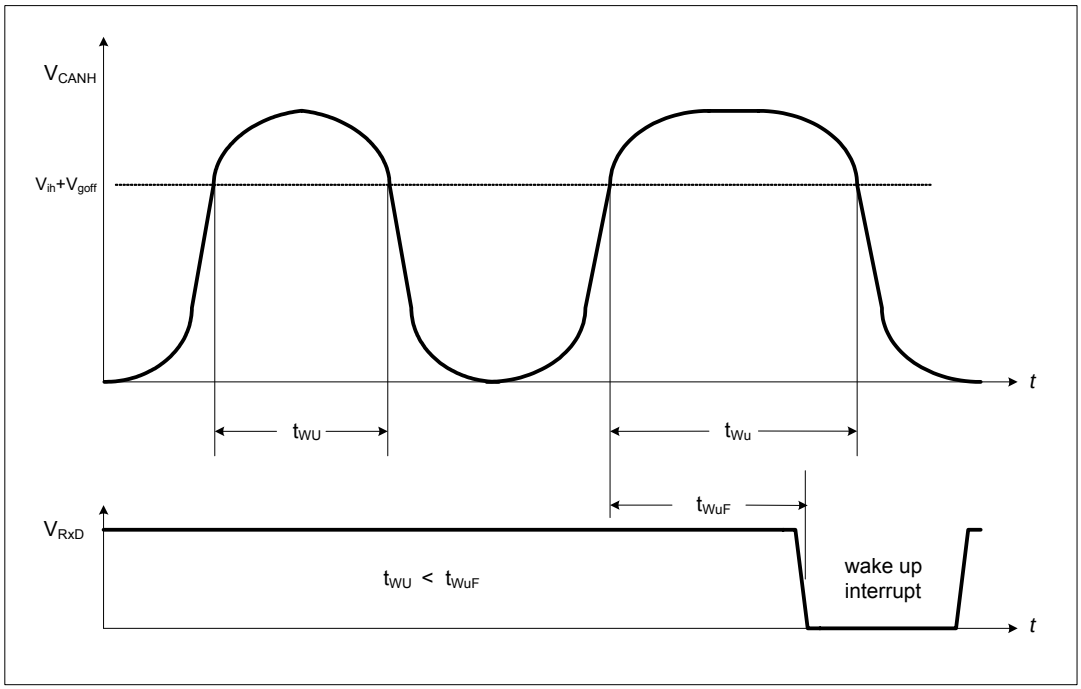


Figure 3 – Wake-up Filter Time Delay

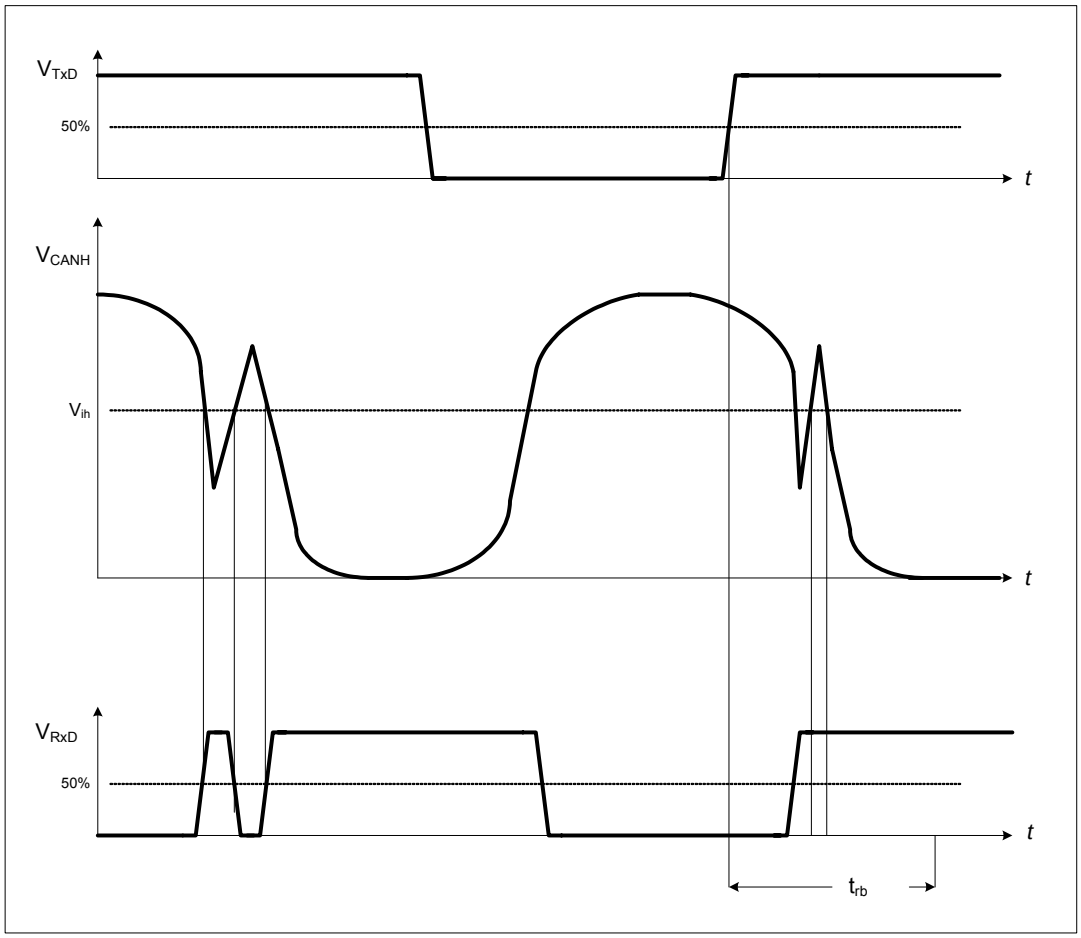


Figure 4 – Receive Blanking Time

3. Functional Description

3.1 TxD Input pin

Logic command to transmit on the single wire CAN bus

TxD Polarity

- TxD = logic 1 (or floating) on this pin produces an undriven or recessive bus state (low bus voltage)
- TxD = logic 0 on this pin produces either a bus normal or a bus high-voltage dominant state depending on the transceiver mode state (high bus voltage)

If the TxD pin is driven to a logic low state while Mode 0,1 pins are in the 0,0 or sleep state, the transceiver cannot drive the CAN Bus pin to the dominant state.
The transceiver provides an internal pull up on the TxD pin, which will cause the transmitter to default to the bus recessive state, when TxD is not driven.
TxD input signals are standard CMOS logic levels for 3.3V and 5V supply voltages.

Time-out feature

In case of a faulty blocked dominant TxD input signal the CANH output is switched off automatically after the specified TxD time-out reaction time to prevent a dominant bus. The transmission is continued by next TxD L to H transition without delay.

3.2 Mode 0 and Mode 1 pins

Select transceiver operating modes

The transceiver provides a weak internal pull-down current on each of these pins, which causes the transceiver to default to sleep mode when they are not driven. The Mode input signals are standard CMOS logic level for 3.3V and 5V supply voltages.

M0	M1	Mode
L	L	Sleep Mode
H	L	High-Speed
L	H	High-Voltage Wake-Up
H	H	Normal Mode

Figure 5 – Truth Table

Mode 0 = 0, Mode 1 = 0 – Sleep mode
Transceiver is in low-power state, waiting for wake-up via high-voltage signal or by mode pins change to any state other than 0,0. In this state, the CAN Bus pin is not in the dominant state regardless of the state of the TxD pin.

Mode 0 = 1, Mode 1 = 0 – High-Speed mode
This mode allows high-speed download with bitrates up to 100Kbit/s. The output waveshaping circuit is disabled in this mode. Bus transmitters which require communicating in high-speed mode are able to drive reduced bus resistance during this mode.

Note: High-speed mode is only allowed with connected tool resistance in parallel to the network load. Otherwise the stability of the output signal is not guaranteed because of the slew rate enhancement for the required rise times .

Mode 0 = 0, Mode 1 = 1 – Transmit with high voltage signals to wake up remote nodes (HVWU)
This bus includes a selective node awake capability, which allows normal communication to take place among some nodes while leaving the other nodes in an undisturbed sleep state. This is accomplished by controlling the signal voltages such that all nodes must wake up when they receive a higher voltage message signal waveform. The communication system communicates to the nodes information as to which nodes are to stay operational (awake) and which nodes are to put themselves into a non-communicating low-power "sleep" state. Communication at the lower, normal voltage levels does not disturb the sleeping nodes.

Mode 0 = 1, Mode 1 = 1 – Normal speed and signal voltage mode
Transmission bit rate in normal communication is 33.333 Kbits/sec. In normal transmission mode the TH8056 supports controlled waveform rise and overshoot times. Waveform trailing edge control is required to assure that high frequency components are minimized at the beginning of the downward voltage slope. The remaining fall time occurs after the bus is inactive with drivers off and is determined by the RC time constant of the total bus load.

3.3 RxD Output pin

Logic data as sensed on the single wire CAN bus

RxD polarity

RxD = logic 1 on this pin indicates a bus recessive state (low bus voltage)
RxD = logic 0 on this pin indicates a bus normal or high-voltage bus dominant state

RxD in Sleep Mode

RxD does not pass signals to the micro processor while in sleep mode until a valid wake-up bus voltage level is received or the Mode 0, 1 pins are not 0,0 respectively. When the valid wake-up bus signal awakens the transceiver, the RxD pin signalizes an interrupt (logic 0 for dominant high-voltage signal). If there is no mode change within the time stated, the transceiver reenters the sleep mode as described in 3.7

When not in sleep mode all valid bus signals will be sent out on the RxD pin.

RxD Typical Load

Resistance: 2.7 kohms
Capacitance: < 25 pF

3.4 Bus LOAD pin

Resistor ground with internal open-on-loss-of-ground protection

When the ECU experiences a loss of ground condition, this pin is switched to a high impedance state.

The ground connection through this pin is not interrupted in any transceiver operating mode including the sleep mode. The ground connection is interrupted only when there is a valid loss of ground condition.

This pin provides the bus load resistor with a path to ground which contributes less than 0.1 volts to the bus offset voltage when sinking the maximum current through one unit load resistor.

The transceiver's maximum bus leakage current contribution to V_{ol} from the LOAD pin when in a loss of ground state is 50 uA over all operating temperatures and 3.5 V < V_{batt} < 26.5V.

3.5 V_{bat} INPUT pin

Vehicle Battery Voltage

The transceiver is fully operational as described in chapter 2 over the range 6V<$V_{bat\ IC}$<18V as measured between the GND pin and this pin.
For 5V < $V_{bat\ IC}$ < 6V the bus operates in normal mode with reduced dominant output voltage and reduced receiver input voltage. High voltage wake-up call is not possible (dominant output voltage is the same as in normal or high-speed mode).
The transceiver operates in normal mode and high-voltage wake-up mode if 18V < $V_{bat\ IC}$ < 26.5V at 85°C for one minute.

For 0V< $V_{bat\ IC}$ < 4.8V, the bus is passive (not driven dominantly) and RxD is undriven (high), regardless of the state of the TxD pin (under-voltage lock-out).

3.6 CAN BUS pin

Bus Input/Output

Wave Shaping in normal and HVWU mode

Wave shaping is incorporated into the transmitter to minimize EMI radiated emissions. An important contributor to emissions is the rise and fall times during output transitions at the “corners” of the voltage waveform. The resultant waveform is one half of a sine wave of frequency 50 – 65 kHz at the rising waveform edge and one quarter of this sine wave at falling or trailing edge.

Short circuits

If the CAN BUS pin is shorted to ground for any duration of time, the current is limited to the specified value, until an over-temperature shut-down circuit disables the output high side drive source transistor (before the local die temperature exceeds the damage limit threshold).

Loss of ground

In case of an ECU loss of ground condition, the LOAD pin is switched into high impedance state. The CANH transmission is continued until the under-voltage lock-out voltage threshold is detected.

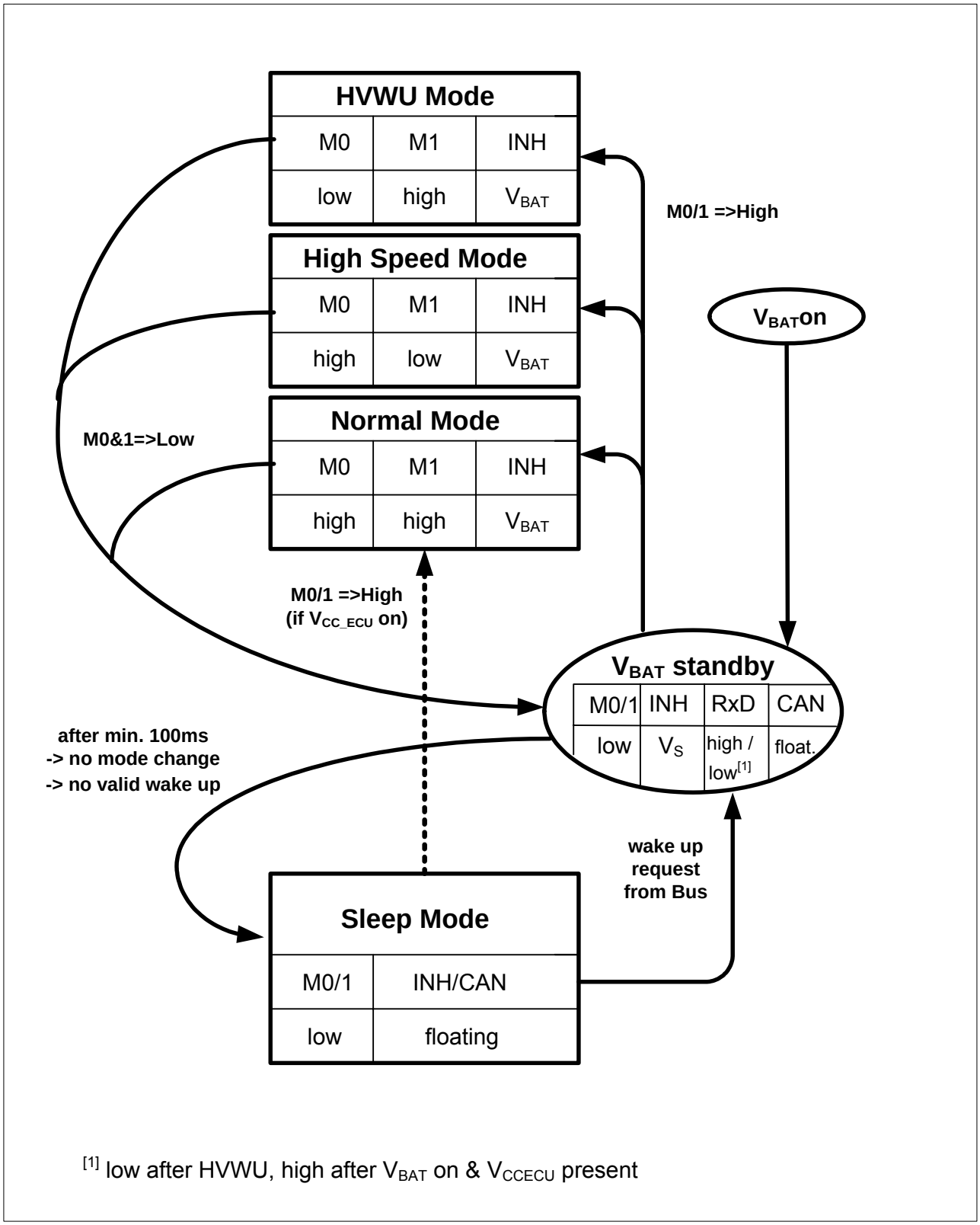
Loss of battery

In case of battery loss (VBAT = 0 or open) the transceiver does not disturb bus communication. The maximum reverse current into power supply system doesn’t exceed 500µA.

3.7 INH Pin (TH8056 KDC A only)

This Pin is a high-voltage highside switch used to control the ECU’s regulated microcontroller voltage supply. After power-on the transceiver automatically enters an intermediate standby mode, the INH output will become HIGH (VBAT) and therefore the external voltage regulator will provide the Vcc supply for the ECU . If there is no mode change within the time stated, the transceiver reenters the sleep mode and the INH output goes to logic 0 (floating). When the transceiver has detected a valid wake-up condition (bus HVWU traffic which exceeds the wake-up filter time delay) the INH output will become HIGH (VBAT) again and the same procedure starts as described after power-on. In case of a mode change into any active mode the sleep timer is stopped and INH keeps high (VBAT) level. If the transceiver enters the sleep mode (M0,1=0), INH goes to logic 0 (floating) no sooner than 100ms when no wake-up signal is present.

3.8 State Diagram



[1] low after HVWU, high after V_{BAT} on & V_{CCECU} present

Figure 6 – State Diagram

3.9 Power Dissipation

The TH8056 has an integrated protection against thermal overload. If the junction temperature reaches the thermal shutdown threshold the TH8056 disables the transmitter driver to reduce the power dissipation to protect the IC itself from thermal overload. The function of the transceiver will become again available if the junction temperate drops below the thermal recovery temperature.

To secure a stable functioning within the application and to avoid a transmitter switch off due to thermal overload under normal operating conditions, the application must take care of the maximum power dissipation of the IC. The junction temperature can be calculated with:

$$T_J = T_a + P_d * \theta_{ja}$$

T_J	Junction temperature
T_a	Ambient temperature
P_d	Dissipated power
θ_{ja}	Thermal resistance

The Junction temperature shouldn't exceed under normal operating conditions the limit specified in chapter 2.3 Static Characteristics.

The power dissipation of an IC is the major factor determining the junction temperature. The TH8056 consumes current in different functions. A part of the supply current goes to the load and the other part dissipates internally. The internal part has a constant passive part and an active part which depends on the actual bus transmission. The complete internal part causes and increasing of the junction temperature.

$$P_{tot} = P_{INT\_a} + P_{INT\_P}$$

P_{INT_a}	Internal power dissipation active
P_{INT_p}	Internal power dissipation passive
P_{tot}	Overall power dissipation
D	Duty cycle for data transmission

The internal passive part can be calculated with the operating voltage and the normal mode supply current recessive. The active part can be calculated with the voltage drop of the driving transistor and the current of the CAN bus. The active part generates only during data transmission power dissipation. Therefore the duty cycle has to be taken into account.

$$P_{INT\_p} = V_{BAT} * I_{BAT}$$
$$P_{INT\_a} = (V_{BAT} - V_{CANH}) * I_{load} * D$$

V_{BAT}	Battery supply voltage
I_{BAT}	Normal mode supply current recessive
I_{load}	Can network current
D	Duty cycle for data transmission
V_{CANH}	Voltage at CANH pin

The power dissipation of the load can be calculated with the CANH voltage and the CAN bus current.

$$P_{load} = V_{CANH} * I_{load} * D$$

where

$$I_{load} = V_{CANH} / R_{load\_net}$$

P_{load}	Power dissipation of the load resistor
I_{load}	Current of CAN network
V_{CANH}	Voltage at CANH pin
R_{load_net}	Network total resistance

Assumptions:

V_{BAT} = 26.5V
R_{load} = 6.49 kΩ
Network with 32 nodes
V_{CANH} = 5.1V
I_{BAT} = 6mA
D = 50%
T_a = 125°C
Θ_{JA} = 70k/W (Thermally enhanced SOIC14 package)

Computations:

R_{load_net} = 6.49kΩ / 32nodes = 203Ω
I_{load} = 5.1V / 203Ω = 25mA
P_{load} = 5.1V * 25mA * 0.5 = 64mW
P_{INT_a} = (26.5V – 5.1V) * 25mA * 0.5 = 267mW
P_{INT_P} = 26.5V * 6mA = 159mW
P_{tot} = 267mW + 159mW = 426mW
T_j = 125°C + 426mW * 70k/W = 155°C

The above calculation shows that under worst case conditions (max. operating voltage, max bus load, max ambient temperature) the TH8056 with the thermally enhanced SOIC14 package operates below the thermal limit. A stable functioning is possible up to these limits.

3.9.1. Thermal behaviour of TH8056 with SOIC8 – TH8056 KDC A8

The thermal impedance of an SOIC8 package is about twice in comparison to the thermally enhanced SOIC14 package. Therefore the maximum power dissipation within this package is only about the half.
The using of the SOIC8 version of TH8056 depends on the network architecture (number of nodes), the max. ambient temperature and the needed functionality (using of INH pin).
The following diagram shows the relationship between junction temperature, ambient temperature and number of nodes, which have to be taken into account for using the SOIC8 version.

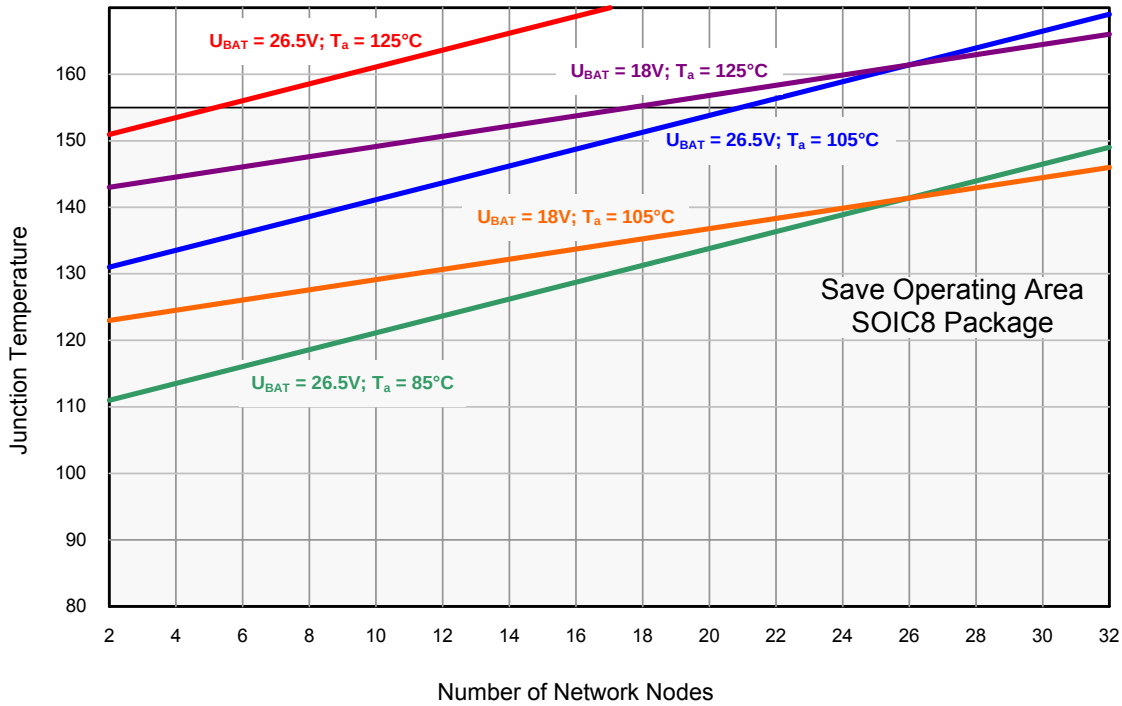


Figure 7 – Save operating area of SOIC8 package

3.10 Application Circuitry

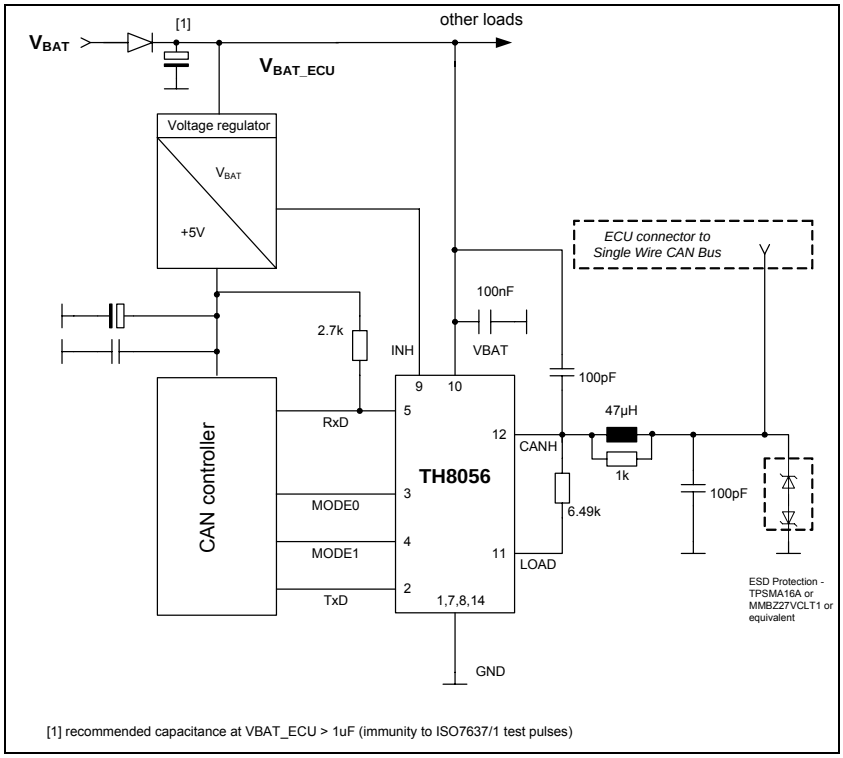


Figure 8 – Application Circuitry TH8056 KDC A

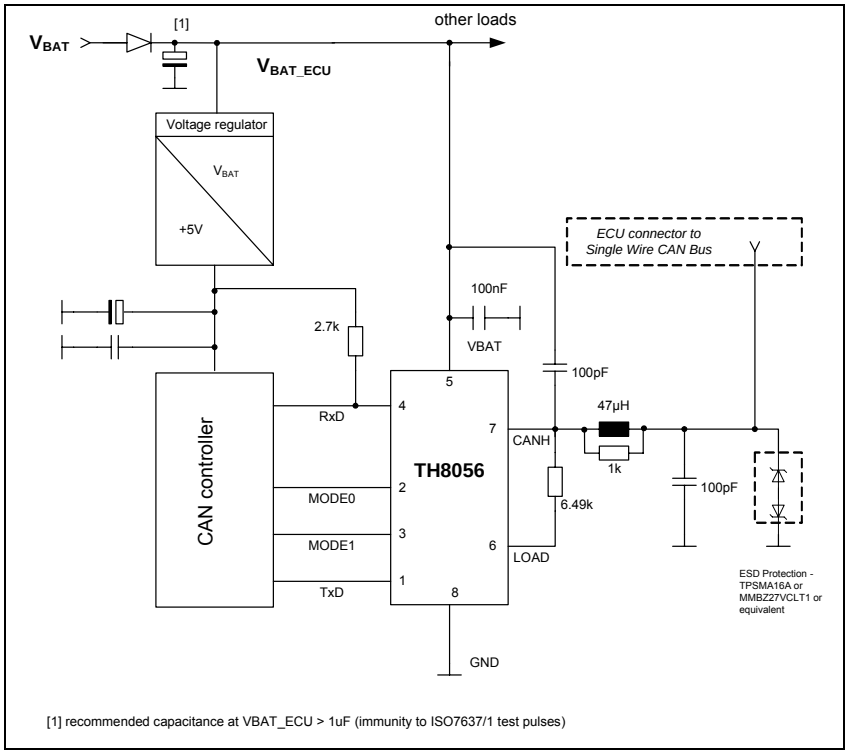
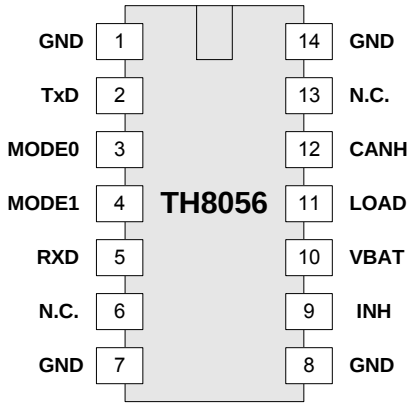


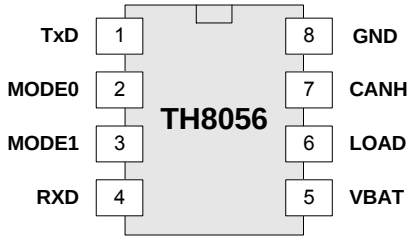
Figure 9 – Application circuitry TH8056 KDC A8

4. Pin Description

TH8056 KDC A



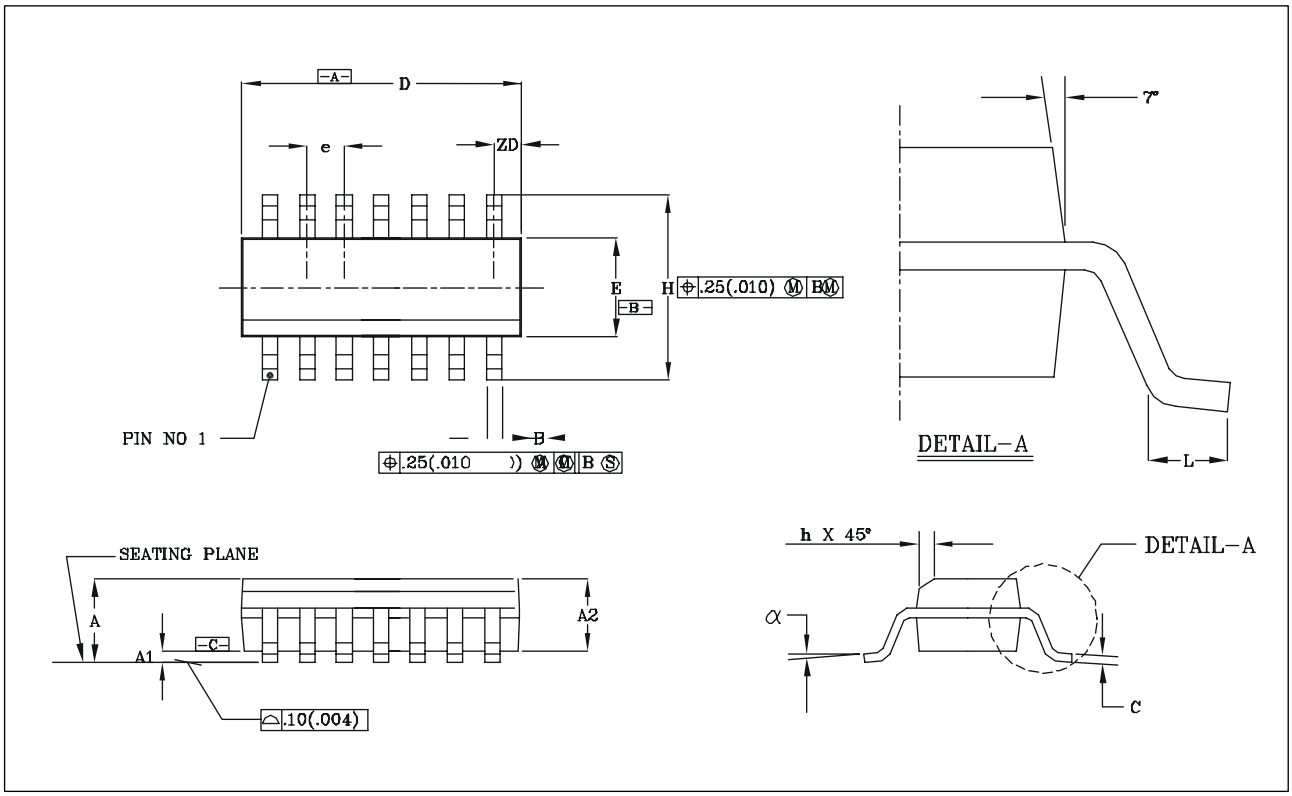
TH8056 KDC A8



Pin TH8056 KDC A	Pin TH8056 KDC A8	Name	IO-Typ	Description
1	-	GND	P	Ground
2	1	TXD	I	Transmit data from MCU to CAN
3	2	MODE0	I	Operating mode select input 0
4	3	MODE1	I	Operating mode select input 1
5	4	RXD	O	Receive data from CAN to MCU
6	-	N.C.		
7	-	GND	P	Ground
8	-	GND	P	Ground
9	-	INH	O	Control Pin for external voltage regulator (high voltage high side switch)
10	5	VBAT	P	Battery voltage
11	6	LOAD	O	Resistor load (loss of ground low side switch)
12	7	CANH	I/O	Single wire CAN bus pin
13	-	N.C.		
14	8	GND	P	Ground

5. Package Dimensions

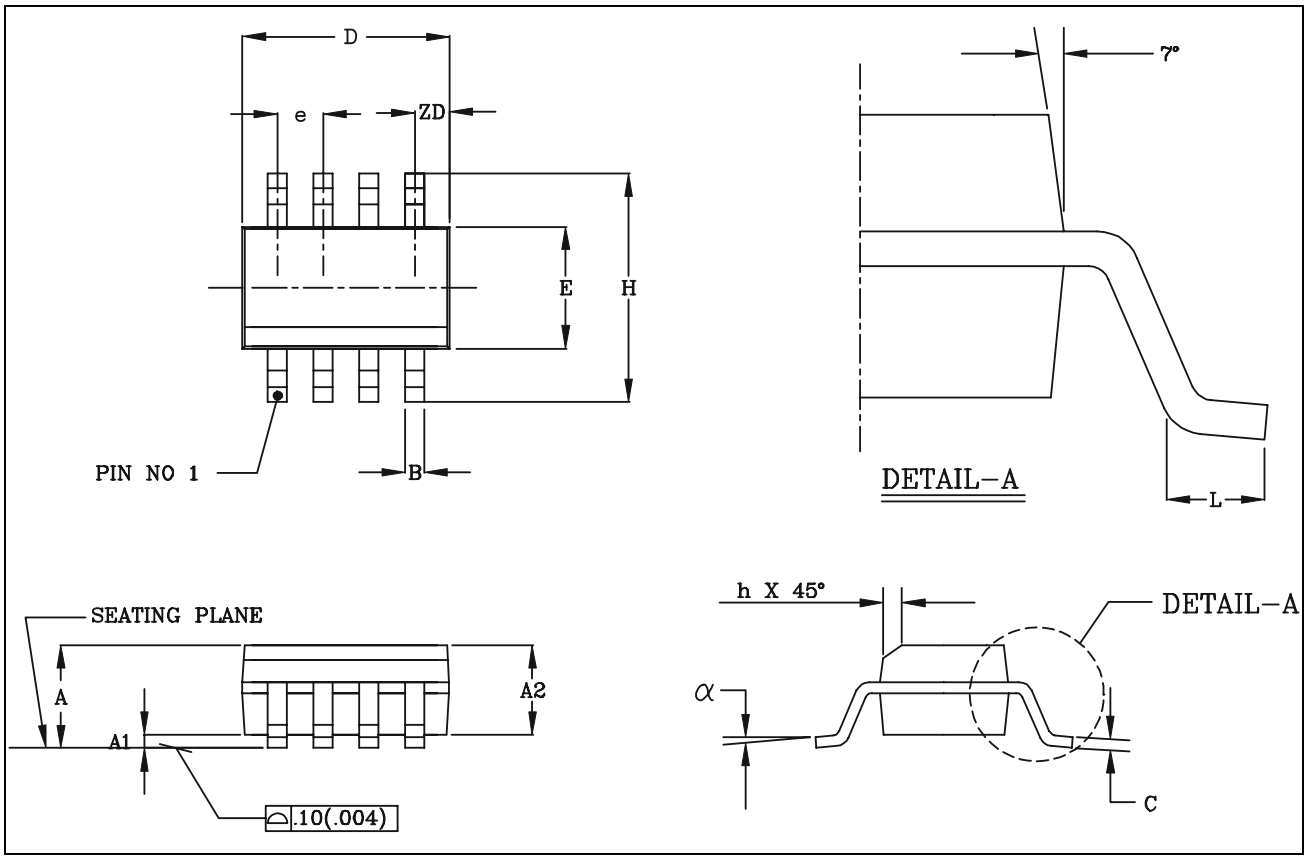
5.1 SOIC14



Small Outline Integrated Circiut (SOIC), SOIC 14, 150 mil

	A1	B	C	D	E	e	H	h	L	A	α	ZD	A2
All Dimension in mm, coplanarity < 0.1 mm													
min	0.10	0.36	0.19	8.56	3.81	1.27	5.80	0.25	0.41	1.52	0°	0.51	1.37
max	0.25	0.45	0.25	8.74	3.99		6.20	0.50	1.27	1.72	8°		1.57
All Dimension in inch, coplanarity < 0.004"													
min	0.004	0.014	0.0075	0.337	0.160	0.050	0.228	0.010	0.016	0.060	0°	0.020	0.054
max	0.01	0.018	0.0098	0.344	0.167		0.244	0.020	0.050	0.068	8°		0.062

5.2 SOIC8

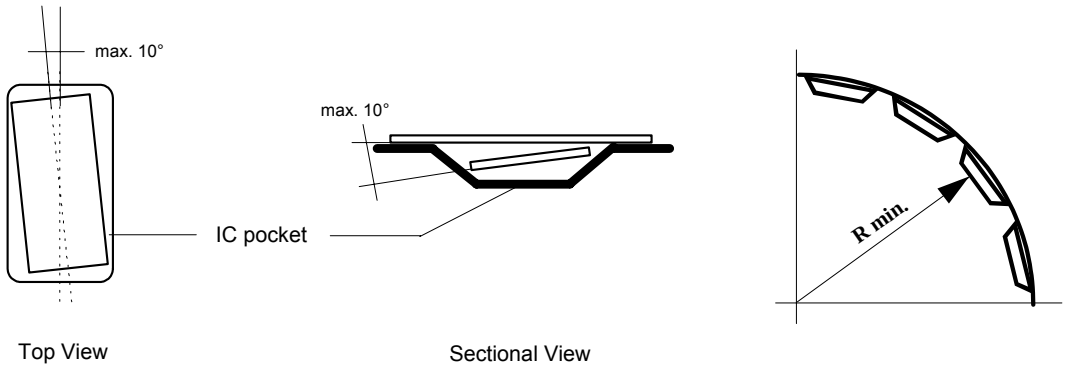


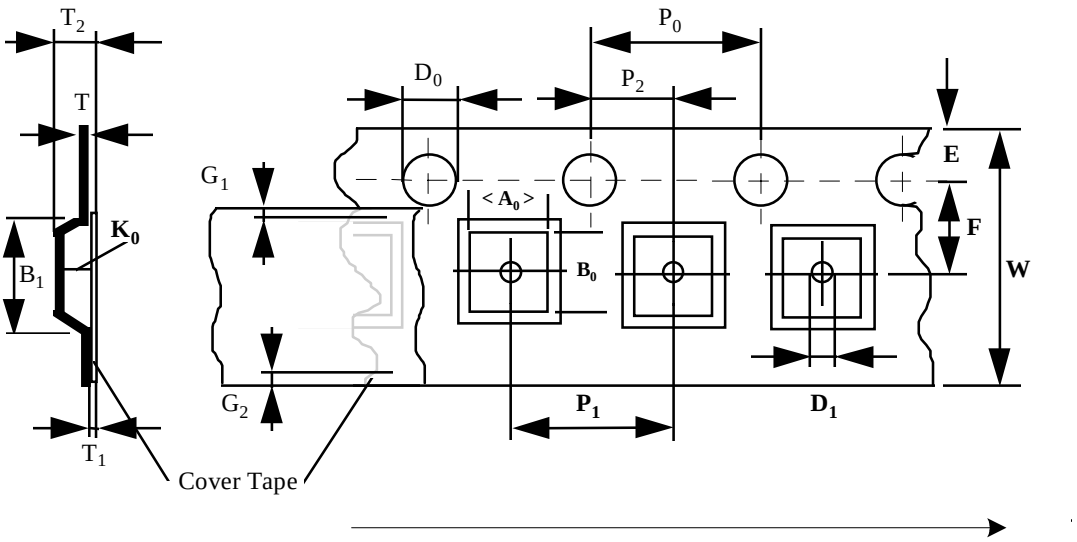
Small Outline Integrated Circiut (SOIC), SOIC 8, 150 mil

	A1	B	C	D	E	e	H	h	L	A	α	ZD	A2
All Dimension in mm, coplanarity < 0.1 mm													
min max	0.10 0.25	0.36 0.46	0.19 0.25	4.80 4.98	3.81 3.99	1.27	5.80 6.20	0.25 0.50	0.41 1.27	1.52 1.72	0° 8°	0.53	1.37 1.57
All Dimension in inch, coplanarity < 0.004”													
min max	0.004 0.0098	0.014 0.018	0.0075 0.0098	0.189 0.196	0.150 0.157	0.050	0.2284 0.244	0.0099 0.0198	0.016 0.050	0.060 0.068	0° 8°	0.021	0.054 0.062

6. Tape and Reel Specification

6.1 Tape Specification





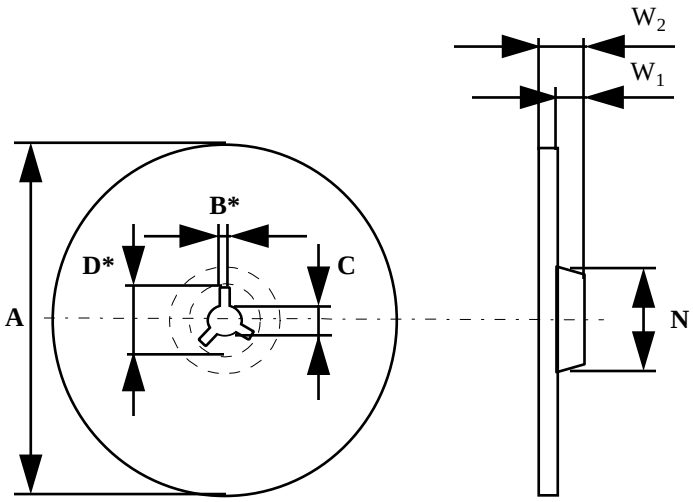
Standard Reel with diameter of 13“

Package	Parts per Reel	Width	Pitch
SOIC14	2500	16 mm	8 mm
SOIC8	2500	12 mm	8 mm

D_0	E	P_0	P_2	T_{max}	$T_{1\,max}$	$G_{1\,min}$	$G_{2\,min}$	$B_{1\,max}$	$D_{1\,min}$	F	P_1	R_{min}	$T_{2\,max}$	W
SOIC14														
1.5 +0.1	1.75 ±0.1	4.0 ±0.1	2.0 ±0.1	0.6	0.1	0.75	0.75	12.1	1.5	7.5 ±0.1	4 – 12 ±0.1	30	8.0	16.0 ±0.3
SOIC8														
1.5 +0.1	1.75 ±0.1	4.0 ±0.1	2.0 ±0.1	0.6	0.1	0.75	0.75	8.2	1.5	5.5 ±0.05	4 ±0.1	30	6.5	12.0 ±0.3

A_0, B_0, K_0 can be calculated with package specification.
Cover Tape width 13.3 mm.

6.2 Reel Specification for SOIC14NB



A_{max}	B*	C	D^*_{min}
330	2.0 ±0.5	13.0 +0,5/-0,2	20.2

Width of half reel	N_{min}	W_1	$W_{2\ max}$
4 mm	100.0	4.4	7.1
8 mm	100.0	8.4	11.1

7. ESD/EMC Remarks

7.1 General Remarks

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

7.2 ESD-Test

The TH8056 is tested according to MIL883D (human body model).

7.3 EMC

The test on EMC impacts is done according to ISO 7637-1 for power supply pins and ISO 7637-3 for data- and signal pins.

Power Supply pin VBAT, CANH, LOAD:

Testpulse	Condition	Duration
1	t_1 = 5 s / U_S = -100 V / t_D = 2 ms	5000 pulses
2	t_1 = 0.5 s / U_S = 100 V / t_D = 0.05 ms	5000 pulses
3a/b	U_S = -200 V/ U_S = 200 V burst 100ns / 10 ms / 90 ms break	1h
5	R_i = 0.5 Ω, t_D = 400 ms t_r = 0.1 ms / U_P+U_S = 40 V	10 pulses every 1min

7.4 Latch Up Test

The TH8056 is tested according to JESD78 (Class 2).

8. Revision History

Version	Changes	Remark	Date
001		Initial Release	Sep. 2002
001a	- Added chapter revision history - Error corrected within Figure 1 - Block Diagram		March 2003
002	- Pinout corrected within Figure 8 – Application Circuitry		06/13/03
003	- compatibility to GMW3089 Version 2.2 - Static Characteristics modified according to GMW3089 V2.2 - Dynamic Characteristics modified according to GMW3089 V2.2 - Bus loading requirements modified according to GMW3089 V2.2 - High-speed Mode added remark - V_{BAT} input pin description changed - Add Tape and Reel Specification - Change of ESD/EMC Remarks		09/18/03
004	- Changed application circuitry according to GMW3089 Rev.2.2		12/01/03
005	- Change of chapter 9. Assembly Information		05/13/04
006	- Change of Order Code		06/14/04
007	- Update of chapter “Features” with compatibility to GMW3089 V2.3 and very low leakage current during loss of ground - Update of chapter “Features” high voltage wake up mode instead of high speed .. - Change of “Static characteristics” o Supply current dominant o Transmit delay - Change of “Dynamic characteristics” o Input min pulse length o Condition for mode change from normal to standby, standby to sleep and sleep to normal - Change of application circuitry acc. To GMW3089 V2.3 Spec.		24/06/04
008	- Change of “Static characteristics” o Offset Wake-up Output High Voltage o Mode pull down resistor		31/08/04
009	- Additional Package Version SOIC8 - Additional chapter “Power Dissipation”		15/04/05
010	- Adaption of sleep mode condition acc. To GMW3089 Rev. 2.4 - Change of ESD capability of CANH pin - Update of Assembly information		21/03/06
011	- Change of Parameter “Input minumum pulse length at CANH” - Change of “Short duration operating supply voltage” - Change of “Receive Delay” - Change of “Low level input voltage” at TxD, Mode 0,1		08/12/06
012	- Change of load pin definition to be compliant to GMW3089 2.4		07/03/07

9. Assembly Information

Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
  Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualification of **RoHS** compliant products (RoHS = European directive on the Restriction Of the Use of Certain Hazardous Substances) please visit the quality page on our website:
http://www.melexis.com/quality_leadfree.asp

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