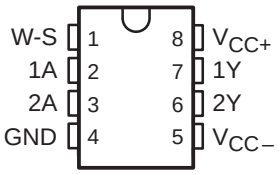
SLLS110B – OCTOBER 1980 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-423-B and -232-E and ITU Recommendations V.10 and V.28**
- **Output Slew Rate Control**
- **Output Short-Circuit-Current Limiting**
- **Wide Supply Voltage Range**
- **8-Pin Package**
- **Designed to Be Interchangeable With National DS9636A**

D OR P PACKAGE
(TOP VIEW)

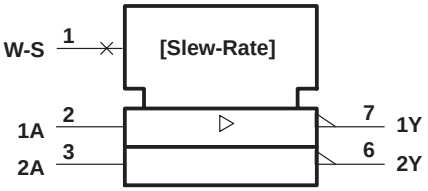


description

The uA9636AC is a dual, single-ended line driver designed to meet ANSI Standards EIA/TIA-423-B and EIA/TIA-232-E and ITU Recommendations V.10 and V.28. The slew rates of both amplifiers are controlled by a single external resistor, $R_{(WS)}$, connected between the wave-shape-control (W-S) terminal and GND. Output current limiting is provided. Inputs are compatible with TTL and CMOS and are diode protected against negative transients. This device operates from ±12 V and is supplied in an 8-pin package.

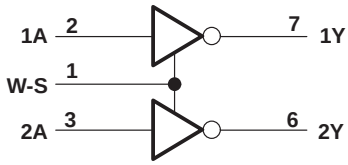
The uA9636AC is characterized for operation from 0°C to 70°C.

logic symbol†

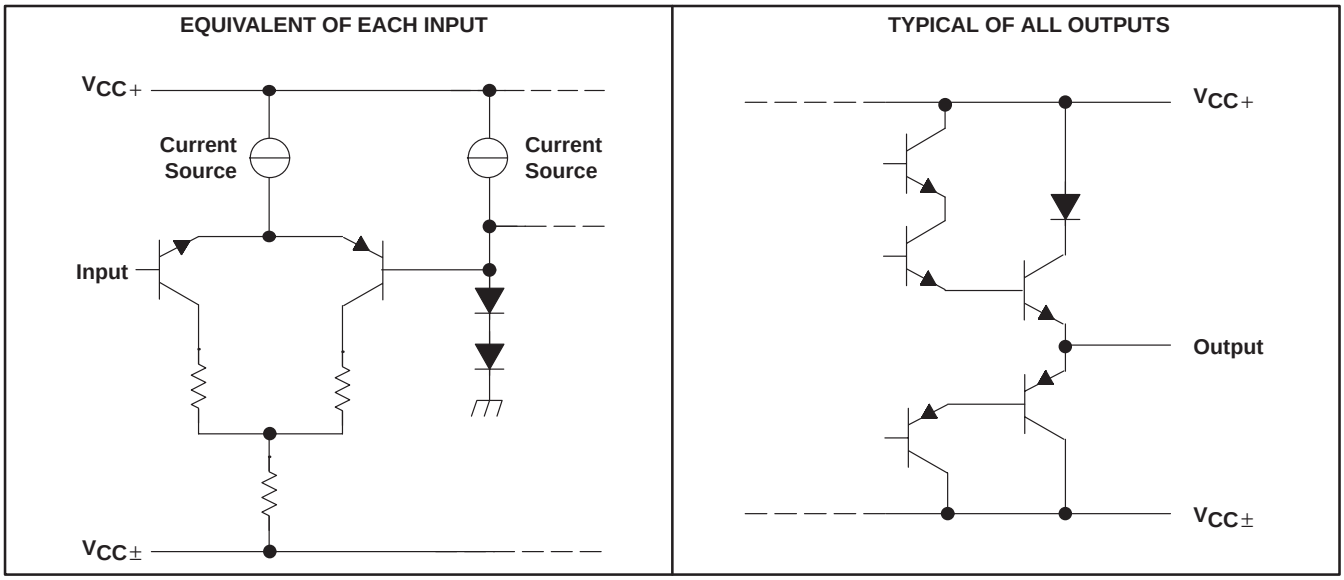


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Positive supply voltage range, V_{CC+} (see Note 1) . . . . . V_{CC-} to 15 V
Negative supply voltage range, V_{CC-} . . . . . 0.5 V to –15 V
Output voltage, V_O . . . . . ±15 V
Output current, I_O . . . . . ±150 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Positive supply voltage, V_{CC+}	10.8	12	13.2	V
Negative supply voltage, V_{CC-}	–10.8	–12	–13.2	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Wave-shaping resistor, $R_{(WS)}$	10		1000	kΩ
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of free-air temperature, supply voltage, and wave-shaping resistance (unless otherwise noted)

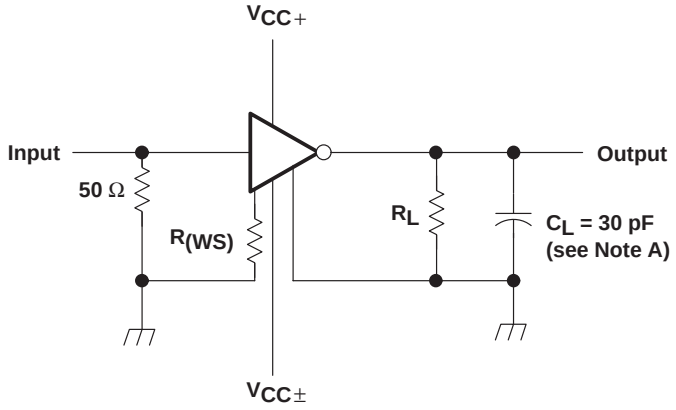
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –15 mA			–1.1	–1.5	V
V_{OH}	High-level output voltage	V_I = 0.8 V	R_L = ∞	5	5.6	6	V
			R_L = 3 kΩ to GND	5	5.6	6	
			R_L = 450 Ω to GND	4	5.4	6	
V_{OL}	Low-level output voltage	V_I = 2 V	R_L = ∞	–6‡	–5.7	–5	V
			R_L = 3 kΩ to GND	–6‡	–5.6	–5	
			R_L = 450 Ω to GND	–6‡	–5.4	–4	
I_{IH}	High-level input current	V_I = 2.4 V				10	μA
		V_I = 5.5 V				100	
I_{IL}	Low-level input current	V_I = 0.4 V			–20	–80	μA
I_O	Output current (power off)	$V_{CC\pm}$ = 0,	V_O = ± 6 V			±100	μA
I_{OS}	Short-circut output current§	V_I = 2 V		15	25	150	mA
		V_I = 0		–15	–40	–150	
r_O	Output resistance	R_L = 450 Ω			25	50	Ω
I_{CC+}	Positive supply current	V_{CC} = ±12 V, $R_{(WS)}$ = 100 kΩ,	V_I = 0, Output open		13	18	mA
I_{CC-}	Negative supply current	V_{CC} = ±12 V, $R_{(WS)}$ = 100 kΩ,	V_I = 0, Output open		–13	–18	mA

† All typical values are at V_{CC} = ±12 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for logic voltage levels, e.g., when –5 V is the maximum, the minimum is a more-negative voltage.
§ Not more than one output should be shorted to ground at a time.

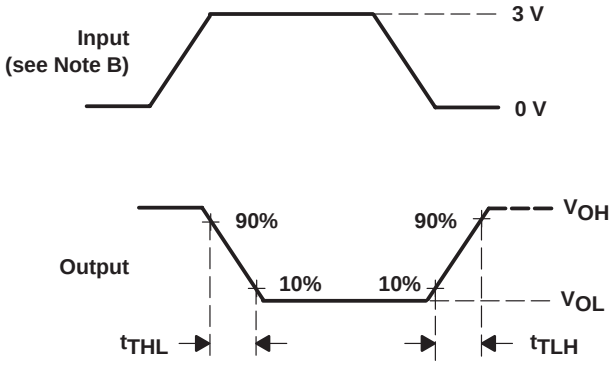
switching characteristics, $V_{CC\pm}$ = ±12 V, T_A = 25°C (see Figure 1)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{TLH}	Transition time, low- to high-level output	R_L = 450 kΩ,	C_L = 30 pF	$R_{(WS)}$ = 10 kΩ	0.8	1.1	1.4	μs
				$R_{(WS)}$ = 100 kΩ	8	11	14	
				$R_{(WS)}$ = 500 kΩ	40	55	70	
				$R_{(WS)}$ = 1 MΩ	80	110	140	
t_{THL}	Transition time, high- to low-level output	R_L = 450 kΩ,	C_L = 30 pF	$R_{(WS)}$ = 10 kΩ	0.8	1.1	1.4	μs
				$R_{(WS)}$ = 100 kΩ	8	11	14	
				$R_{(WS)}$ = 500 kΩ	40	55	70	
				$R_{(WS)}$ = 1 MΩ	80	110	140	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$, PRR ≤ 1 kHz, duty cycle = 50%.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs INPUT VOLTAGE

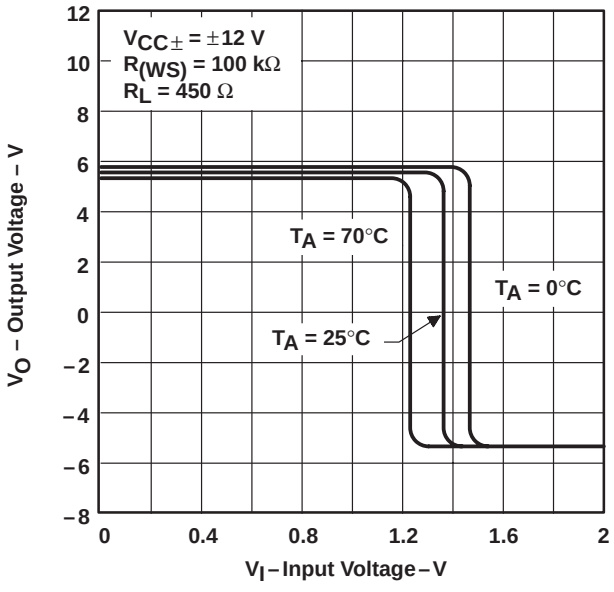


Figure 2

INPUT CURRENT vs INPUT VOLTAGE

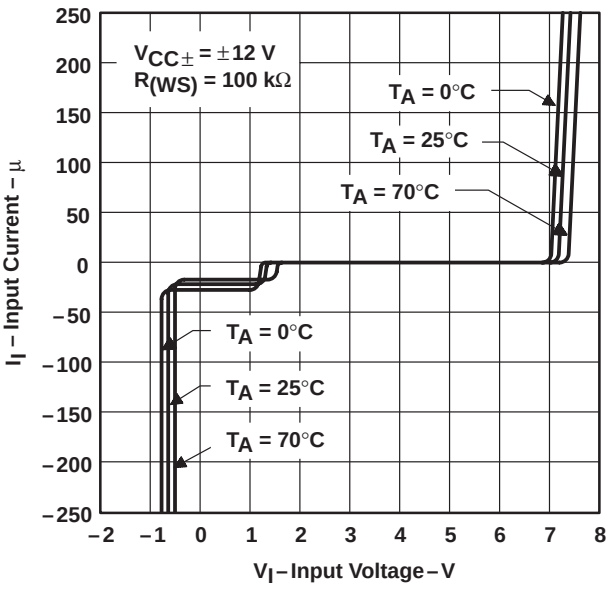


Figure 3

TYPICAL CHARACTERISTICS

OUTPUT CURRENT vs OUTPUT VOLTAGE (POWER ON)

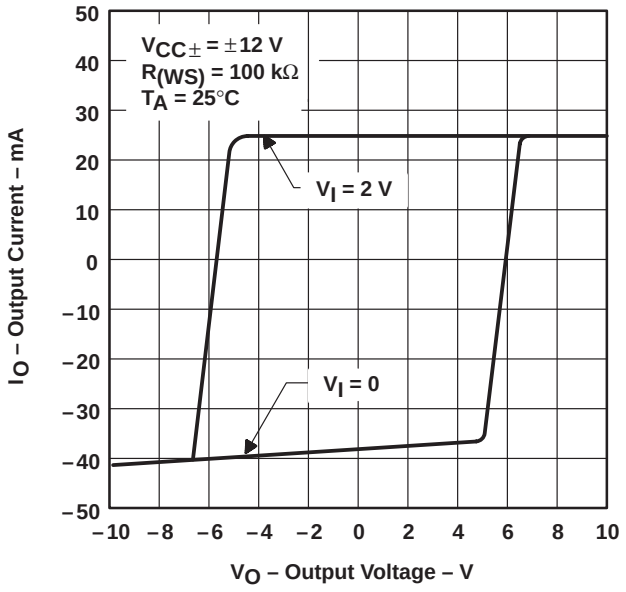


Figure 4

OUTPUT CURRENT vs OUTPUT VOLTAGE (POWER OFF)

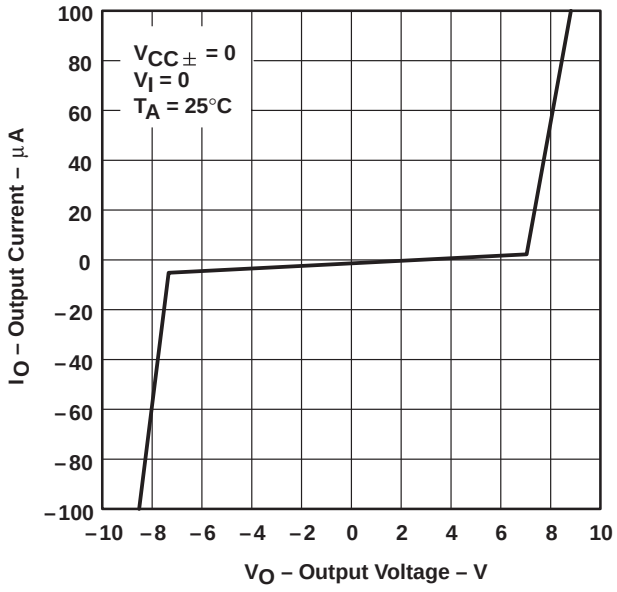


Figure 5

TRANSITION TIME vs WAVE-SHAPING RESISTANCE

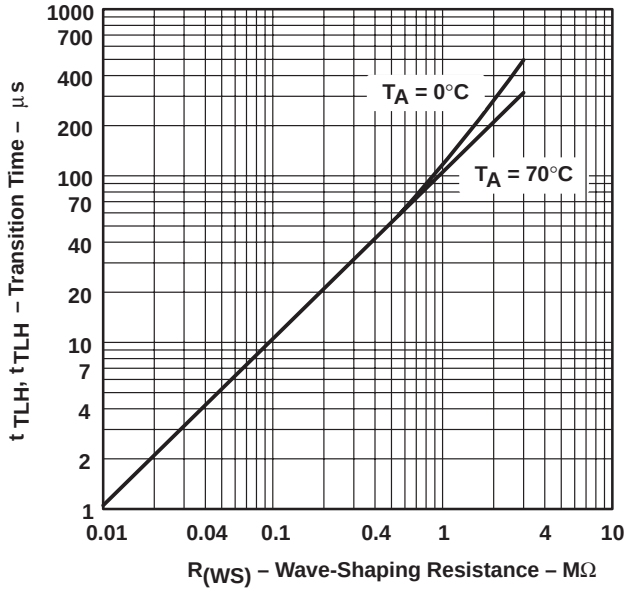


Figure 6

APPLICATION INFORMATION

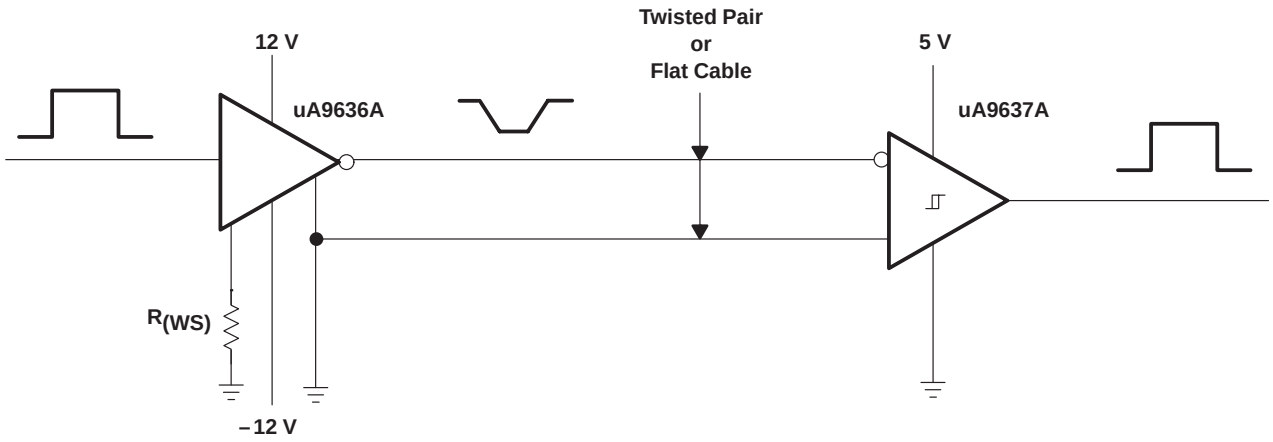


Figure 7. EIA/TIA-423-B System Application

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		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
UA9636ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA9636ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA9636ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA9636ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA9636ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA9636ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA9636ACJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
UA9636ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
UA9636ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

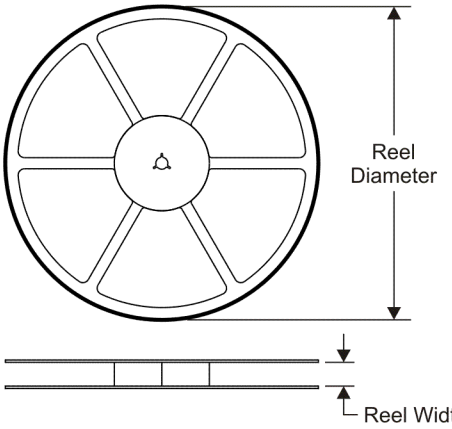
[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

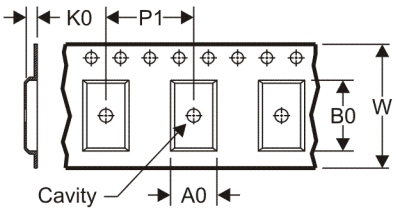
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

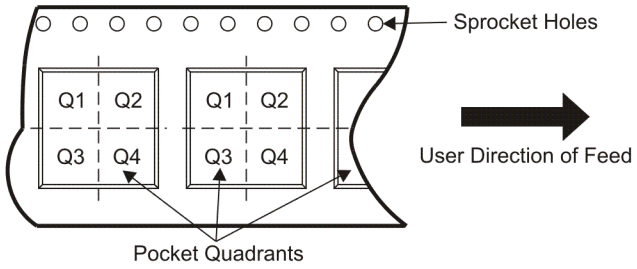


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

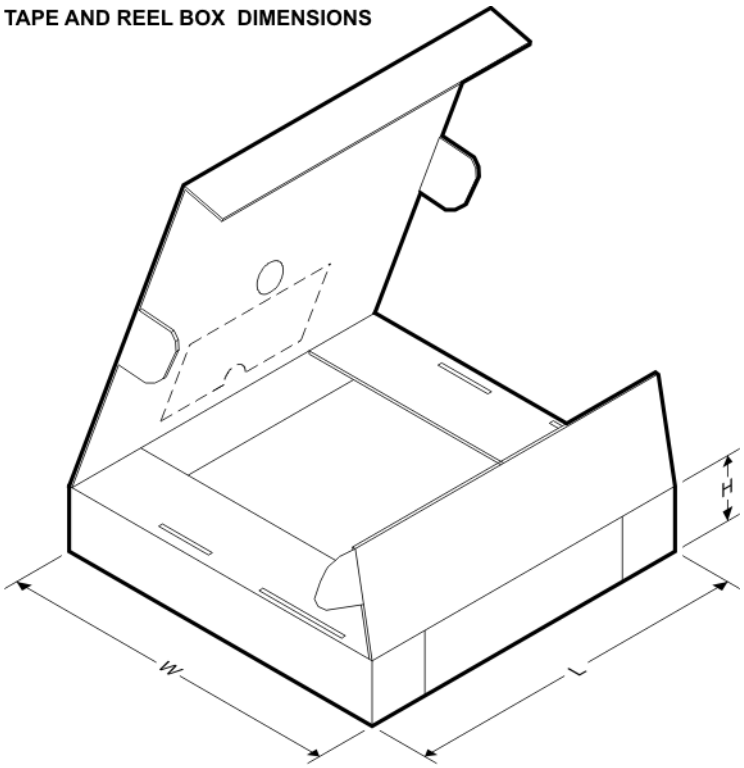
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA9636ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

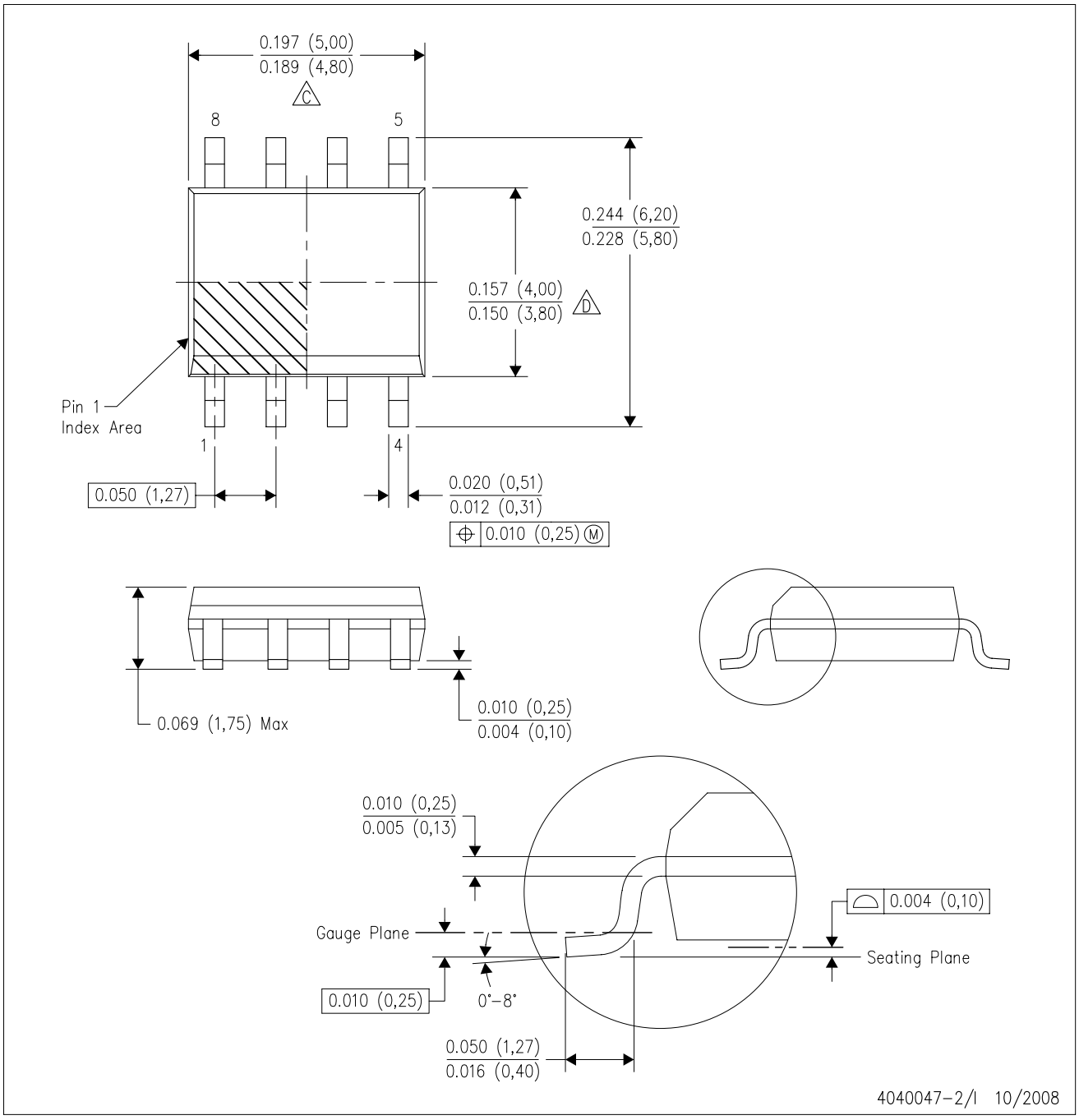
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA9636ACDR	SOIC	D	8	2500	340.5	338.1	20.6

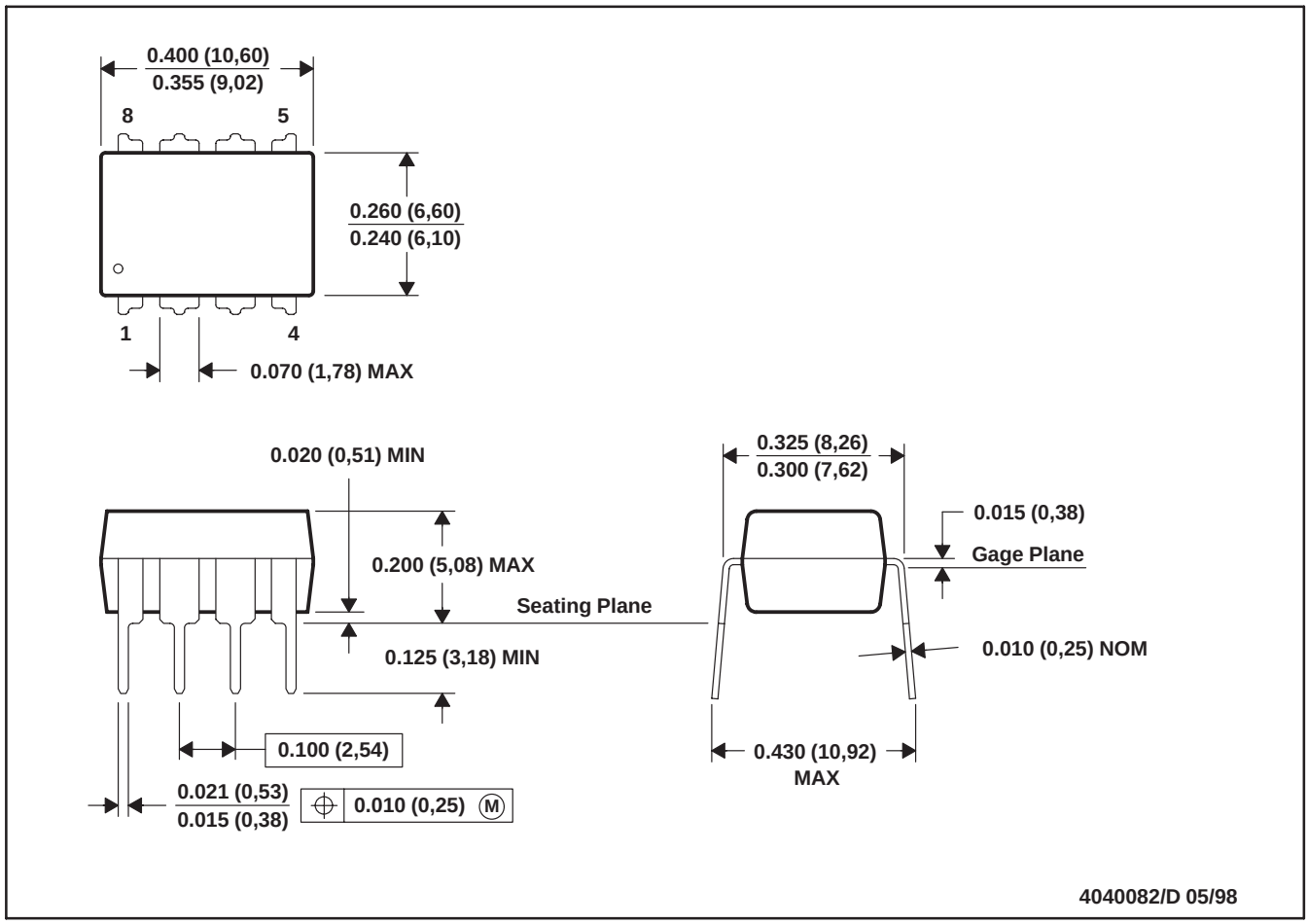
D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

MPDI001A – JANUARY 1995 – REVISED JUNE 1999

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**

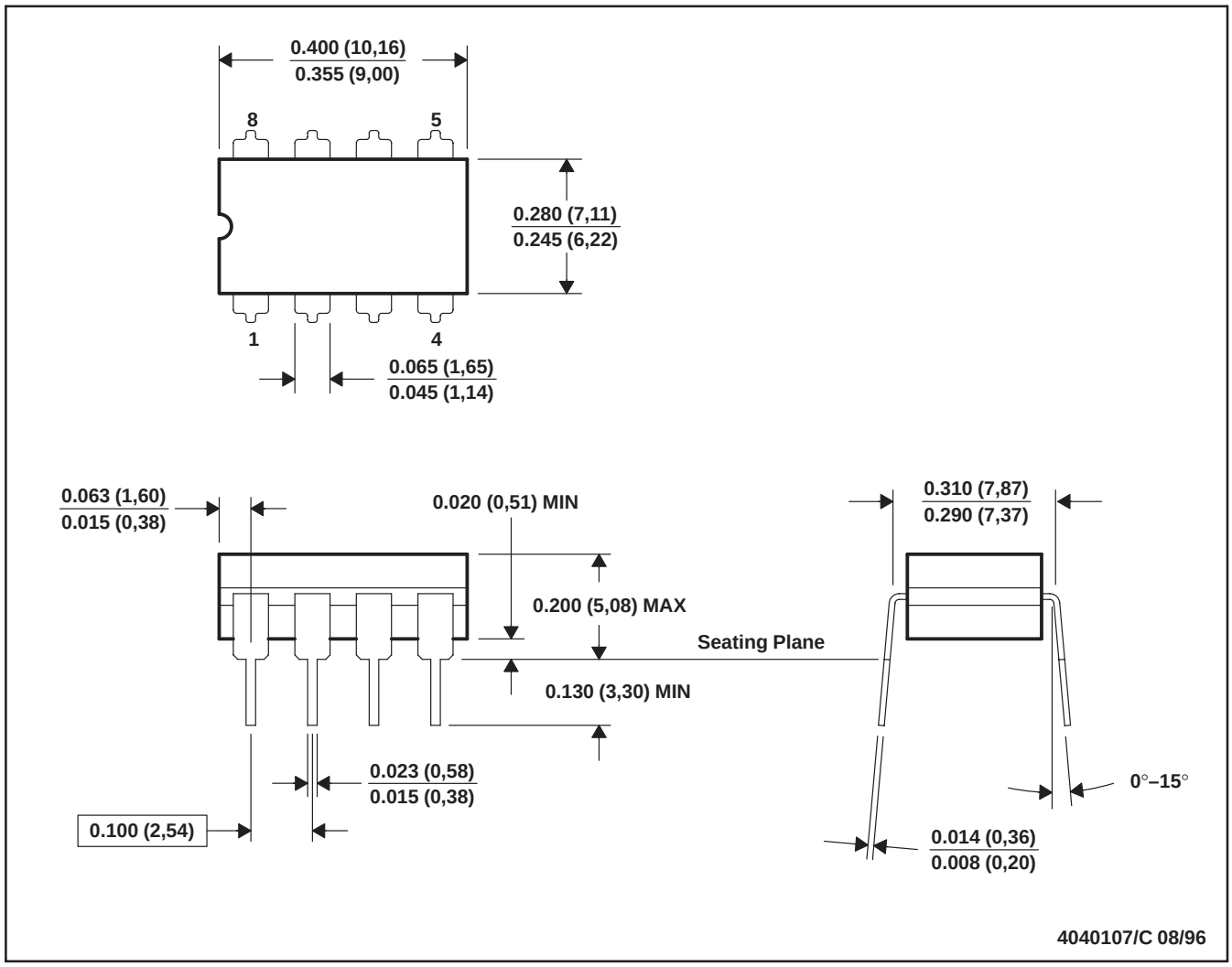


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

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