Three Phase Multi-Function Energy Metering IC with Serial Port

Preliminary Technical Data — ADE7754*

FEATURES

High Accuracy, supports IEC 687/1036
Compatible with 3-phase/3-wire, 3-phase/4-wire and any type of 3-phase services
Less than 0.1% error over a dynamic range of 500 to 1
The ADE7754 supplies *Active Energy, Apparent Energy, Voltage rms, Current rms* and *Sampled Waveform Data*.
Digital Power, Phase & Input Offset Calibration.
An On-Chip temperature sensor (±3°C typ. after calibration)
On-Chip user Programmable thresholds for line voltage SAG and overdrive detections.
A SPI compatible Serial Interface with Interrupt Request line (IRQ).
A pulse output with programmable frequency
Proprietary ADCs and DSP provide high accuracy over large variations in environmental conditions and time.
Reference 2.5V±8% (Drift 30 ppm/°C typical) with external overdrive capability
Single 5V Supply, Low power (15mW typical)

GENERAL DESCRIPTION

The ADE7754 is a high accuracy three-phase electrical energy measurement IC with a serial interface and a pulse output. The ADE7754 incorporates second order sigma-delta ADCs, reference circuitry, temperature sensor, and all the signal processing required to perform Active Energy measurement, Apparent Energy measurement and rms calculation.

The ADE7754 provides different solutions to measure Active and Apparent Energy from the six analog inputs thus enabling the use of the ADE7754 in various Power meter services as 3-phase 4-wire, 3-phase 3-wire but also 4-wire delta.

In addition to RMS calculation, Real and Apparent power informations, the ADE7754 provides system calibration features for each phase, i.e., channel offset correction, phase calibration and power calibration. The CF logic output gives instantaneous real power information.

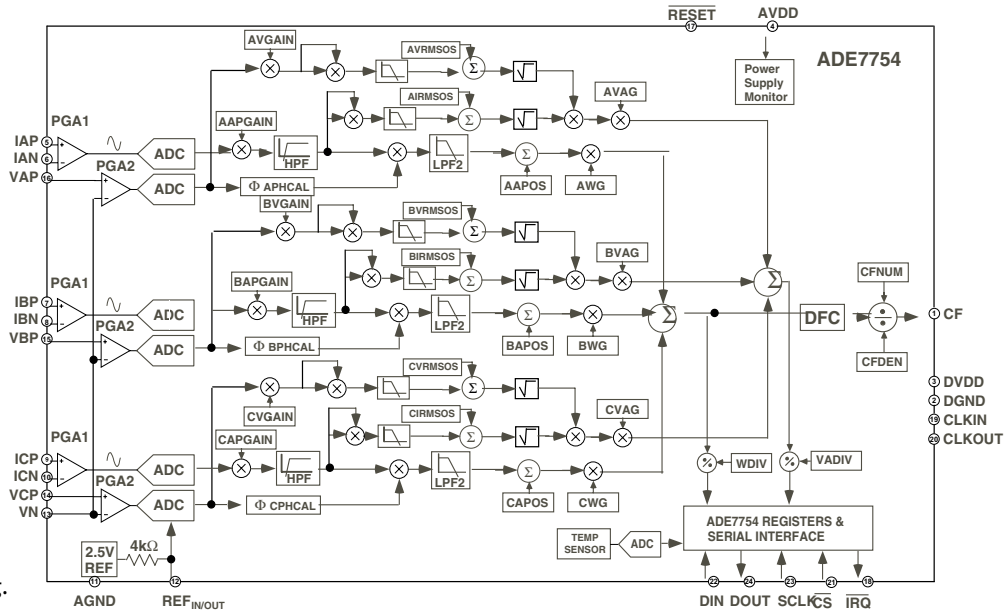
The ADE7754 has a waveform sample register which enables access to ADC outputs. The part also incorporates a detection circuit for short duration low or high voltage variations. The voltage threshold levels and the duration (no. of half line cycles) of the variation are user programmable.

A zero crossing detection is synchronized which the zero crossing point of the line voltage of each of the three phases. This information is used to measure each line's Period. It is also used internally to the chip in the Line Active Energy and Line Apparent Energy accumulation modes. This permits faster and more accurate calibration of the power calculations. This signal is also useful for synchronization of relay switching.

Data is read from the ADE7754 via the SPI serial interface. The interrupt request output ($\overline{IRQ}$) is an open drain, active low logic output. The $\overline{IRQ}$ output will go active low when one or more interrupt events have occurred in the ADE7754. A status register will indicate the nature of the interrupt.

The ADE7754 is available in a 24-lead SOIC package.

FUNCTIONAL BLOCK DIAGRAM



⋆ Patents pending.

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ADE7754–SPECIFICATIONS

(AVDD = DVDD = 5V±5%, AGND = DGND = 0V, On-Chip Reference, CLKIN=10MHz, TMIN to TMAX = -40°C to +85°C)

Parameters		Units	Test Conditions/Comments
ACCURACY			
Measurement Error (per phase)	0.1	% typ	Over a dynamic range of 500 to 1
Phase Error Between Channels			Line Frequency = 45Hz to 65Hz
(PF=0.8 capacitive)	±0.05	° max	Phase Lead 37°
(PF=0.5 inductive)	±0.05	° max	Phase Lag 60°
AC Power Supply Rejection[1]			
Output Frequency Variation	0.01	% typ	V1P = V2P = V3P = ±100mV rms
DC Power Supply Rejection[1]			
Output Frequency Variation	0.01	% typ	V1P = V2P = V3P = ±100mV rms
ANALOG INPUTS			
Maximum Signal Levels	500	mV max	Differential input
Input Impedance (DC)	400	k min	
Bandwidth (-3dB)	3.5	kHz typ	
ADC Offset Error[1]	10	mV max	Uncalibrated error, see Terminology for detail
Gain Error[1]	±4	% typ	External 2.5V reference
Gain Error Match[1]	±3	% typ	External 2.5V reference
REFERENCE INPUT			
$REF_{IN/OUT}$ Input Voltage Range	2.7	V max	2.5V +8%
	2.3	V min	2.5V -8%
Input Impedance	4	kΩ min	
Input Capacitance	10	pF max	
TEMPERATURE SENSOR	±2	°C	Calibrated DC offset
ON-CHIP REFERENCE			
Reference Error	±200	mV max	
Temperature Coefficient	30 typ	ppm/°C	
CLKIN			
Input Clock Frequency	15	MHz max	
	5	MHz min	
LOGIC INPUTS			
$\overline{RESET}$, DIN, SCLK CLKIN and $\overline{CS}$			
Input High Voltage, V_{INH}	2.4	V min	DV_{DD}=5V ± 5%
Input Low Voltage, V_{INL}	0.8	V max	DV_{DD}=5V ± 5%
Input Current, I_{IN}	±3	µA max	Typical 10nA, Vin=0V to DV_{DD}
Input Capacitance, C_{IN}	10	pF max	
LOGIC OUTPUTS			
CF, $\overline{IRQ}$, DOUT and CLKOUT			
Output High Voltage, V_{OH}	4	V min	DVDD=5V ± 5%
Output Low Voltage, V_{OL}	1	V max	DVDD=5V ± 5%
POWER SUPPLY			For specified performance
AV_{DD}	4.75	V min	5V - 5%
	5.25	V max	5V +5%
DV_{DD}	4.75	V min	5V - 5%
	5.25	V max	5V +5%
AI_{DD}	TBD	mA max	
DI_{DD}	TBD	mA max	

NOTES:
1. See Terminology section for explanation of specifications.
2. See plots in Typical Performance Graph.
3. Specification subject to change without notice.

ORDERING GUIDE

MODEL	PACKAGE OPTION
ADE7754AR	SO-24
EVAL-ADE7754EB	ADE7754 Evaluation Board

ADE7754 TIMING CHARACTERISTICS[1,2]

(AV_{DD} = DV_{DD} = 5V ± 5%, AGND = DGND = 0V, On-Chip Reference, CLKIN = 10MHz XTAL, TMIN to TMAX = -40°C to +85°C)

Parameter		Units	Test Conditions/Comments
Write timing			
t_1	50	ns (min)	$\overline{CS}$ falling edge to first SCLK falling edge
t_2	50	ns (min)	SCLK logic high pulse width
t_3	50	ns (min)	SCLK logic low pulse width
t_4	10	ns (min)	Valid Data Set up time before falling edge of SCLK
t_5	5	ns (min)	Data Hold time after SCLK falling edge
t_6	900	ns (min)	Minimum time between the end of data byte transfers.
t_7	50	ns (min)	Minimum time between byte transfers during a serial write.
t_8	100	ns (min)	$\overline{CS}$ Hold time after SCLK falling edge.
Read timing			
t_9	1	µs (min)	Minimum time between read command (i.e. a write to Communication Register) and data read.
t_{10}	50	ns (min)	Minimum time between data byte transfers during a multibyte read.
t_{11}[3]	30	ns (min)	Data access time after SCLK rising edge following a write to the Communications Register
t_{12}[4]	100	ns (max)	Bus relinquish time after falling edge of SCLK.
	10	ns (min)	
t_{13}[4]	100	ns (max)	Bus relinquish time after rising edge of $\overline{CS}$.
	10	ns (min)	

NOTES

[1] Sample tested during initial release and after any redesign or process change that may affect this parameter. All input signals are specified with tr = tf = 5ns (10% to 90%) and timed from a voltage level of 1.6V.

[2] See timing diagram below and Serial Interface section of this data sheet.

[3] Measured with the load circuit in Figure 1 and defined as the time required for the output to cross 0.8V or 2.4V.

[4] Derived from the measured time taken by the data outputs to change 0.5V when loaded with the circuit in Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50pF capacitor. This means that the time quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

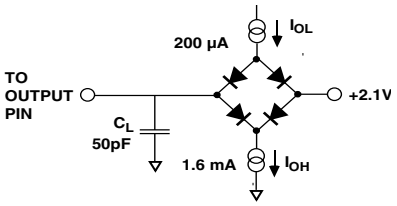
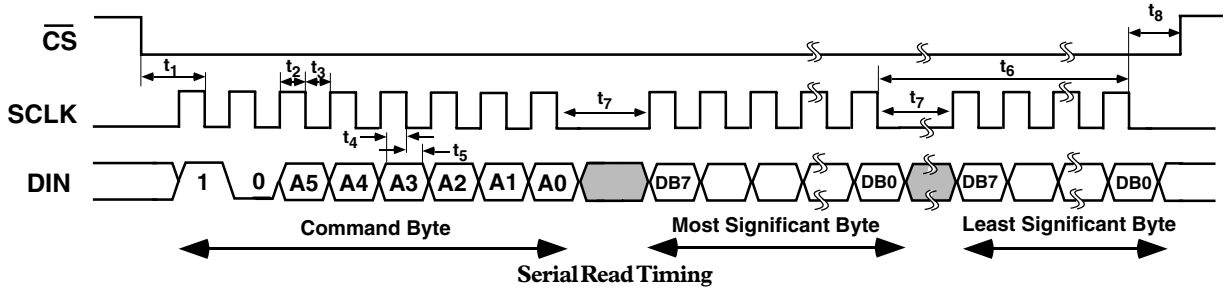
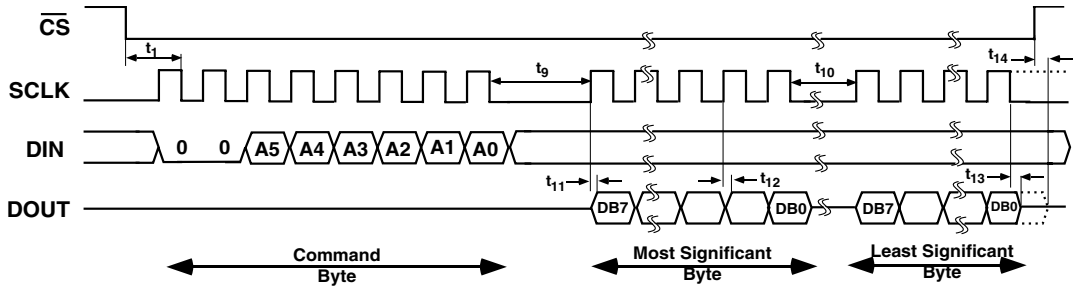


Figure 1 - Load Circuit for Timing Specifications

Serial Write Timing



Serial Read Timing



ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND ..... –0.3V to +7V
DV_{DD} to DGND ..... –0.3V to +7V
DV_{DD} to AV_{DD} ..... –0.3V to +0.3V
Analog Input Voltage to AGND
I_{AP},I_{AN},I_{BP},I_{BN},I_{CP},I_{CN},V_{AP},V_{BP},V_{CP},V_N . –6V to +6V
Reference Input Voltage to AGND –0.3V to AV_{DD}+0.3V
Digital Input Voltage to DGND . –0.3V to DV_{DD}+0.3V
Digital Output Voltage to DGND –0.3V to DV_{DD}+0.3V
Operating Temperature Range
Industrial ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
24-Lead SOIC, Power Dissipation ..... TBD mW
θ_{JA} Thermal Impedance ..... 53°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADE7754 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Terminology

MEASUREMENT ERROR

The error associated with the energy measurement made by the ADE7754 is defined by the following formula:

$$\textit{Percentage Error} = \left(\frac{\textit{Energy registered by ADE7754} - \textit{True Energy}}{\textit{True Energy}} \times 100\%\right)$$

PHASE ERROR BETWEEN CHANNELS

The HPF (High Pass Filter) in the current channel has a phase lead response. To offset this phase response and equalize the phase response between channels a phase correction network is also placed in the current channel. The phase correction network ensures a phase match between the current channels and voltage channels to within ±0.1° over a range of 45Hz to 65Hz and ±0.2° over a range 40Hz to 1kHz. This phase mismatch between the voltage and the current channels can be further reduced with the phase calibration register in each phase.

POWER SUPPLY REJECTION

This quantifies the ADE7754 measurement error as a percentage of reading when the power supplies are varied. For the AC PSR measurement a reading at nominal supplies (5V) is taken. A second reading is obtained with the same input signal levels when an ac (175mVrms/100Hz) signal is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading—see Measurement Error definition above.

For the DC PSR measurement a reading at nominal supplies (5V) is taken. A second reading is obtained with the same input signal levels when the power supplies are varied ±5%. Any error introduced is again expressed as a percentage of reading.

ADC OFFSET ERROR

This refers to the DC offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection - see characteristic curves. However, when HPFs are switched on the offset is removed from the current channels and the power calculation is not affected by this offset.

GAIN ERROR

The gain error in the ADE7754 ADCs, is defined as the difference between the measured ADC output code (minus the offset) and the ideal output code - see *Current Channel ADC* & *Voltage Channel ADC*. The difference is expressed as a percentage of the ideal code.

GAIN ERROR MATCH

The Gain Error Match is defined as the gain error (minus the offset) obtained when switching between a gain of 1, 2 or 4. It is expressed as a percentage of the output ADC code obtained under a gain of 1.

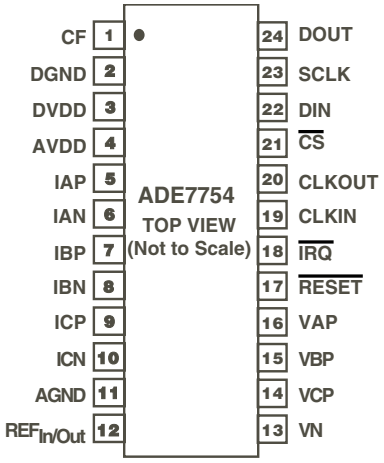
PIN FUNCTION DESCRIPTION

Pin No.	MNEMONIC	DESCRIPTION
1	CF	Calibration Frequency logic output. The CF logic output gives Active Power information. This output is intended to be used for operational and calibration purposes. The full-scale output frequency can be scaled by writing to the CFNUM and CFDEN registers.
2	DGND	This provides the ground reference for the digital circuitry in the ADE7754, i.e. multiplier, filters and digital-to-frequency converter. Because the digital return currents in the ADE7754 are small, it is acceptable to connect this pin to the analog ground plane of the whole system. However high bus capacitance on the DOUT pin may result in noisy digital current which could affect performance.
3	DV_{DD}	Digital power supply. This pin provides the supply voltage for the digital circuitry in the ADE7754. The supply voltage should be maintained at 5V ± 5% for specified operation. This pin should be decoupled to DGND with a 10µF capacitor in parallel with a ceramic 100nF capacitor.
4	AV_{DD}	Analog power supply. This pin provides the supply voltage for the analog circuitry in the ADE7754. The supply should be maintained at 5V ± 5% for specified operation. Every effort should be made to minimize power supply ripple and noise at this pin by the use of proper decoupling. The typical performance graphs in this data sheet show the power supply rejection performance. This pin should be decoupled to AGND with a 10µF capacitor in parallel with a ceramic 100nF capacitor.
5,6; 7,8; 9,10	I_{AP}, I_{AN}; I_{BP}, I_{BN}; I_{CP}, I_{CN}	Analog inputs for current channel. This channel is intended for use with the current transducer and is referenced in this document as the current channel. These inputs are fully differential voltage inputs with maximum differential input signal levels of ±0.5V, ±0.25V and ±0.125V, depending on the gain selections of the internal PGA -See *Analog Inputs*. All inputs have internal ESD protection circuitry, and in addition an overvoltage of ±6V can be sustained on these inputs without risk of permanent damage.
11	AGND	This pin provides the ground reference for the analog circuitry in the ADE7754, i.e. ADCs, temperature sensor, and reference. This pin should be tied to the analog ground plane or the quietest ground reference in the system. This quiet ground reference should be used for all analog circuitry, e.g. anti aliasing filters, current and voltage transducers etc. In order to keep ground noise around the ADE7754 to a minimum, the quiet ground plane should only connected to the digital ground plane at one point. It is acceptable to place the entire device on the analog ground plane.
12	$REF_{IN/OUT}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 2.5V ± 8% and a typical temperature coefficient of 30ppm/°C. An external reference source may also be connected at this pin. In either case this pin should be decoupled to AGND with a 1µF ceramic capacitor.
13, 14 15, 16	V_N, V_{CP}, V_{BP}, V_{AP}	Analog inputs for the voltage channel. This channel is intended for use with the voltage transducer and is referenced as the voltage channel in this document. These inputs are single-ended voltage inputs with maximum signal level of ±0.5V with respect to V_N for specified operation. These inputs are voltage inputs with maximum differential input signal levels of ±0.5V, ±0.25V and ±0.125V, depending on the gain selections of the internal PGA - see *Analog Inputs*. All inputs have internal ESD protection circuitry, and in addition an over voltage of ±6V can be sustained on these inputs without risk of permanent damage.
17	$\overline{RESET}$	Reset pin for the ADE7754. A logic low on this pin will hold the ADCs and digital circuitry (including the Serial Interface) in a reset condition.
18	$\overline{IRQ}$	Interrupt Request Output. This is an active low open drain logic output. Maskable interrupts include: Active Energy Register at half level, Apparent Energy Register at half level, and waveform sampling up to 26kSPS. See *ADE7754 Interrupts*.

Pin No.	MNEMONIC	DESCRIPTION
19	CLKIN	Master clock for ADCs and digital signal processing. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7754. The clock frequency for specified operation is 10MHz. Ceramic load capacitors of between 22pF and 33pF should be used with the gate oscillator circuit. Refer to crystal manufacturers data sheet for load capacitance requirements
20	CLKOUT	A crystal can be connected across this pin and CLKIN as described above to provide a clock source for the ADE7754. The CLKOUT pin can drive one CMOS load when either an external clock is supplied at CLKIN or a crystal is being used.
21	$\overline{CS}$	Chip Select. Part of the four wire Serial Interface. This active low logic input allows the ADE7754 to share the serial bus with several other devices. See *ADE7754 Serial Interface.*
. 22	DIN	Data Input for the Serial Interface. Data is shifted in at this pin on the falling edge of SCLK—see *ADE7754 Serial Interface*.
23	SCLK	Serial Clock Input for the synchronous serial interface. All Serial data transfers are synchronized to this clock—see *ADE7754 Serial Interface*. The SCLK has a Schmidt-trigger Input for use with a clock source which has a slow edge transition time, e.g., opto-isolator outputs etc.
24	DOUT	Data Output for the Serial Interface. Data is shifted out at this pin on the rising edge of SCLK. This logic output is normally in a high impedance state unless it is driving data onto the serial data bus—see *ADE7754 Serial Interface*.

PIN CONFIGURATION

SOIC Package



ACCESSING THE ADE7754 ON-CHIP REGISTERS

All ADE7754 functionality is accessed via the on-chip registers. Each register is accessed by first writing to the communications register and then transferring the register data. For a full description of the serial interface protocol, see *Serial Interface* section of this data sheet.

Communications Register

The Communications register is an eight bit, write-only register which controls the serial data transfer between the ADE7754 and the host processor. All data transfer operations must begin with a write to the communications register. The data written to the communications register determines whether the next operation is a read or a write and which register is being accessed. Table I below outlines the bit designations for the Communications register.

Table VII : Communications Register

Bit Location	Bit Mnemonic	Description
0 to 5	A0 to A5	The five LSBs of the Communications register specify the register for the data transfer operation. Table II lists the address of each ADE7754 on-chip register.
6	RESERVED	This bit is unused and should be set to zero.
7	W/$\overline{R}$	When this bit is a logic one the data transfer operation immediately following the write to the Communications register will be interpreted as a write to the ADE7754. When this bit is a logic zero the data transfer operation immediately following the write to the Communications register will be interpreted as a read operation.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W/$\overline{R}$	0	A5	A4	A3	A2	A1	A0

Table VIII. ADE7754 REGISTER LIST

Address [A5:A0]	Name	R/W*	Length	Default Value	Description
00h	Reserved	-			Reserved.
01h	AENERGY	R	24	0	Active Energy register. Active power is accumulated over time in this read-only register. The AENERGY register can hold a minimum of 5 seconds of active energy information with full-scale analog inputs before it overflows - *See Energy Calculation*. Bit 7 to 3 of the WATMODE register determine how the Active energy is processed from the 6 Analog inputs.
02h	RAENERGY	R	24	0	Same as the AENERGY register, except that the register is reset to zero following a read operation.
03h	LAENERGY	R	24	0	Line Accumulation Active Energy register. The instantaneous active power is accumulated in this read-only register over the LINCYC number of half line cycles. Bit 2 to 0 of the WATMODE register determines, how the Line Accumulation Active energy is processed from the 6 Analog inputs.
04h	VAENERGY	R	24	0	VA Energy register. Real power is accumulated over time in this read-only register. Bit 7 to 3 of the VAMODE register determines, how the Apparent energy is processed from the 6 Analog inputs.
05h	RVAENERGY	R	24	0	Same as the VAENERGY register except that the register is reset to zero following a read operation.
06h	LVAENERGY	R	24	0	Real Energy register. The instantaneous real power is accumulated in this read-only register over the LINCYC number of half line cycles. Bit 2 to 0 of the VAMODE register determines how the Apparent energy is processed from the 6 Analog inputs.
07h	PERIOD	R	15	0	Period of the line input estimated by Zero-crossing processing. Data bits 0 to 1 of the MMODE register determines the voltage channel used for Period calculation.
08h	TEMP	R	8	0	Temperature register. This register contains the result of the latest temperature conversion. Please refer to *Temperature Measurement* section on this datasheet for details on how to interpret the content of this register.
09h	WFORM	R	24	0	Waveform register. This register contains the digitized waveform of one of the six analog inputs. The source is selected by data bits 0 to 2 in the WAVMode register.
0Ah	OPMODE	R/W	8	4	Operational Mode Register. This register defines the general configuration of the ADE7754. See *OPMode Register*.
0Bh	MMODE	R/W	8	70h	Measurement Mode register. This register defines the channel used for Period and Peak detection measurements. See *MMode Register*.
0Ch	WAVMODE	R/W	8	0	Waveform Mode register. This register defines the channel and the sampling frequency used in Waveform sampling mode. See *WAVMode Register*.
0Dh	WATMODE	R/W	8	3Fh	This register configures the formula applied for the Active Energy and Line active energy measurements. See *WATMode Register*.
0Eh	VAMODE	R/W	8	3Fh	This register configures the formula applied for the Apparent Energy and Line Apparent Energy measurements. See *VAMode Register*.
0Fh	MASK	R/W	16	0	IRQ Mask register. It determines if an interrupt event will generate an active-low output at $\overline{\text{IRQ}}$ pin - see *ADE7754 Interrupts*.
10h	STATUS	R	16	0	IRQ Status register. This register contains information regarding the source of ADE7754 interrupts - see *ADE7754 Interrupts*.
11h	RSTATUS	R	16	0	Same as the STATUS register. Except that its contents are reset to zero (all flags cleared) after a read operation.

Address [A5:A0]	Name	R/W*	Length	Default Value	Description
12h	ZXTOUT	R/W	16	FFFFh	Zero Cross Time Out register. If no zero crossing is detected within a time period specified by this register the interrupt request line (IRQ) will go active low for the corresponding line voltage. The maximum time -out period is 2.3 seconds - see *Zero Crossing Detection.*
13h	LINCYC	R/W	16	FFFFh	Line Cycle register. The content of this register sets the number of half line cycles while the active energy and the apparent energy are accumulated in the LAENERGY and LVAENERGY registers - See *Energy Calibration*.
14h	SAGCYC	R/W	8	FFh	Sag Line Cycle register. This register specifies the number of consecutive half-line cycles where voltage channel input falls below a threshold level. This register is common to the three line voltage SAG detection. The detection threshold is specified by SAGLVL register - See *Voltage SAG Detection*.
15h	SAGLVL	R/W	8	0	SAG Voltage Level. This register specifies the detection threshold for SAG event. This register is common to the three line voltage SAG detection. See the description of SAGCYC register for details.
16h	VPEAK	R/W	8	FFh	Voltage Peak Level. This register sets the level of the voltage peak detection. If the selected voltage phase exceeds this level, the PKV flag in the status register is set.
17h	IPEAK	R/W	8	FFh	Current Peak Level. This register sets the level of the current peak detection. If the selected current phase exceeds this level, the PKI flag in the status register is set.
18h	GAIN	R/W	8	0	PGA Gain register. This register is used to adjust the gain selection for the PGA in current and voltage channels - See *Analog Inputs*.
19h	AWG	R/W	12	0	Phase A Active Power Gain register. This register calculation can be calibrated by writing to this register. The calibration range is 50% of the nominal full scale active power. The resolution of the gain adjust is 0.0244% / LSB.
1Ah	BWG	R/W	12	0	Phase B Active Power Gain
1Bh	CWG	R/W	12	0	Phase C Active Power Gain
1Ch	AVAG	R/W	12	0	VA Gain register. This register calculation can be calibrated by writing this register. The calibration range is 50% of the nominal full scale real power. The resolution of the gain adjust is 0.02444% / LSB.
1Dh	BVAG	R/W	12	0	Phase B VA Gain
1Eh	CVAG	R/W	12	0	Phase C VA Gain
1Fh	APHCAL	R/W	6	0	Phase A Phase Calibration Register
20h	BPHCAL	R/W	6	0	Phase B Phase Calibration Register
21h	CPHCAL	R/W	6	0	Phase C Phase Calibration Register
22h	AAPOS	R/W	12	0	Phase A Power Offset Calibration Register
23h	BAPOS	R/W	12	0	Phase B Power Offset Calibration Register
24h	CAPOS	R/W	12	0	Phase C Power Offset Calibration Register
25h	CFNUM	R/W	12	3Fh	CF Scaling Numerator register. The content of this register is used in the numerator of CF output scaling.
26h	CFDEN	R/W	12	3Fh	CF Scaling Denominator register. The content of this register is used in the denominator of CF output scaling.
27h	WDIV	R/W	8	0	Active Energy register divider
28h	VADIV	R/W	8	0	Apparent Energy register divider
29h	AIRMS	R	24	0	Phase A Current channel RMS register. The register contains the RMS component of one input of the current channel. The source is selected by data bits in the mode register.
2Ah	BIRMS	R	24	0	Phase B Current channel RMS register.
2Bh	CIRMS	R	24	0	Phase C Current channel RMS register.
2Ch	AVRMS	R	24	0	Phase A Voltage channel RMS register.
2Dh	BVRMS	R	24	0	Phase B Voltage channel RMS register.
2Eh	CVRMS	R	24	0	Phase C Voltage channel RMS register.

Address [A5:A0]	Name	R/W*	Length	Default Value	Description
2Fh	AIRMSOS	R/W	12	0	Phase A Current RMS offset correction register.
30h	BIRMSOS	R/W	12	0	Phase B Current RMS offset correction register.
31h	CIRMSOS	R/W	12	0	Phase C Current RMS offset correction register.
32h	AVRMSOS	R/W	12	0	Phase A Voltage RMS offset correction register.
33h	BVRMSOS	R/W	12	0	Phase B Voltage RMS offset correction register.
34h	CVRMSOS	R/W	12	0	Phase C Voltage RMS offset correction register.
35h	AAPGAIN	R/W	12	0	Phase A Active Power Gain Adjust. The Active Power accumulation of the phase A can be calibrated by writing to this register. The calibration range is ±50% of the nominal full scale of the Active Power. The resolution of the gain is 0.0244% / LSB - see *Current channel Gain Adjust*
36h	BAPGAIN	R/W	12	0	Phase B Active Power Gain Adjust
37h	CAPGAIN	R/W	12	0	Phase C Active Power Gain Adjust
38h	AVGAIN	R/W	12	0	Phase A voltage RMS gain. The Apparent Power accumulation of the phase A can be calibrated by writing to this register. The calibration range is ±50% of the nominal full scale of the Apparent Power. The resolution of the gain is 0.0244% / LSB - see *Voltage RMS Gain Adjust*
39h	BVGAIN	R/W	12	0	Phase B voltage RMS gain
3Ah	CVGAIN	R/W	12	0	Phase C voltage RMS gain
3Bh 3Dh					Reserved
3Eh	CHKSUM	R	8		Check sum register. The content of this register represents a XOR of each bytes of the latest register read from the SPI port.
3Fh	VERSION	R	8		Version of the Die

*R/W: Read/Write capability of the register.

R: Read only register.

R/W: Register that can be both read and written.

Operational Mode Register (0Ah)

The general configuration of the ADE7754 is defined by writing to the OPMODE register. Table III below summarizes the functionality of each bit in the OPMODE register .

Table IX OPMode Register

Bit Location	Bit Mnemonic	Default Value	Description
0	DISHPF	0	The HPF (High Pass Filter) in all current channel inputs are disabled when this bit is set.
1	DISLPF	0	The LPFs (Low Pass Filter) in all current channel inputs are disabled when this bit is set.
2	DISCF	1	The Frequency output CF is disabled when this bit is set.
3-5	DISMOD	0	By setting these bits, ADE7754's A/D converters can be turned off. In normal operation, these bits should be left at logic zero.
			DISMOD2 DISMOD1 DISMOD0
			0 0 0 Normal operation
			1 0 0 Normal operation, by setting this bit to logic 1 the analog inputs to current channel are connected to the ADC for voltage channel and the analog inputs to voltage channel are connected to the ADC for current channel
			0 0 1 Current channel A/D converters OFF
			0 0 1 Current channel A/D converters OFF + chan nels swapped
			0 1 0 Voltage Channel A/D converters OFF
			1 1 0 Voltage Channel A/D converters OFF + chan nels swapped
			0 1 1 ADE7754 in Sleep Mode
			1 1 1 ADE7754 powered down
6	SWRST	0	Software chip reset. A data transfer to the ADE7754 should not take place for at least 18µs after a software reset.
7	RESERVED	-	This is intended for factory testing only and should be left at zero.

Measurement Mode Register (0Bh)
The configuration of the period and Peak measurements made by the ADE7754 are defined by writing to the MMODE register. Table IV below summarizes the functionality of each bit in the MMODE register .

Table X MMode Register

Bit Location	Bit Mnemonic	Default Value	Description
0-1	PERDSEL	0	These bits are used to select the source of the measurement of the voltage line period. PERDSEL1 PERDSEL0 Source 0 0 Phase A 0 1 Phase B 1 0 Phase C 1 1 Reserved
2-3	PEAKSEL	0	These bits select the line voltage and current phase used for the PEAK detection. If the selected line voltage is above the level defined in the PKVLVL register, the PKV flag in the Interrupt Status register is set. If the selected current input is above the level defined in the PKILVL register, the PKI flag in the Interrupt Status register is set. PEAKSEL1 PEAKSEL0 Source 0 0 Phase A 0 1 Phase B 1 0 Phase C 1 1 Reserved
4-6	ZXSEL	7	These bits select the phases used for counting the number of zero crossing in the Line Active and Apparent accumulation modes. bit 4, 5 and 6 select Phase A, Phase B and Phase C respectively.
7			Reserved

Waveform Mode Register (0Ch)
The Waveform sampling mode of the ADE7754 is defined by writing to the WAVMODE register. Table V below summarizes the functionality of each bit in the WAVMODE register .

Table XI WAVMode Register

Bit Location	Bit Mnemonic	Default Value	Description
0-2	WAVSEL	0	These bits are used to select the source of the Waveform sample WAVSEL2 WAVSEL1 WAVSEL0 Source 0 0 0 Voltage Phase A 0 0 1 Voltage Phase B 0 1 0 Voltage Phase C 0 1 1 Current Phase A 1 0 0 Current Phase B 1 0 1 Current Phase C 1 1 0 or 1 Reserved
3-4	DTRT	0	These bits are used to select the Waveform sampling update rate DTRT1 DTRT0 Update rate 0 0 26.0ksps (CLKIN/3/128) 0 1 13.0ksps (CLKIN/3/256) 1 0 6.5ksps (CLKIN/3/512) 1 1 3.3ksps (CLKIN/3/1024)
5	LVARSEL	0	This bit is used to enable the accumulation of the sign of the Line VAR energy into the LAENERGY register.
6-7			Reserved

Watt Mode Register (0Dh)
The phases involved in the Active Energy measurement of the ADE7754 are defined by writing to the WATMODE register. Table VI below summarizes the functionality of each bit in the WATMODE register .

Table XII WATMode Register

Bit Location	Bit Mnemonic	Default Value	Description
7-6	WATMOD	0	These bits are used to select the formula used for Active Energy calculation WATMOD1 WAVMOD0 Active Energy calculation 0 0 VAxIA + VBxIB + VCxIC 0 1 VAx(IA-IB) + 0 + VCx(IC-IB) 1 0 VAx(IA-IB) + 0 + VCxIC 1 1 Reserved
5-3	WATSEL	7	These bits are used to select separately each part of the formula, depending on the Active Energy measurement method. Setting bit 5 to logic one selects the first term of the formula (VAxIA or VAx(IA-IB)). Setting bit 4 to logic one selects the second term of the formula (VBxIB or 0 depending on WATMOD configuration). Setting bit 3 to logic one selects the last term of the formula (VCxIC or VC(IC-IB)). Any combination of these bits are possible to address calibration and operational needs.
2-0	LWATSEL	7	These bits are used to select separately each part of the formula, depending on the Line Active Energy measurement method. The behavior of these bits is the same as WATSEL bits. Bit 2 selects the first term of the formula and so on.

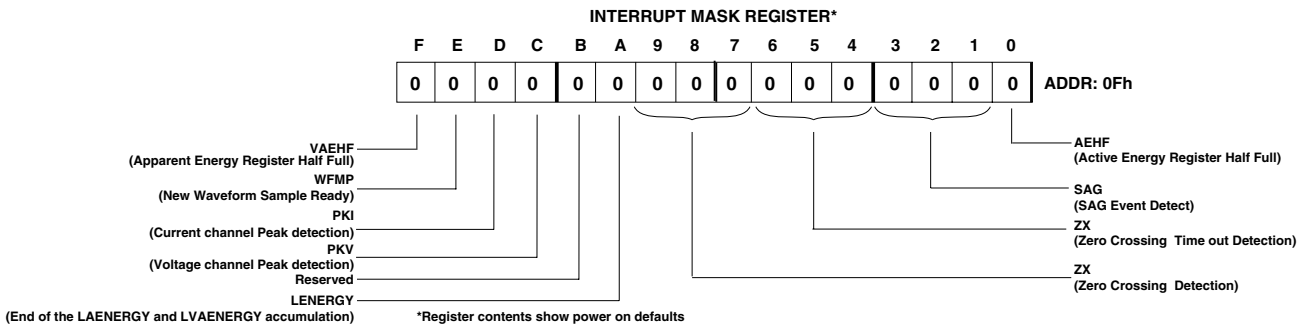
VA Mode Register (0Eh)
The phases involved in the Apparent Energy measurement of the ADE7754 are defined by writing to the VAMODE register. Table VII below summarizes the functionality of each bit in the VAMODE register .

Table XIII VAMode Register

Bit Location	Bit Mnemonic	Default Value	Description
7-6	VAMOD	0	These bits are used to select the formula used for Active Energy calculation VAMOD1 VAMOD0 Apparent Energy calculation 0 0 $VA_{rms}xIA_{rms}+VB_{rms}xIB_{rms}+VC_{rms}xIC_{rms}$ 0 1 $VA_{rms}xIA_{rms}+(VA_{rms}+VC_{rms})/2xIB_{rms}+VC_{rms}xIC_{rms}$ 1 0 $VA_{rms}xIA_{rms}+VA_{rms}xIB_{rms}+VC_{rms}xIC_{rm}$ 1 1 Reserved
5-3	VASEL	7	These bits are used to select separately each part of the formula, depending on the Apparent Energy measurement method. Setting bit 5 to logic one selects the first term of the formula ($VA_{rms}xIA_{rms}$). Setting bit 4 to logic one selects the second term of the formula ($VB_{rms}xIB_{rms}$ or $(VA_{rms}+VC_{rms})/2xIB_{rms}$ or $VA_{rms}xIB_{rms}$ depending on VAMOD configuration). Setting bit 3 to logic one selects the first term of the formula ($VC_{rms}xIC_{rms}$). Any combination of these bits are possible to address calibration and operational needs.
2-0	LVASEL	7	These bits are used to select separately each part of the formula, depending on the Line Apparent Energy measurement method. The behavior of these bits is the same as VASEL bits. Bit 2 selects the first term of the formula and so on.

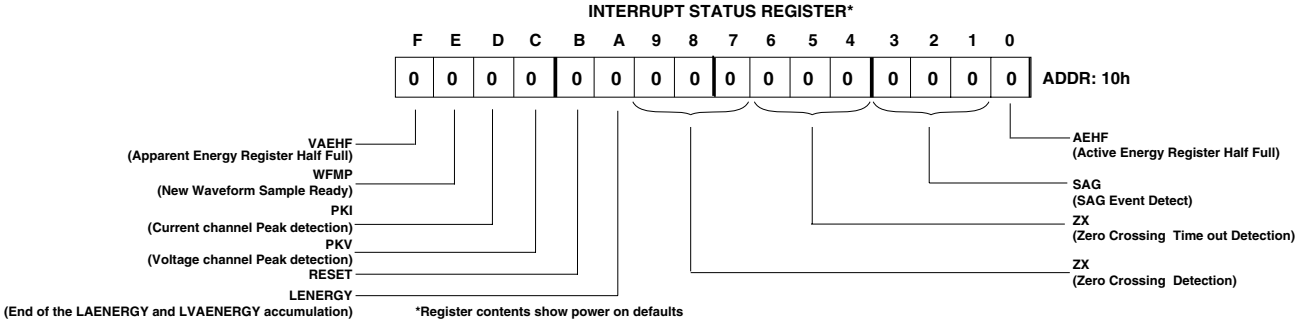
Interrupt Mask Register (0Fh)
When an interrupt event occurs in the ADE7754, the $\overline{IRQ}$ logic output goes active low if the mask bit for this event is logic one in this register. The IRQ logic output is reset to its default collector open state when the RSTATUS register is read. The following describes the function of each bit in the Interrupt Mask Register.

Bit Location	Interrupt Flag	Default Value	Description
0	AEHF	0	Enables an interrupt when there is a 0 to 1 transition of the MSB of the AENERGY register (i.e. the AENERGY register is half-full)
1	SAGA	0	Enables an interrupt when there is a SAG on the line voltage of the Phase A
2	SAGB	0	Enables an interrupt when there is a SAG on the line voltage of the Phase B
3	SAGC	0	Enables an interrupt when there is a SAG on the line voltage of the Phase C
4	ZXTOA	0	Enables an interrupt when there is a zero crossing time out detection on Phase A
5	ZXTOB	0	Enables an interrupt when there is a zero crossing time out detection on Phase B
6	ZXTOC	0	Enables an interrupt when there is a zero crossing time out detection on Phase C
7	ZXA	0	Enables an interrupt when there is a zero crossing in voltage channel of the phase A —*Zero Crossing Detection*
8	ZXB	0	Enables an interrupt when there is a zero crossing in voltage channel of the phase B —*Zero Crossing Detection*
9	ZXC	0	Enables an interrupt when there is a zero crossing in voltage channelof the phase C —*Zero Crossing Detection*
Ah	LENERGY	0	Enables an interrupt when the LAENERGY and LVAENERGY accumulations over LINCYC are finished
Bh			Reserved
Ch	PKV	0	Enables an interrupt when the voltage input selected in the MMODE register is above the value in the PKVLVL register
Dh	PKI	0	Enables an interrupt when the current input selected in the MMODE register is above the value in the PKILVL register.
Eh	WFSM	0	Enables an interrupt when a data is present in the Waveform Register.
Fh	VAEHF	0	Enables an interrupt when there is a 0 to 1 transition of the MSB of the VAENERGY register (i.e. the VAENERGY register is half-full)



Interrupt Status Register (10h) / Reset Interrupt Status Register (11h)
The Interrupt Status Register is used to determine the source of an interrupt event. When an interrupt event occurs in the ADE7754, the corresponding flag in the Interrupt Status Register is set logic high. The $\overline{IRQ}$ pin will go active low if the corresponding bit in the Interrupt Mask register is set logic high. When the MCU services the interrupt, it must first carry out a read from the Interrupt Status Register to determine the source of the interrupt. All the interrupts in the Interrupt Status Register stay at their logic high state after an event occurs. The state of the interrupt bit in the Interrupt Status register is reset to its default value once the Reset Interrupt Status register is read.

Bit Location	Interrupt Flag	Default Value	Event Description
0	AEHF	0	Indicates that an interrupt was caused by the 0 to 1 transition of the MSB of the AENERGY register (i.e. the AENERGY register is half-full)
1	SAGA	0	Indicates that an interrupt was caused by a SAG on the line voltage of the Phase A
2	SAGB	0	Indicates that an interrupt was caused by a SAG on the line voltage of the Phase B
3	SAGC	0	Indicates that an interrupt was caused by a SAG on the line voltage of the Phase C
4	ZXTOA	0	Indicates that an interrupt was caused by a missing zero crossing on the line voltage of the Phase A
5	ZXTOB	0	Indicates that an interrupt was caused by a missing zero crossing on the line voltage of the Phase B
6	ZXTOC	0	Indicates that an interrupt was caused by a missing zero crossing on the line voltage of the Phase C
7	ZXA	0	Indicates a detection of zero crossing in the voltage channel of the phase A
8	ZXB	0	Indicates a detection of zero crossing in the voltage channel of the phase B
9	ZXB	0	Indicates a detection of zero crossing in the voltage channel of the phase C
Ah	LENERGY	0	In Line energy accumulation, it indicates the end of an integration over an integer number of half line cycles (LINCYC) —see *Energy Calibration*
Bh	RESET	0	Indicates that the 5V power supply is below 4V
Ch	PKV	0	Indicates that an interrupt was caused when the selected voltage input is above the value in the PKVLV register.
Dh	PKI	0	Indicates that an interrupt was caused when the selected current input is above the value in the PKILV register.
Eh	WFSM	0	Indicates that new data is present in the Waveform Register.
Fh	VAEHF	0	Indicates that an interrupt was caused by the 0 to 1 transition of the MSB of the VAENERGY register (i.e. the VAENERGY register is half-full)



ADE7754

NOTE

For a complete datasheet of the ADE7754, please contact us on our website at:
http://forms.analog.com/Form_Pages/energymeter/contact.asp

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

24-LEAD SOIC

(R-24)