20 mW Power, 2.3 V to 5.5 V, 50 MHz Complete DDS

AD9834

FEATURES

Narrow-band SFDR >72 dB
2.3 V to 5.5 V Power Supply
50 MHz Ref Clock, 0 MHz to 25 MHz Output
Sine Output/Triangular Output
On-Board Comparator
3-Wire SPI® Interface
Extended Temperature Range: –40°C to +105°C
Power-Down Option
20 mW Power Consumption at 3 V
20-Lead TSSOP Package

APPLICATIONS

Frequency Stimulus/Waveform Generation
Frequency Phase Tuning and Modulation
Low Power RF/Communications Systems
Liquid and Gas Flow Measurement
Sensory Applications—Proximity, Motion, and Defect Detection
Test and Medical Equipment

GENERAL DESCRIPTION

The AD9834 is a 50 MHz low power DDS device capable of producing high performance sine and triangular outputs. It also has an on-board comparator that allows a square wave to be produced for clock generation. Consuming only 20 mW of power at 3 V makes the AD9834 an ideal candidate for power-sensitive applications.

Capability for phase modulation and frequency modulation is provided. The Frequency registers are 28 bits; with a 50 MHz clock rate, resolution of 0.2 Hz can be achieved. Similarly, with a 1 MHz clock rate, the AD9834 can be tuned to 0.004 Hz resolution. Frequency and phase modulation are affected by loading registers through the serial interface and toggling the registers using software or the FSELECT/PSELECT pins, respectively.

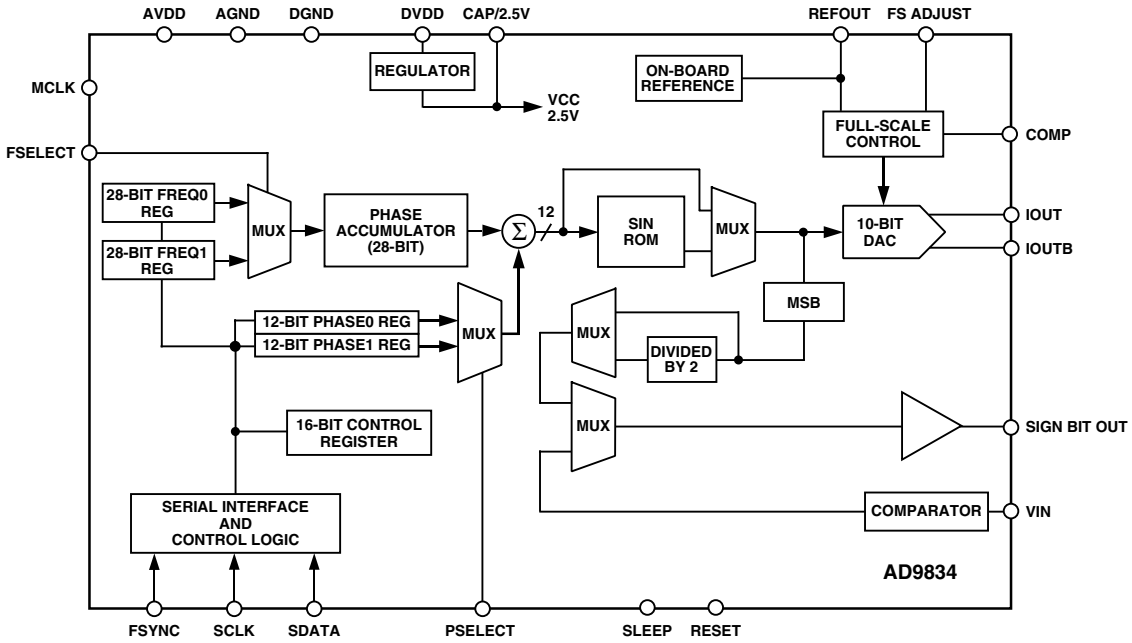
The AD9834 is written to via a 3-wire serial interface. This serial interface operates at clock rates up to 40 MHz and is compatible with DSP and microcontroller standards.

The device operates with a power supply from 2.3 V to 5.5 V. The analog and digital sections are independent and can be run from different power supplies, e.g., AVDD can equal 5 V with DVDD equal to 3 V.

The AD9834 has a power-down pin (SLEEP) that allows external control of the power-down mode. Sections of the device that are not being used can be powered down to minimize the current consumption, e.g., the DAC can be powered down when a clock output is being generated.

The part is available in a 20-lead TSSOP package.

FUNCTIONAL BLOCK DIAGRAM



REV. 0

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AD9834–SPECIFICATIONS[1] (VDD = 2.3 V to 5.5 V, AGND = DGND = 0 V, $T_A = T_{MIN}$ to T_{MAX}, R_{SET} = 6.8 kΩ, R_{LOAD} = 200 Ω for IOUT and IOUTB, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SIGNAL DAC SPECIFICATIONS					
Resolution		10		Bits	
Update Rate			50	MSPS	
I_{OUT} Full Scale[2]		3.0		mA	
V_{OUT} Max		0.6		V	
V_{OUT} Min		30		mV	
Output Compliance[3]			0.8	V	
DC Accuracy					
Integral Nonlinearity		±1		LSB	
Differential Nonlinearity		±0.5		LSB	
DDS SPECIFICATIONS					
Dynamic Specifications					
Signal-to-Noise Ratio	55	60		dB	f_{MCLK} = 50 MHz, $f_{OUT} = f_{MCLK}/4096$
Total Harmonic Distortion		–66	–56	dBc	f_{MCLK} = 50 MHz, $f_{OUT} = f_{MCLK}/4096$
Spurious-Free Dynamic Range (SFDR)					
Wideband (0 to Nyquist)		–60	–56	dBc	f_{MCLK} = 50 MHz, $f_{OUT} = f_{MCLK}/50$
Narrow Band (±200 kHz)		–78	–67	dBc	f_{MCLK} = 50 MHz, $f_{OUT} = f_{MCLK}/50$
Clock Feedthrough		–50		dBc	
Wake-Up Time		1		ms	
COMPARATOR					
Input Voltage Range			1	V p-p	AC-Coupled Internally
Input Capacitance		10		pF	
Input High-Pass Cutoff Frequency		4		MHz	
Input DC Resistance		5		MΩ	
Input Leakage Current			10	µA	
OUTPUT BUFFER					
Output Rise/Fall Time		12		ns	Using a 15 pF Load
Output Jitter		120		ps rms	3 MHz Sine Wave 0.6 V p-p
VOLTAGE REFERENCE					
Internal Reference	1.12	1.18	1.24	V	
REFOUT Output Impedance[4]		1		kΩ	
Reference TC		100		ppm/°C	
LOGIC INPUTS					
V_{INH}, Input High Voltage	1.7			V	2.3 V to 2.7 V Power Supply
	2.0			V	2.7 V to 3.6 V Power Supply
	2.8			V	4.5 V to 5.5 V Power Supply
V_{INL}, Input Low Voltage			0.6	V	2.3 V to 2.7 V Power Supply
			0.7	V	2.7 V to 3.6 V Power Supply
			0.8	V	4.5 V to 5.5 V Power Supply
I_{INH}/I_{INL}, Input Current			10	µA	
C_{IN}, Input Capacitance		3		pF	
POWER SUPPLIES					f_{MCLK} = 50 MHz, $f_{OUT} = f_{MCLK}/4096$
AVDD	2.3		5.5	V	
DVDD	2.3		5.5	V	
I_{AA}[5]		3.8	5	mA	
I_{DD}[5]		2.0	3	mA	I_{DD} Code Dependent. See TPC 2.
$I_{AA} + I_{DD}$[5]		5.8	8	mA	
Low Power Sleep Mode		0.5		mA	DAC Powered Down, MCLK Running

NOTES

[1]Operating temperature range is as follows: B Version: –40°C to +105°C, typical specifications are at 25°C.

[2]For compliance, with specified load 200 Ω, I_{OUT} full scale should not exceed 4 mA.

[3]Guaranteed by design.

[4]Applies when REFOUT is sourcing current. The impedance is higher when REFOUT is sinking current.

[5]Measured with the digital inputs static and equal to 0 V or DVDD.

Specifications subject to change without notice.

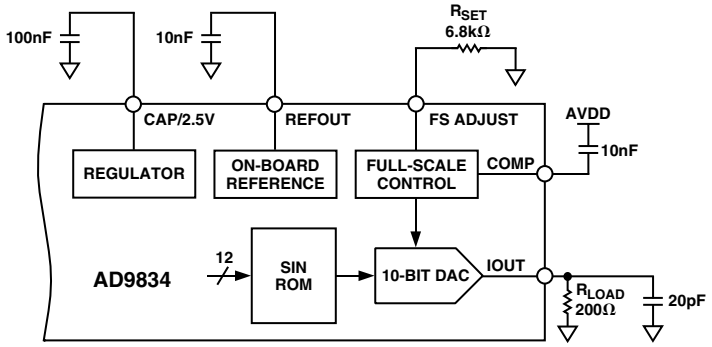


Figure 1. Test Circuit Used to Test the Specifications

TIMING CHARACTERISTICS[1] (DVDD = 2.3 V to 5.5 V, AGND = DGND = 0 V, unless otherwise noted.)

Parameter	Limit at T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
t_1	20	ns min	MCLK Period
t_2	8	ns min	MCLK High Duration
t_3	8	ns min	MCLK Low Duration
t_4	25	ns min	SCLK Period
t_5	10	ns min	SCLK High Duration
t_6	10	ns min	SCLK Low Duration
t_7	5	ns min	FSYNC to SCLK Falling Edge Setup Time
$t_{8\ min}$	10	ns min	FSYNC to SCLK Hold Time
$t_{8\ max}$	t_4–5	ns max	
t_9	5	ns min	Data Setup Time
t_{10}	3	ns min	Data Hold Time
t_{11}	8	ns min	FSELECT, PSELECT Setup Time before MCLK Rising Edge
t_{11A}	8	ns min	FSELECT, PSELECT Setup Time after MCLK Rising Edge
t_{12}	5	ns min	SCLK High to FSYNC Falling Edge Setup Time

[1]Guaranteed by design, not production tested.

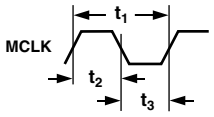


Figure 2. Master Clock

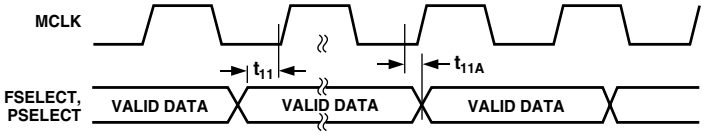


Figure 3. Control Timing

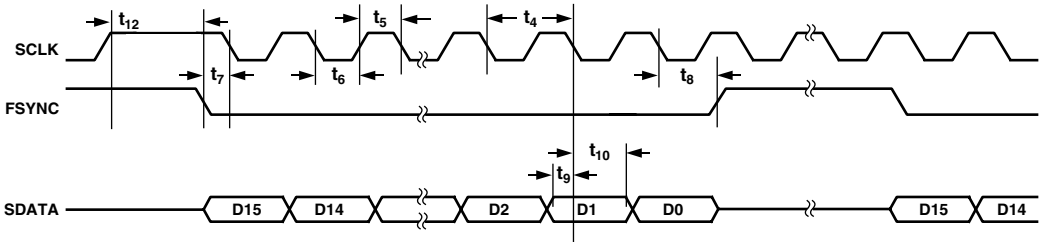


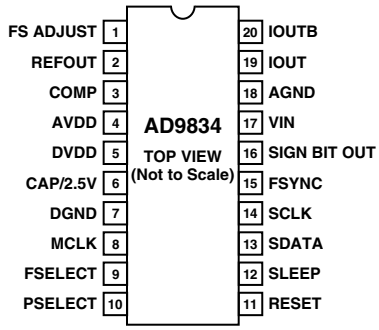
Figure 4. Serial Timing

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C, unless otherwise noted.)

AVDD to AGND ..... –0.3 V to +6 V
DVDD to DGND ..... –0.3 V to +6 V
AVDD to DVDD ..... –0.3 V to +0.3 V
AGND to DGND ..... –0.3 V to +0.3 V
CAP/2.5V ..... 2.75 V
Digital I/O Voltage to DGND ..... –0.3 V to DVDD + 0.3 V
Analog I/O Voltage to AGND ..... –0.3 V to AVDD + 0.3 V
Operating Temperature Range
  Industrial (B Version) ..... –40°C to +105°C
Storage Temperature Range ..... –65°C to +150°C
Maximum Junction Temperature ..... 150°C
TSSOP Package
  θ_{JA} Thermal Impedance ..... 143°C/W
  θ_{JC} Thermal Impedance ..... 45°C/W
Lead Temperature, Soldering (10 sec) ..... 300°C
  IR Reflow, Peak Temperature ..... 220°C

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9834BRU	–40°C to +105°C	20-Lead TSSOP (Thin Shrink Small Outline Package)	RU-20
EVAL-AD9834EB		Evaluation Board	

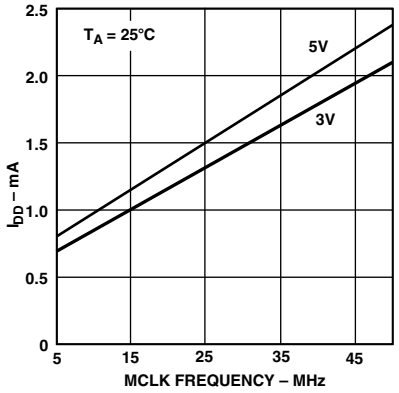
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9834 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

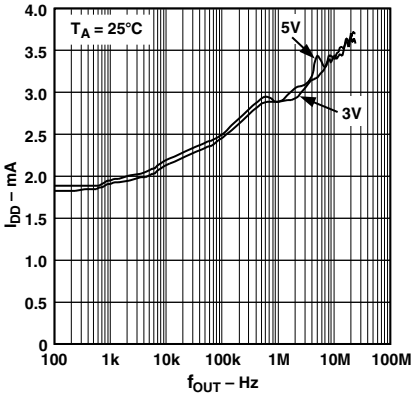
PIN FUNCTIONS DESCRIPTIONS

Pin Number	Mnemonic	Function
Analog Signal and Reference		
1	FS ADJUST	Full-Scale Adjust Control. A resistor (R_{SET}) is connected between this pin and AGND. This determines the magnitude of the full-scale DAC current. The relationship between R_{SET} and the full-scale current is as follows: $IOUT_{FULL\ SCALE} = 18 \times V_{REFOUT}/R_{SET}$ $V_{REFOUT} = 1.20\ V$ *nominal,* $R_{SET} = 6.8\ k\Omega$ *typical*
2	REFOUT	Voltage Reference Output. The AD9834 has an internal 1.20 V reference that is made available at this pin.
3	COMP	DAC Bias Pin. This pin is used for decoupling the DAC bias voltage.
17	VIN	Input to Comparator. The comparator can be used to generate a square wave from the sinusoidal DAC output. The DAC output should be filtered appropriately before being applied to the comparator to improve jitter. When bits OPBITEN and SIGNPIB in the control register are set to "1," the comparator input is connected to VIN.
19, 20	IOUT, IOUTB	Current Output. This is a high impedance current source. A load resistor of nominally 200 Ω should be connected between IOUT and AGND. IOUTB should preferably be tied through an external load resistor of 200 Ω to AGND, but can be tied directly to AGND. A 20 pF capacitor to AGND is also recommended to prevent clock feedthrough.
Power Supply		
4	AVDD	Positive Power Supply for the Analog Section. AVDD can have a value from 2.3 V to 5.5 V. A 0.1 μF decoupling capacitor should be connected between AVDD and AGND.
5	DVDD	Positive Power Supply for the Digital Section. DVDD can have a value from 2.3 V to 5.5 V. A 0.1 μF decoupling capacitor should be connected between DVDD and DGND.
6	CAP/2.5V	The digital circuitry operates from a 2.5 V power supply. This 2.5 V is generated from DVDD using an on-board regulator (when DVDD exceeds 2.7 V). The regulator requires a decoupling capacitor of typically 100 nF that is connected from CAP/2.5V to DGND. If DVDD is equal to or less than 2.7 V, CAP/2.5V should be shorted to DVDD.
7	DGND	Digital Ground.
18	AGND	Analog Ground.
Digital Interface and Control		
8	MCLK	Digital Clock Input. DDS output frequencies are expressed as a binary fraction of the frequency of MCLK. The output frequency accuracy and phase noise are determined by this clock.
9	FSELECT	Frequency Select Input. FSELECT controls which frequency register, FREQ0 or FREQ1, is used in the phase accumulator. The frequency register to be used can be selected using the pin FSELECT or the bit FSEL. When the bit FSEL is being used to select the frequency register, this pin, FSELECT, should be tied to CMOS high or low.
10	PSELECT	Phase Select Input. PSELECT controls which phase register, PHASE0 or PHASE1, is added to the phase accumulator output. The phase register to be used can be selected using the pin PSELECT or the bit PSEL. When the phase registers are being controlled by the bit PSEL, this pin, PSELECT, should be tied to CMOS high or low.
11	RESET	Active High Digital Input. RESET resets appropriate internal registers to zero, which corresponds to an analog output of midscale. RESET does not affect any of the addressable registers.
12	SLEEP	Active High Digital Input. When this pin is high, the DAC is powered down. This pin has the same function as control bit SLEEP12.
13	SDATA	Serial Data Input. The 16-bit serial data-word is applied to this input.
14	SCLK	Serial Clock Input. Data is clocked into the AD9834 on each falling SCLK edge.
15	FSYNC	Active Low Control Input. This is the frame synchronization signal for the input data. When FSYNC is taken low, the internal logic is informed that a new word is being loaded into the device.
16	SIGN BIT OUT	Logic Output. The comparator output is available on this pin or, alternatively, the MSB from the NCO can be output on this pin. Setting bit OPBITEN in the control register to "1" enables this output pin. Bit SIGNPIB determines whether the comparator output or the MSB from the NCO is output on the pin.

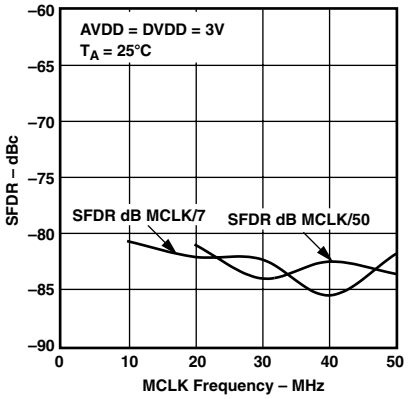
AD9834–Typical Performance Characteristics



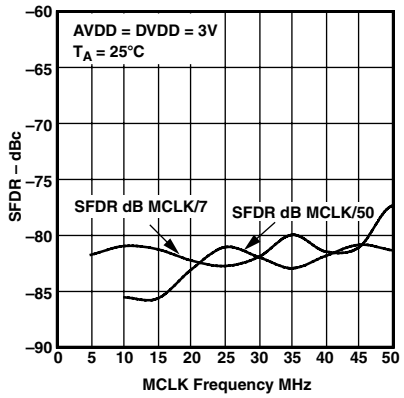
TPC 1. Typical Current Consumption vs. MCLK Frequency



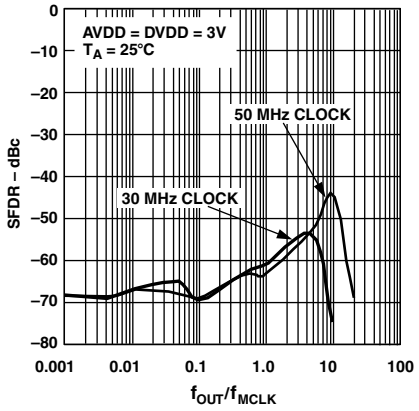
TPC 2. Typical I_{DD} vs. f_{OUT} for f_{MCLK} = 50 MHz



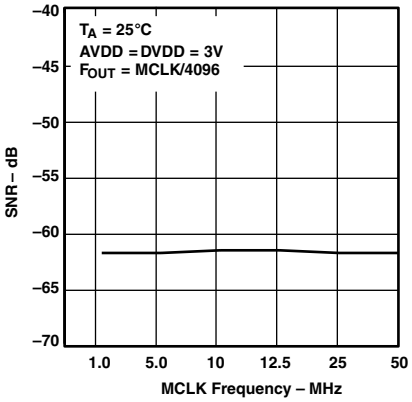
TPC 3. Narrow-Band SFDR vs. MCLK Frequency



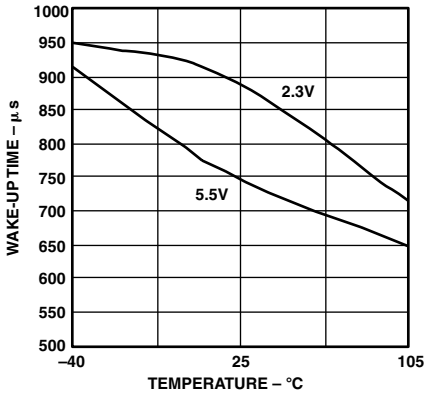
TPC 4. Wideband SFDR vs. MCLK Frequency



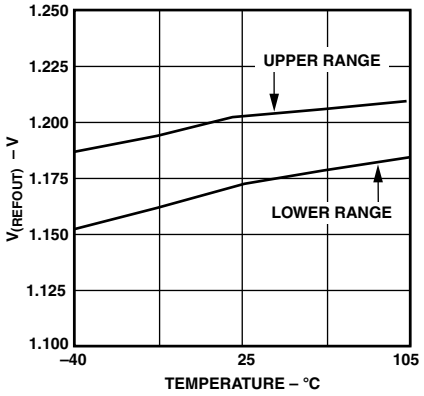
TPC 5. Wideband SFDR vs. f_{OUT}/f_{MCLK} for Various MCLK Frequencies



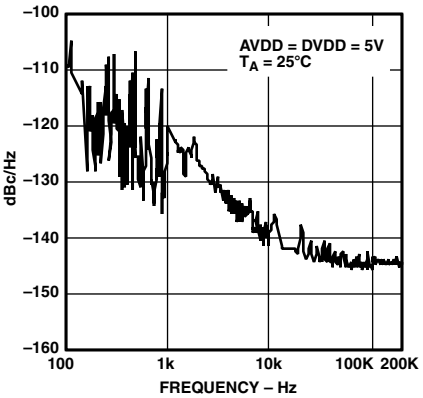
TPC 6. SNR vs. MCLK Frequency



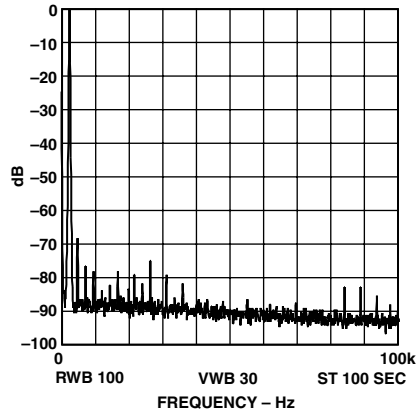
TPC 7. Wake-Up Time vs. Temperature



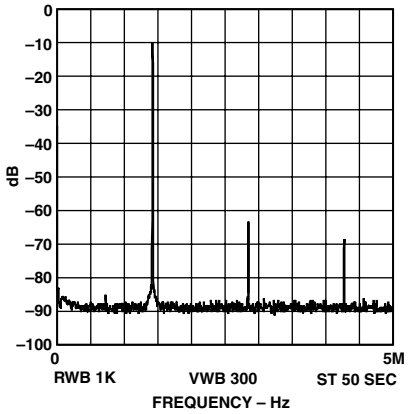
TPC 8. V_{REFOUT} vs. Temperature



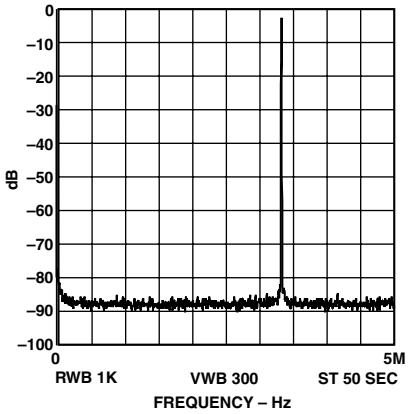
TPC 9. Output Phase Noise, f_{OUT} = 2 MHz, MCLK = 50 MHz



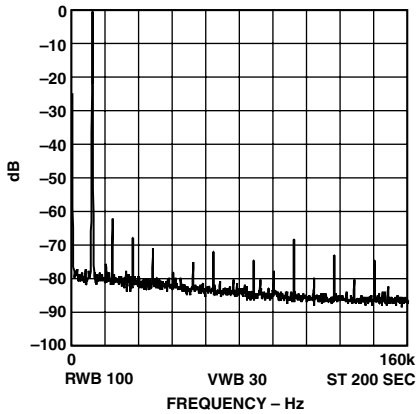
TPC 10. f_{MCLK} = 10 MHz; f_{OUT} = 2.4 kHz, Frequency Word = 000FBA9



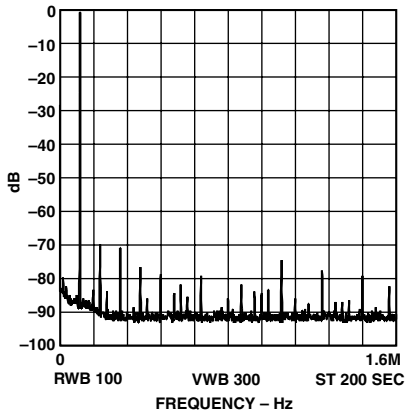
TPC 11. f_{MCLK} = 10 MHz; f_{OUT} = 1.43 MHz = f_{MCLK}/7, Frequency Word = 2492492



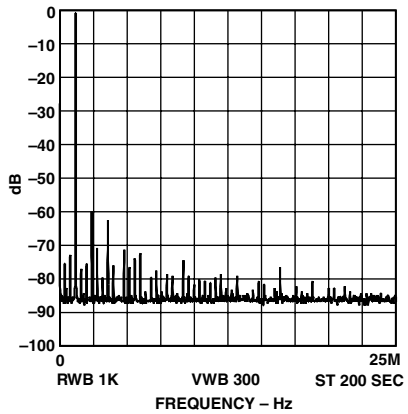
TPC 12. f_{MCLK} = 10 MHz; f_{OUT} = 3.33 MHz = f_{MCLK}/3, Frequency Word = 5555555



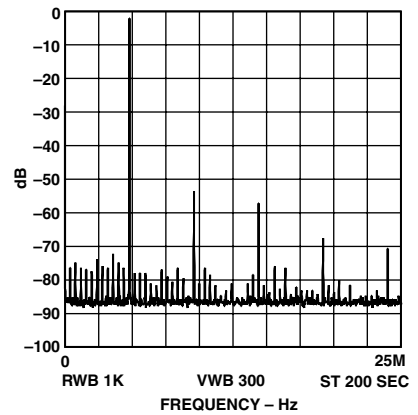
TPC 13. f_{MCLK} = 50 MHz; f_{OUT} = 12 kHz, Frequency Word = 000FBA9



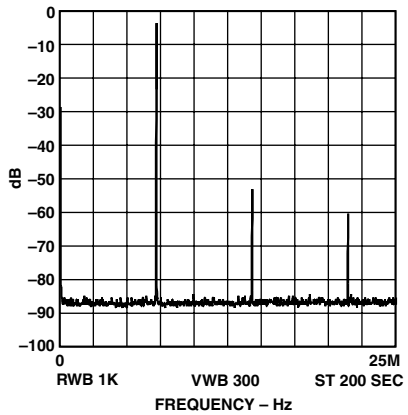
TPC 14. f_{MCLK} = 50 MHz; f_{OUT} = 120 kHz, Frequency Word = 009D496



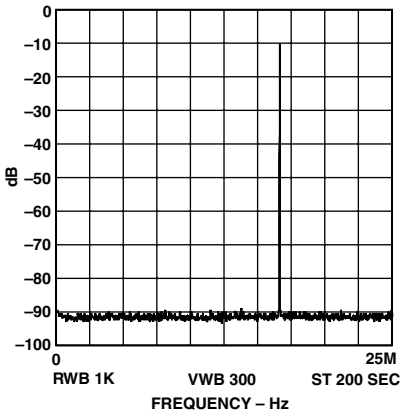
TPC 15. f_{MCLK} = 50 MHz; f_{OUT} = 1.2 MHz, Frequency Word = 0624DD3



TPC 16. f_{MCLK} = 50 MHz; f_{OUT} = 4.8 MHz, Frequency Word = 189374C



TPC 17. f_{MCLK} = 50 MHz; f_{OUT} = 7.143 MHz = f_{MCLK}/7, Frequency Word = 2492492



TPC 18. f_{MCLK} = 50 MHz; f_{OUT} = 16.667 MHz = f_{MCLK}/3, Frequency Word = 5555555

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale, a point 0.5 LSB below the first code transition (000 . . . 00 to 000 . . . 01) and full scale, a point 0.5 LSB above the last code transition (111 . . . 10 to 111 . . . 11). The error is expressed in LSBs.

Differential Nonlinearity
This is the difference between the measured and ideal 1 LSB change between two adjacent codes in the DAC. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity.

Output Compliance
The output compliance refers to the maximum voltage that can be generated at the output of the DAC to meet the specifications. When voltages greater than that specified for the output compliance are generated, the AD9834 may not meet the specifications listed in the data sheet.

Spurious-Free Dynamic Range
Along with the frequency of interest, harmonics of the fundamental frequency and images of these frequencies are present at the output of a DDS device. The spurious-free dynamic range (SFDR) refers to the largest spur or harmonic present in the band of interest. The wideband SFDR gives the magnitude of the largest harmonic or spur relative to the magnitude of the fundamental frequency in the "0" to Nyquist bandwidth. The narrow band SFDR gives the attenuation of the largest spur or harmonic in a bandwidth of ±200 kHz about the fundamental frequency.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the rms value of the fundamental. For the AD9834, *THD* is defined as:

$$THD = 20\ log\sqrt{\frac{V_2^{\ 2} + V_3^{\ 2} + V_4^{\ 2} + V_5^{\ 2} + V_6^{\ 2}}{V_1}}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency. The value for SNR is expressed in decibels.

Clock Feedthrough
There will be feedthrough from the MCLK input to the analog output. Clock feedthrough refers to the magnitude of the MCLK signal relative to the fundamental frequency in the AD9834's output spectrum.

THEORY OF OPERATION

Sine waves are typically thought of in terms of their magnitude form a(t) = sin (ωt). However, these are nonlinear and not easy to generate except through piecewise construction. On the other hand, the angular information is linear in nature. That is, the phase angle rotates through a fixed angle for each unit of time. The angular rate depends on the frequency of the signal by the traditional rate of $\omega = 2\pi f$.

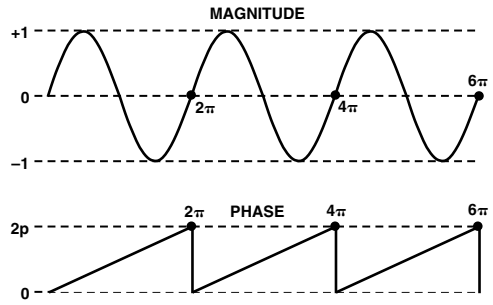


Figure 5. Sine Wave

Knowing that the phase of a sine wave is linear and given a reference interval (clock period), the phase rotation for that period can be determined.

$$\Delta Phase = \omega \Delta t$$

Solving for ω

$$\omega = \Delta Phase/\Delta t = 2\pi f$$

Solving for *f* and substituting the reference clock frequency for the reference period ($1/f_{MCLK} = \Delta t$)

$$f = \Delta Phase \times f_{MCLK}/2\pi$$

The AD9834 builds the output based on this simple equation. A simple DDS chip can implement this equation with three major subcircuits: Numerically Controlled Oscillator + Phase Modulator, SIN ROM, and Digital-to-Analog Convertor.

Each of these subcircuits is discussed in the following section.

CIRCUIT DESCRIPTION

The AD9834 is a fully integrated Direct Digital Synthesis (DDS) chip. The chip requires one reference clock, one low precision resistor, and eight decoupling capacitors to provide digitally created sine waves up to 25 MHz. In addition to the generation of this RF signal, the chip is fully capable of a broad range of simple and complex modulation schemes. These modulation schemes are fully implemented in the digital domain, allowing accurate and simple realization of complex modulation algorithms using DSP techniques.

The internal circuitry of the AD9834 consists of the following main sections: a Numerically Controlled Oscillator (NCO), Frequency and Phase Modulators, SIN ROM, a Digital-to-Analog Converter, a Comparator, and a Regulator.

Numerically Controlled Oscillator Plus Phase Modulator
This consists of two frequency select registers, a phase accumulator, two phase offset registers, and a phase offset adder. The main component of the NCO is a 28-bit phase accumulator. Continuous time signals have a phase range of 0 to 2π. Outside this range of numbers, the sinusoid functions repeat themselves in a periodic manner. The digital implementation is no different. The accumulator simply scales the range of phase numbers into a multibit digital word. The phase accumulator in the AD9834 is implemented with 28 bits. Therefore, in the AD9834, $2\pi = 2^{28}$. Likewise, the Δ*Phase* term is scaled into this range of numbers:
$0 < \Delta Phase < 2^{28} - 1$. Making these substitutions into the equation above

$$f = \Delta Phase \times f_{MCLK}/2^{28}$$

where $0 < \Delta Phase < 2^{28} - 1$.

The input to the phase accumulator can be selected either from the FREQ0 Register or FREQ1 Register, and is controlled by the FSELECT pin or the FSEL bit. NCOs inherently generate continuous phase signals, thus avoiding any output discontinuity when switching between frequencies.

Following the NCO, a phase offset can be added to perform phase modulation using the 12-bit phase registers. The contents of one of these phase registers is added to the most significant bits of the NCO. The AD9834 has two phase registers, the resolution of these registers being $2\pi/4096$.

SIN ROM

To make the output from the NCO useful, it must be converted from phase information into a sinusoidal value. Since phase information maps directly into amplitude, the SIN ROM uses the digital phase information as an address to a look-up table and converts the phase information into amplitude. Although the NCO contains a 28-bit phase accumulator, the output of the NCO is truncated to 12 bits. Using the full resolution of the phase accumulator is impractical and unnecessary as this would require a look-up table of 2^{28} entries. It is necessary only to have sufficient phase resolution such that the errors due to truncation are smaller than the resolution of the 10-bit DAC. This requires the SIN ROM to have two bits of phase resolution more than the 10-bit DAC.

The SIN ROM is enabled using bits MODE and OPBITEN in the control register. This is explained further in Table XIV.

Digital-to-Analog Converter

The AD9834 includes a high impedance current source 10-bit DAC capable of driving a wide range of loads. The full-scale output current can be adjusted for optimum power and external load requirements through the use of a single external resistor (R_{SET}).

The DAC can be configured for either single-ended or differential operation. IOUT and IOUTB can be connected through equal external resistors to AGND to develop complementary output voltages. The load resistors can be any value required, as long as the full-scale voltage developed across it does not exceed the voltage compliance range. Since full-scale current is controlled by R_{SET}, adjustments to R_{SET} can balance changes made to the load resistors.

Comparator

The AD9834 can be used to generate synthesized digital clock signals. This can be done by using the on-board self-biasing comparator, which converts the DAC's sinusoidal signal to a square wave. The output from the DAC may be filtered externally before being applied to the comparator input. The comparator reference voltage is the time average of the signal applied to V_{IN}. The comparator can accept signals in the range of approximately 100 mV p-p to 1 V p-p. As the comparator's input is ac-coupled, to operate correctly as a zero crossing detector, it requires a minimum input frequency of typically 3 MHz. The comparator's output will be a square wave with an amplitude from 0 V to DVDD.

To enable the comparator, bits SIGNPIB and OPBITEN in the control resister are set to "1." This is explained further in Table XIII.

Regulator

The AD9834 has separate power supplies for the analog and digital sections. AVDD provides the power supply required for the analog section, while DVDD provides the power supply for the digital section. Both of these supplies can have a value of 2.3 V to 5.5 V and are independent of each other, e.g., the analog section can be operated at 5 V, and the digital section can be operated at 3 V, or vice versa.

The internal digital section of the AD9834 is operated at 2.5 V. An on-board regulator steps down the voltage applied at DVDD to 2.5 V. The digital interface (serial port) of the AD9834 is also operated from DVDD. These digital signals are level shifted within the AD9834 to make them 2.5 V compatible.

When the applied voltage at the DVDD pin of the AD9834 is equal to or less than 2.7 V, the pins CAP/2.5V and DVDD should be tied together, thus bypassing the on-board regulator.

FUNCTIONAL DESCRIPTION

Serial Interface

The AD9834 has a standard 3-wire serial interface that is compatible with SPI, QSPI™, MICROWIRE™, and DSP interface standards.

Data is loaded into the device as a 16-bit word under the control of a serial clock input, SCLK. The timing diagram for this operation is given in Figure 4.

The FSYNC input is a level triggered input that acts as a frame synchronization and chip enable. Data can only be transferred into the device when FSYNC is low. To start the serial data transfer, FSYNC should be taken low, observing the minimum FSYNC to SCLK falling edge setup time, t_7. After FSYNC goes low, serial data will be shifted into the device's input shift register on the falling edges of SCLK for 16 clock pulses. FSYNC may be taken high after the 16th falling edge of SCLK, observing the minimum SCLK falling edge to FSYNC rising edge time, t_8. Alternatively, FSYNC can be kept low for a multiple of 16 SCLK pulses and then brought high at the end of the data transfer. In this way, a continuous stream of 16-bit words can be loaded while FSYNC is held low, with FSYNC only going high after the 16th SCLK falling edge of the last word is loaded.

The SCLK can be continuous, or alternatively, the SCLK can idle high or low between write operations but must be high when FSYNC goes low (t_{12}).

Powering up the AD9834

The flow chart in Figure 8 shows the operating routine for the AD9834. When the AD9834 is powered up, the part should be reset. This will reset appropriate internal registers to "0" to provide an analog output of midscale. To avoid spurious DAC outputs while the AD9834 is being initialized, the RESET bit/pin should be set to "1" until the part is ready to begin generating an output. RESET does not reset the phase, frequency, or control registers. These registers will contain invalid data, and therefore should be set to a known value by the user. The RESET bit/pin should then be set to "0" to begin generating an output. The data will appear on the DAC output eight MCLK cycles after RESET is set to "0."

Latency

Associated with each operation is a latency. When the pins FSELECT and PSELECT change value, there is a pipeline delay before control is transferred to the selected register. When the timing specifications t_{11} and t_{11A} are met (see Figure 3), FSELECT and PSELECT have latencies of eight MCLK cycles. When the timing specifications t_{11} and t_{11A} are not met, the latency is increased by one MCLK cycle.

Similarly, there is a latency associated with each asynchronous write operation. If a selected frequency/phase register is loaded with a new word, there is a delay of eight to nine MCLK cycles before the analog output will change. (There is an uncertainty of one MCLK cycle as it depends on the position of the MCLK rising edge when the data is loaded into the destination register.)

The negative transition of the RESET and SLEEP functions are sampled on the internal falling edge of MCLK, therefore they also have a latency associated with them.

The Control Register

The AD9834 contains a 16-bit control register that sets up the AD9834 as the user wishes to operate it. All control bits, except MODE, are sampled on the internal negative edge of MCLK.

Table II describes the individual bits of the control register. The different functions and the various output options from the AD9834 are described in more detail in the section following Table II.

To inform the AD9834 that the contents of the control register will be alterred, D15 and D14 must be set to "0" as shown below.

Table I. Control Register

D15	D14	D13 D0
0	0	CONTROL BITS

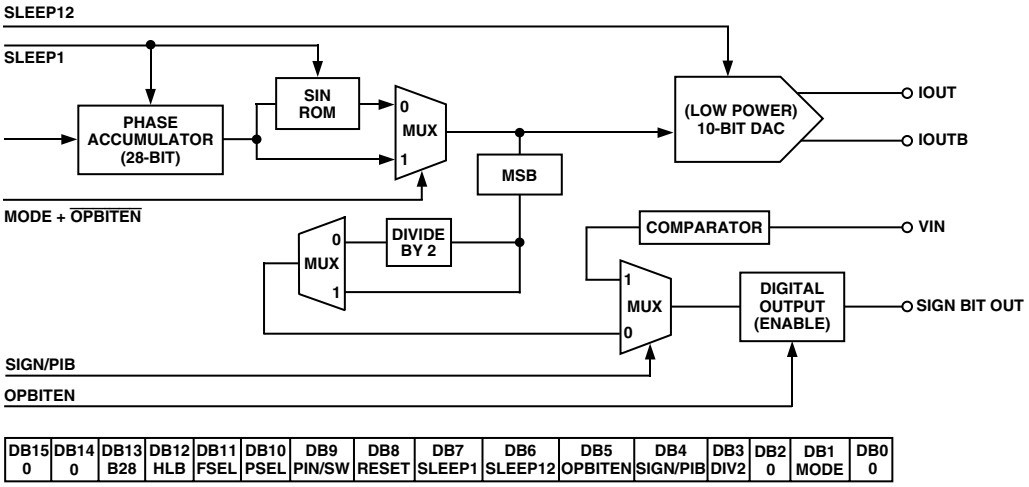


Figure 6. Function of Control Bits

Table II. Description of Bits in the Control Register

Bit	Name	Function
D13	B28	Two write operations are required to load a complete word into either of the frequency registers. B28 = 1 allows a complete word to be loaded into a frequency register in two consecutive writes. The first write contains the 14 LSBs of the frequency word and the next write will contain the 14 MSBs. The first 2 bits of each 16-bit word define the frequency register to which the word is loaded and should, therefore, be the same for both of the consecutive writes. Refer to Table VI for the appropriate addresses. The write to the frequency register occurs after both words have been loaded, so the register never holds an intermediate value. An example of a complete 28-bit write is shown in Table VII. When B28 = 0, the 28-bit frequency register operates as two 14-bit registers, one containing the 14 MSBs and the other containing the 14 LSBs. This means that the 14 MSBs of the frequency word can be altered independent of the 14 LSBs and vice versa. To alter the 14 MSBs or the 14 LSBs, a single write is made to the appropriate frequency address. The control bit D12 (HLB) informs the AD9834 whether the bits to be altered are the 14 MSBs or 14 LSBs.
D12	HLB	This control bit allows the user to continuously load the MSBs or LSBs of a frequency register while ignoring the remaining 14 bits. This is useful if the complete 28-bit resolution is not required. HLB is used in conjunction with D13 (B28). This control bit indicates whether the 14 bits being loaded are being transferred to the 14 MSBs or 14 LSBs of the addressed frequency register. D13 (B28) must be set to "0" to be able to change the MSBs and LSBs of a frequency word separately. When D13 (B28) = 1, this control bit is ignored. HLB = 1 allows a write to the 14 MSBs of the addressed frequency register. HLB = 0 allows a write to the 14 LSBs of the addressed frequency register.
D11	FSEL	The FSEL bit defines whether the FREQ0 Register or the FREQ1 Register is used in the phase accumulator. See Table IV on selecting a frequency register.

Table II. Description of Bits in the Control Register (continued)

Bit	Name	Function
D10	PSEL	The PSEL bit defines whether the PHASE0 Register or the PHASE1 Register data is added to the output of the phase accumulator. See Table V on selecting a phase register.
D9	PIN/SW	Functions that select frequency and phase registers, reset internal registers, and power down the DAC can be implemented using either software or hardware. PIN/SW selects the source of control for these functions. PIN/SW = 1 implies that the functions are being controlled using the appropriate control pins. PIN/SW = 0 implies that the functions are being controlled using the appropriate control bits.
D8	RESET	RESET = 1 resets internal registers to "0," which corresponds to an analog output of midscale. RESET = 0 disables RESET. This function is explained further in Table XI.
D7	SLEEP1	When SLEEP1 = 1, the internal MCLK clock is disabled. The DAC output will remain at its present value as the NCO is no longer accumulating. When SLEEP1 = 0, MCLK is enabled. This function is explained further in Table XII.
D6	SLEEP12	SLEEP12 = 1 powers down the on-chip DAC. This is useful when the AD9834 is used to output the MSB of the DAC data. SLEEP12 = 0 implies that the DAC is active. This function is explained further in Table XII.
D5	OPBITEN	The function of this bit is to control whether there is an output at the pin SIGN BIT OUT. This bit should remain at "0" if the user is not using the pin SIGN BIT OUT. OPBITEN = 1 enables the pin SIGN BIT OUT. When OPBITEN equals "0," the SIGN BIT OUT output buffer is put into a high impedance state, and therefore no output is available at the SIGN BIT OUT pin.
D4	SIGNPIB	The function of this bit is to control what is output at the pin SIGN BIT OUT. When SIGNPIB = 1, the on-board comparator is connected to SIGN BIT OUT. After filtering the sinusoidal output from the DAC, the waveform can be applied to the comparator to generate a square waveform. This is explained further in Table XIII. When SIGNPIB = 0, the MSB (or MSB/2) of the DAC data is connected to the pin SIGN BIT OUT. The bit DIV2 controls whether it is the MSB or MSB/2 that is output.
D3	DIV2	DIV2 is used in association with SIGNPIB and OPBITEN. This is fully explained in Table XIII. When DIV2 = 1, the digital output is passed directly to the SIGN BIT OUT pin. When DIV2 = 0, the digital output/2 is passed directly to the SIGN BIT OUT pin.
D2	Reserved	This bit must always be set to "0."
D1	MODE	The function of this bit is to control what is output at the IOUT/IOUTB pins. This bit should be set to "0" if the control bit OPBITEN = 1. When MODE = 1, the SIN ROM is bypassed, resulting in a triangle output from the DAC. When MODE = 0, the SIN ROM is used to convert the phase information into amplitude information, which results in a sinusoidal signal at the output (see Table XIV).
D0	Reserved	This bit must always be set to "0."

The Frequency and Phase Registers

The AD9834 contains two frequency registers and two phase registers. These are described in Table III.

Table III. Frequency/Phase Registers

Register	Size	Description
FREQ0	28 Bits	Frequency Register "0." When FSEL bit or FSELECT pin = 0, this register defines the output frequency as a fraction of the MCLK frequency.
FREQ1	28 Bits	Frequency Register "1." When FSEL bit or FSELECT pin = 1, this register defines the output frequency as a fraction of the MCLK frequency.
PHASE0	12 Bits	Phase Offset Register "0." When PSEL bit or PSELECT pin = 0, the contents of this register are added to the output of the phase accumulator.
PHASE1	12 Bits	Phase Offset Register "1." When PSEL bit or PSELECT pin = 1, the contents of this register are added to the output of the phase accumulator.

The analog output from the AD9834 is:

$$f_{MCLK}/2^{28} \times FREQREG$$

where *FREQREG* is the value loaded into the selected frequency register. This signal will be phase shifted by

$$2\pi/4096 \times PHASEREG$$

where *PHASEREG* is the value contained in the selected phase register. Consideration must be given to the relationship of the selected output frequency and the reference clock frequency to avoid unwanted output anomalies.

Access to the frequency and phase registers is controlled by both the FSELECT/PSELECT pins and the FSEL/PSEL control bits. If the control bit PIN/SW = 1, the pins control the function; whereas, if PIN/SW = 0, the bits control the function. This is outlined in Tables IV and V. If the FSEL/PSEL bits are being used, the pins should preferably be held at CMOS logic high or low. Control of the frequency/phase registers can be interchanged from the pins to the bits.

Table IV. Selecting a Frequency Register

FSELECT	FSEL	PIN/SW	Selected Register
0	X	1	FREQ0 REG
1	X	1	FREQ1 REG
X	0	0	FREQ0 REG
X	1	0	FREQ1 REG

Table V. Selecting a Phase Register

PSELECT	PSEL	PIN/SW	Selected Register
0	X	1	PHASE0 REG
1	X	1	PHASE1 REG
X	0	0	PHASE0 REG
X	1	0	PHASE1 REG

The FSELECT and PSELECT pins are sampled on the internal falling edge of MCLK. It is recommended that the data on these pins does not change within a time window of the falling edge of MCLK (see Figure 3 for timing). If FSELECT/PSELECT changes value when a falling edge occurs, there is an uncertainty of one MCLK cycle as to when control is transferred to the other frequency/phase register.

The flow charts in Figures 9 and 10 show the routine for selecting and writing to the frequency and phase registers of the AD9834.

Writing to a Frequency Register

When writing to a frequency register, Bits D15 and D14 give the address of the frequency register.

Table VI. Frequency Register Bits

D15	D14	D13	D0
0	1	14 FREQ0 REG BITS	
1	0	14 FREQ1 REG BITS	

If the user wishes to alter the entire contents of a frequency register, two consecutive writes to the same address must be performed, as the frequency registers are 28 bits wide. The first write will contain the 14 LSBs, while the second write will contain the 14 MSBs. For this mode of operation, the control bit B28 (D13) should be set to "1." An example of a 28-bit write is shown in Table VII.

Table VII. Writing FFFC000 to FREQ0 REG

SDATA Input	Result of Input Word
0010 0000 0000 0000	Control Word Write (D15, D14 = 00), B28 (D13) = 1, HLB (D12) = X
0100 0000 0000 0000	FREQ0 REG Write (D15, D14 = 01), 14 LSBs = 0000
0111 1111 1111 1111	FREQ0 REG Write (D15, D14 = 01), 14 MSBs = 3FFF

In some applications, the user does not need to alter all 28 bits of the frequency register. With coarse tuning, only the 14 MSBs are altered, while with fine tuning only the 14 LSBs are altered. By setting the control bit B28 (D13) to "0," the 28-bit frequency register operates as two 14-bit registers, one containing the 14 MSBs and the other containing the 14 LSBs. This means that the 14 MSBs of the frequency word can be altered independent of the 14 LSBs, and vice versa. Bit HLB (D12) in the control register identifies which 14 bits are being altered. Examples of this are shown in Tables VIII and IX.

Table VIII. Writing 3FFF to the 14 LSBs of FREQ1 REG

SDATA Input	Result of Input Word
0000 0000 0000 0000	Control Word Write (D15, D14 = 00), B28 (D13) = 0, HLB (D12) = 0, i.e., LSBs
1011 1111 1111 1111	FREQ1 REG Write (D15, D14 = 10), 14 LSBs = 3FFF

Table IX. Writing 00FF to the 14 MSBs of FREQ0 REG

SDATA Input	Result of Input Word
0001 0000 0000 0000	Control Word Write (D15, D14 = 00), B28 (D13) = 0, HLB (D12) = 1, i.e., MSBs
0100 0000 1111 1111	FREQ0 REG Write (D15, D14 = 01), 14 MSBs = 00FF

Writing to a Phase Register

When writing to a phase register, bits D15 and D14 are set to 11. Bit D13 identifies which phase register is being loaded.

Table X. Phase Register Bits

D15	D14	D13	D12	D11		D0
1	1	0	X	MSB	12 PHASE0 BITS	LSB
1	1	1	X	MSB	12 PHASE1 BITS	LSB

The RESET Function

The RESET function resets appropriate internal registers to "0" to provide an analog output of midscale. RESET does not reset the phase, frequency, or control registers.

When the AD9834 is powered up, the part should be reset. To reset the AD9834, set the RESET pin/bit to "1." To take the part out of reset, set the pin/bit to "0." A signal will appear at the DAC output seven MCLK cycles after RESET is set to "0."

The RESET function is controlled by both the RESET pin and the RESET control bit. If the control bit PIN/SW = 0, the RESET bit controls the function, whereas if PIN/SW = 1, the pin controls the function.

Table XI. Applying RESET

RESET Pin	RESET Bit	PIN/SW	Result
0	X	1	No Reset Applied
1	X	1	Internal Registers Reset
X	0	0	No Reset Applied
X	1	0	Internal Registers Reset

The effect of asserting the RESET pin is seen immediately at the output, i.e., the zero to one transition of this pin is not sampled. However, the negative transition of RESET is sampled on the internal falling edge of MCLK.

The SLEEP Function

Sections of the AD9834 that are not in use can be powered down to minimize power consumption. This is done using the SLEEP function. The parts of the chip that can be powered down are the internal clock and the DAC. The DAC can be powered down through hardware or software. The pin/bits required for the SLEEP function are outlined in Table XII.

Table XII. Applying the SLEEP Function

SLEEP Pin	SLEEP1 Bit	SLEEP12 Bit	PIN/SW Bit	Result
0	X	X	1	No Power-Down
1	X	X	1	DAC Powered Down
X	0	0	0	No Power-Down
X	0	1	0	DAC Powered Down
X	1	0	0	Internal Clock Disabled
X	1	1	0	Both the DAC Powered Down and the Internal Clock Disabled

DAC Powered Down

This is useful when the AD9834 is used to output the MSB of the DAC data only. In this case, the DAC is not required so it can be powered down to reduce power consumption.

Internal Clock Disabled

When the internal clock of the AD9834 is disabled, the DAC output will remain at its present value as the NCO is no longer accumulating. New frequency, phase, and control words can be written to the part when the SLEEP1 control bit is active. The synchronizing clock is still active which means that the selected frequency and phase registers can also be changed either at the pins or by using the control bits. Setting the SLEEP1 bit to "0" enables the MCLK. Any changes made to the registers while SLEEP1 was active will be seen at the output after a certain latency.

The effect of asserting the SLEEP pin is seen immediately at the output, i.e., the zero to one transition of this pin is not sampled. However, the negative transition of SLEEP is sampled on the internal falling edge of MCLK.

The SIGN BIT OUT Pin

The AD9834 offers a variety of outputs from the chip. The digital outputs are available from the SIGN BIT OUT pin. The available outputs are the comparator output or the MSB of the DAC data. The bits controlling the SIGN BIT OUT pin are outlined in Table XIII.

This pin must be enabled before use. The enabling/disabling of this pin is controlled by the bit OPBITEN (D5) in the control register. When OPBITEN = 1, this pin is enabled. Note that the MODE bit (D1) in the control register should be set to "0" if OPBITEN = 1.

Comparator Output

The AD9834 has an on-board comparator. To connect this comparator to the SIGN BIT OUT pin, the SIGNPIB (D4) control bit must be set to "1." After filtering the sinusoidal output from the DAC, the waveform can be applied to the comparator to generate a square waveform.

MSB from the NCO

The MSB from the NCO can be output from the AD9834. By setting the SIGNPIB (D4) control bit to "0," the MSB of the DAC data is available at the SIGN BIT OUT pin. This is useful as a coarse clock source. This square wave can also be divided by two before being output. The bit DIV2 (D3) in the control register controls the frequency of this output from the SIGN BIT OUT pin.

Table XIII. Various Outputs from SIGN BIT OUT

OPBITEN Bit	MODE Bit	SIGNPIB Bit	DIV2 Bit	SIGN BIT OUT Pin
0	X	X	X	High Impedance
1	0	0	0	DAC Data MSB/2
1	0	0	1	DAC Data MSB
1	0	1	0	Reserved
1	0	1	1	Comparator Output
1	1	X	X	Reserved

The IOUT/IOUTB Pins

The analog outputs from the AD9834 are available from the IOUT/IOUTB pins. The available outputs are a sinusoidal output or a triangle output.

Sinusoidal Output

The SIN ROM is used to convert the phase information from the frequency and phase registers into amplitude information, which results in a sinusoidal signal at the output. To have a sinusoidal output from the IOUT/IOUTB pins, set the bit MODE (D1) = 0.

Triangle Output

The SIN ROM can be bypassed so that the truncated digital output from the NCO is sent to the DAC. In this case, the output is no longer sinusoidal. The DAC will produce 10-bit linear triangular function. To have a triangle output from the IOUT/IOUTB pins, set the bit MODE (D1) = 1.

Note that the SLEEP pin/SLEEP12 bit must be "0" (i.e., the DAC is enabled) when using these pins.

Table XIV. Various Outputs from IOUT/IOUTB

OPBITEN Bit	MODE Bit	IOUT/IOUTB Pins
0	0	Sinusoid
0	1	Triangle
1	0	Sinusoid
1	1	Reserved

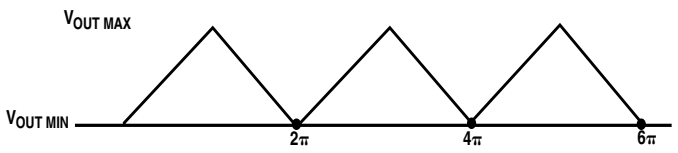


Figure 7. Triangle Output

APPLICATIONS

Because of the various output options available from the part, the AD9834 can be configured to suit a wide variety of applications.

One of the areas where the AD9834 is suitable is in modulation applications. The part can be used to perform simple modulation such as FSK. More complex modulation schemes such as GMSK and QPSK can also be implemented using the AD9834.

In an FSK application, the two frequency registers of the AD9834 are loaded with different values. One frequency will represent the space frequency, while the other will represent the mark frequency. The digital data stream is fed to the FSELECT pin, which will cause the AD9834 to modulate the carrier frequency between the two values.

The AD9834 has two phase registers; this enables the part to perform PSK. With phase shift keying, the carrier frequency is phase shifted, the phase being altered by an amount that is related to the bit stream being input to the modulator.

The AD9834 is also suitable for signal generator applications. With the on-board comparator, the device can be used to generate a square wave.

With its low current consumption, the part is suitable for applications in which it can be used as a local oscillator.

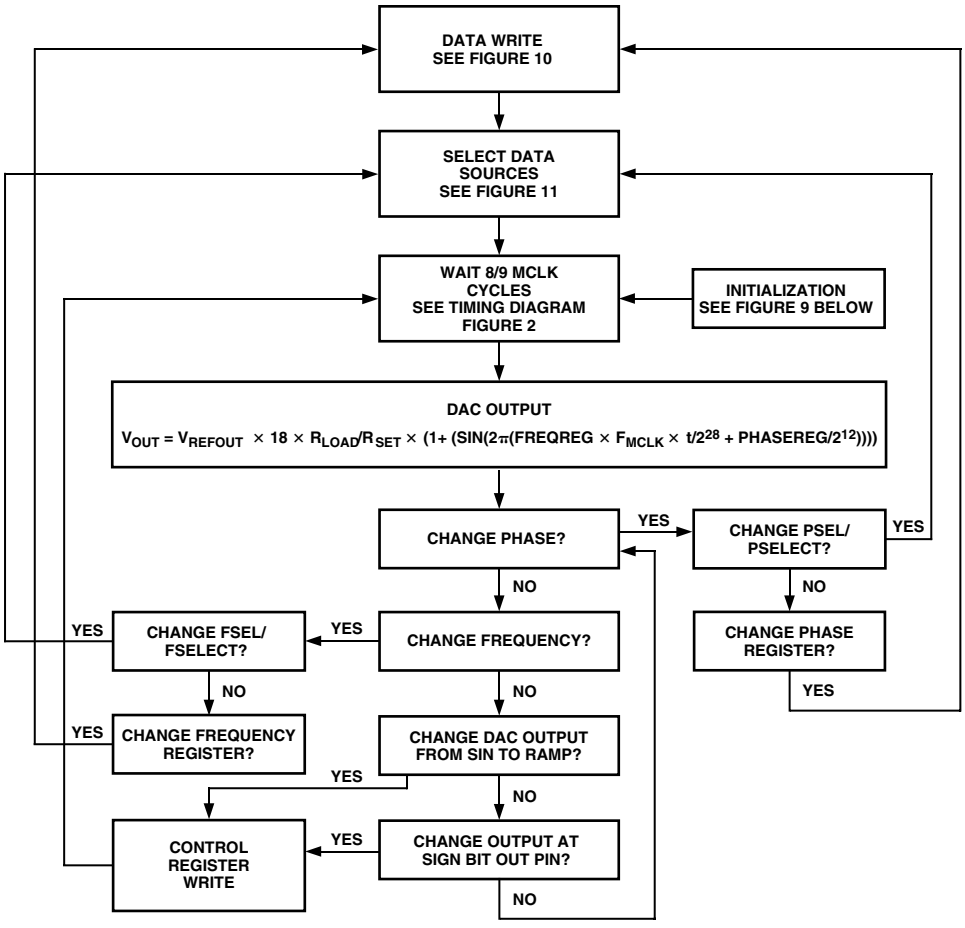


Figure 8. Flow Chart for Initialization and Operation

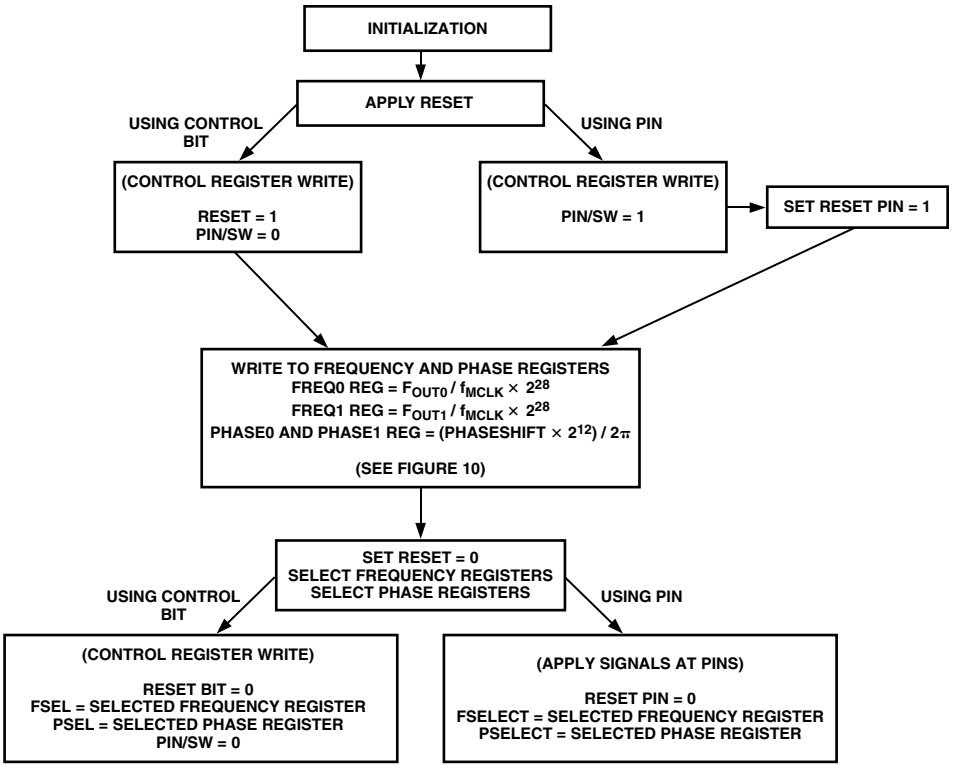


Figure 9. Initialization

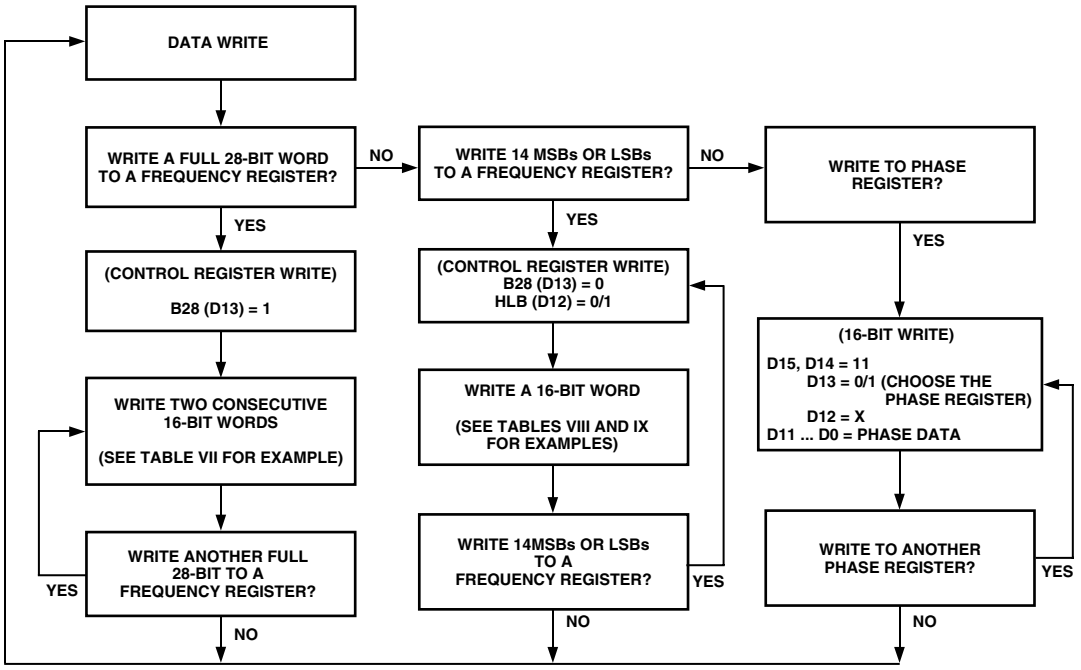


Figure 10. Data Writes

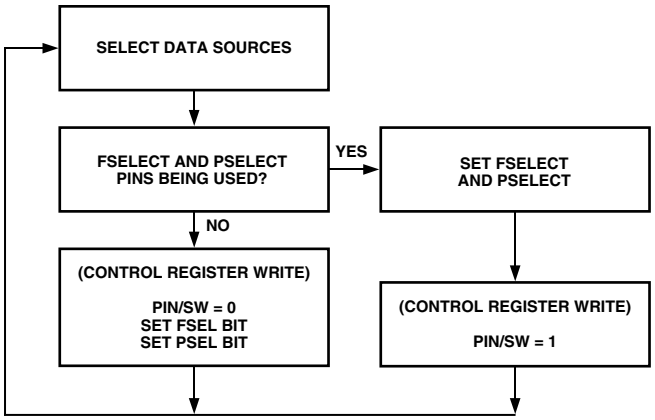


Figure 11. Selecting Data Sources

GROUNDING AND LAYOUT

The printed circuit board that houses the AD9834 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally best for ground planes since it gives the best shielding. Digital and analog ground planes should only be joined in one place. If the AD9834 is the only device requiring an AGND to DGND connection, then the ground planes should be connected at the AGND and DGND pins of the AD9834. If the AD9834 is in a system where multiple devices require AGND to DGND connections, the connection should be made at one point only, a star ground point that should be established as close as possible to the AD9834.

Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD9834 to avoid noise coupling. The power supply lines to the AD9834 should use as large a track as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the other side.

Good decoupling is important. The analog and digital supplies to the AD9834 are independent and separately pinned out to minimize coupling between analog and digital sections of the device. All analog and digital supplies should be decoupled to AGND and DGND, respectively, with 0.1 µF ceramic capacitors in parallel with 10 µF tantalum capacitors. To achieve the best from the decoupling capacitors, they should be placed as close as possible to the device, ideally right up against the device. In systems where a common supply is used to drive both the AVDD and DVDD of the AD9834, it is recommended that the system's AVDD supply be used. This supply should have the recommended analog supply decoupling between the AVDD pins of the AD9834 and AGND, and the recommended digital supply decoupling capacitors between the DVDD pins and DGND.

Proper operation of the comparator requires good layout strategy. The strategy must minimize the parasitic capacitance between V_{IN} and the SIGN BIT OUT pin by adding isolation using a ground plane. For example, in a multilayered board, the V_{IN} signal could be connected to the top layer and the SIGN BIT OUT connected to the bottom layer, so that isolation is provided by the power and ground planes between.

INTERFACING TO MICROPROCESSORS

The AD9834 has a standard serial interface that allows the part to interface directly with several microprocessors. The device uses an external serial clock to write the data/control information into the device. The serial clock can have a frequency of 40 MHz maximum. The serial clock can be continuous, or it can idle high or low between write operations. When data/control information is being written to the AD9834, FSYNC is taken low and is held low while the 16 bits of data are being written into the AD9834. The FSYNC signal frames the 16 bits of information being loaded into the AD9834.

AD9834 to ADSP-21xx Interface

Figure 12 shows the serial interface between the AD9834 and the ADSP-21xx. The ADSP-21xx should be set up to operate in the SPORT Transmit Alternate Framing Mode (TFSW = 1). The ADSP-21xx is programmed through the SPORT control register and should be configured as follows:

- Internal clock operation (ISCLK = 1)
- Active low framing (INVTFS = 1)
- 16-bit word length (SLEN = 15)
- Internal frame sync signal (ITFS = 1)
- Generate a frame sync for each write (TFSR = 1)

Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. The data is clocked out on each rising edge of the serial clock and clocked into the AD9834 on the SCLK falling edge.

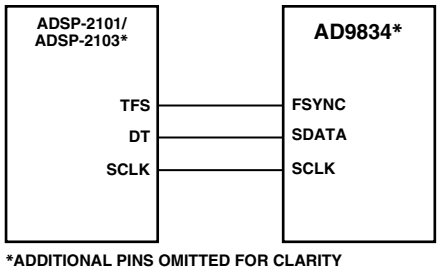


Figure 12. ADSP-2101/ADSP-2103 to AD9834 Interface

AD9834 to 68HC11/68L11 Interface

Figure 13 shows the serial interface between the AD9834 and the 68HC11/68L11 microcontroller. The microcontroller is configured as the master by setting bit MSTR in the SPCR to "1," which provides a serial clock on SCK while the MOSI output drives the serial data line SDATA. Since the microcontroller does not have a dedicated frame sync pin, the FSYNC signal is derived from a port line (PC7). The setup conditions for correct operation of the interface are as follows:

- SCK idles high between write operations (CPOL = 0).
- Data is valid on the SCK falling edge (CPHA = 1).

When data is being transmitted to the AD9834, the FSYNC line is taken low (PC7). Serial data from the 68HC11/68L11 is

transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. In order to load data into the AD9834, PC7 is held low after the first 8 bits are transferred and a second serial write operation is performed to the AD9834. Only after the second 8 bits have been transferred should FSYNC be taken high again.

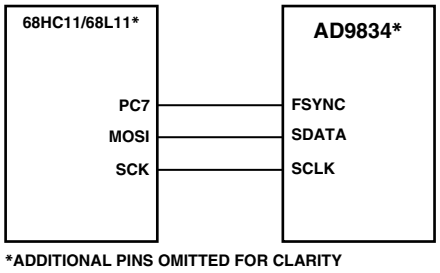


Figure 13. 68HC11/68L11 to AD9834 Interface

AD9834 to 80C51/80L51 Interface

Figure 14 shows the serial interface between the AD9834 and the 80C51/80L51 microcontroller. The microcontroller is operated in mode "0" so that TXD of the 80C51/80L51 drives SCLK of the AD9834, while RXD drives the serial data line SDATA. The FSYNC signal is again derived from a bit programmable pin on the port (P3.3 being used in the diagram). When data is to be transmitted to the AD9834, P3.3 is taken low. The 80C51/80L51 transmits data in 8-bit bytes, thus only eight falling SCLK edges occur in each cycle. To load the remaining 8 bits to the AD9834, P3.3 is held low after the first 8 bits have been transmitted, and a second write operation is initiated to transmit the second byte of data. P3.3 is taken high following the completion of the second write operation. SCLK should idle high between the two write operations. The 80C51/80L51 outputs the serial data in a format that has the LSB first. The AD9834 accepts the MSB first (the 4 MSBs being the control information, the next 4 bits being the address while the 8 LSBs contain the data when writing to a destination register). Therefore, the transmit routine of the 80C51/80L51 must take this into account and rearrange the bits so that the MSB is output first.

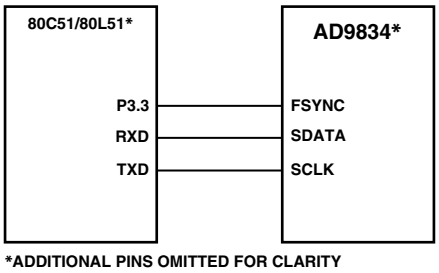


Figure 14. 80C51/80L51 to AD9834 Interface

AD9834 to DSP56002 Interface

Figure 15 shows the interface between the AD9834 and the DSP56002. The DSP56002 is configured for normal mode asynchronous operation with a gated internal clock (SYN = 0, GCK = 1, SCKD = 1). The frame sync pin is generated internally (SC2 = 1), the transfers are 16 bits wide (WL1 = 1, WL0 = 0), and the frame sync signal will frame the 16 bits (FSL = 0). The frame sync signal is available on pin SC2, but needs to be inverted before being applied to the AD9834. The interface to the DSP56000/DSP56001 is similar to that of the DSP56002.

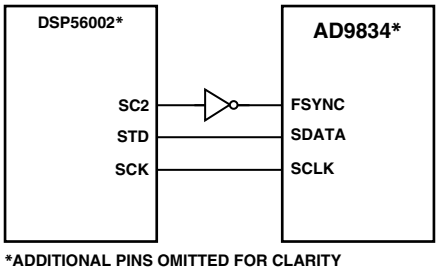


Figure 15. DSP56002 to AD9834 Interface

AD9834 EVALUATION BOARD

The AD9834 evaluation board allows designers to evaluate the high performance AD9834 DDS modulator with a minimum of effort.

To prove that this device will meet the user's waveform synthesis requirements, the user only requires a power supply, an IBM compatible PC, and a spectrum analyzer along with the evaluation board.

The DDS evaluation kit includes a populated, tested AD9834 printed circuit board. The evaluation board interfaces to the parallel port of an IBM compatible PC. Software is available with the evaluation board that allows the user to easily program the AD9834. A schematic of the evaluation board is shown in Figure 15. The software will run on any IBM compatible PC that has Microsoft WIN95™, WIN98™, Windows ME™, or Windows 2000 NT™ installed.

Using the AD9834 Evaluation Board

The AD9834 evaluation kit is a test system designed to simplify the evaluation of the AD9834. An application note is also available with the evaluation board and gives full information on operating the evaluation board.

Prototyping Area

An area is available on the evaluation board for the user to add additional circuits to the evaluation test set. Users may want to build custom analog filters for the output or add buffers and operational amplifiers to be used in the final application.

XO vs. External Clock

The AD9834 can operate with master clocks up to 50 MHz. A 50 MHz oscillator is included on the evaluation board. However, this oscillator can be removed and, if required, an external CMOS clock connected to the part.

Power Supply

Power to the AD9834 evaluation board must be provided externally through pin connections. The power leads should be twisted to reduce ground loops.

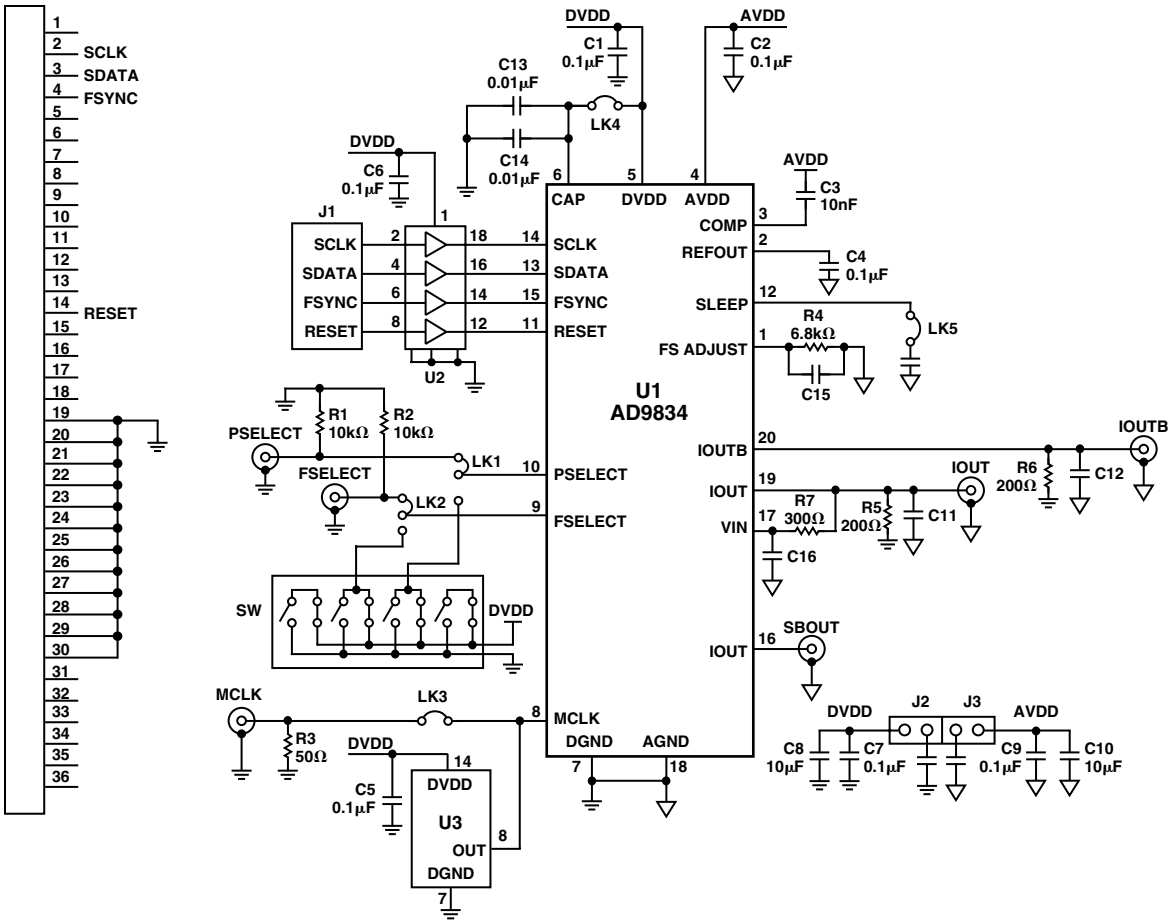


Figure 16. Evaluation Board Layout

Integrated Circuits

U3	OSC XTAL 50 MHz
U1	AD9834BRU
U2	74HCT244

Capacitors

C1, C2, C5, C6, C7, C9, C14	100 nF Ceramic Capacitor
C3, C4, C13	10 nF Ceramic Capacitor
C8, C10	10 µF Tantalum Capacitor
C11, C12, C15, C16	Option for Extra Decoupling Capacitors

Resistors

R1, R2	10 kΩ Resistor
R3	50 Ω Resistor
R4	6.8 kΩ Resistor
R5, R6	200 Ω Resistor
R7	300 Ω Resistor

Links

LK1, LK2, LK5	3-Pin Sil Header
LK3, LK4	2-Pin Sil Header

Switch

SW	End Stackable Switch (SDC Double Throw)

Sockets

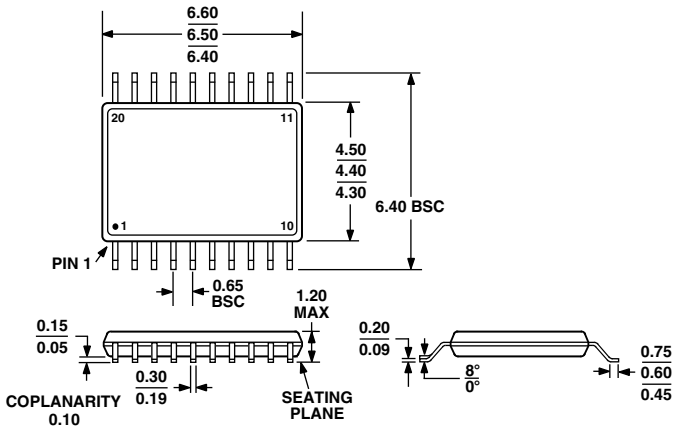
PSEL1, FSEL1, CLK1	Subminiature BNC
IOUT, IOUTB, SBOUT	Connector

Connectors

J1	36-Pin Edge Connector
J2, J3	PCB Mounting Terminal Block

OUTLINE DIMENSIONS

20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters



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