

# SN54HC373, SN74HC373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS140B – DECEMBER 1982 – REVISED MAY 1997

- Eight High-Current Latches in a Single Package
- High-Current 3-State True Outputs Can Drive up to 15 LSTTL Loads
- Full Parallel Access for Loading
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

## description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

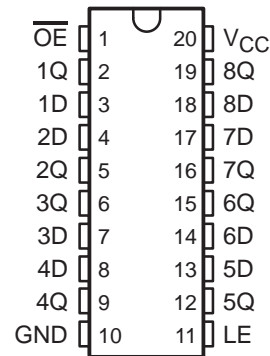
The eight latches of the 'HC373 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

An output-enable ( $\overline{OE}$ ) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

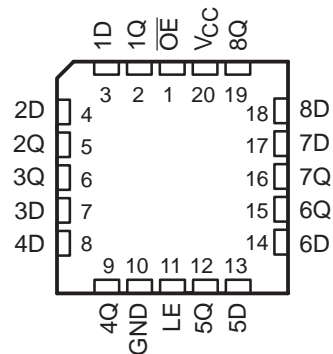
$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54HC373 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74HC373 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54HC373 . . . J OR W PACKAGE  
SN74HC373 . . . DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



SN54HC373 . . . FK PACKAGE  
(TOP VIEW)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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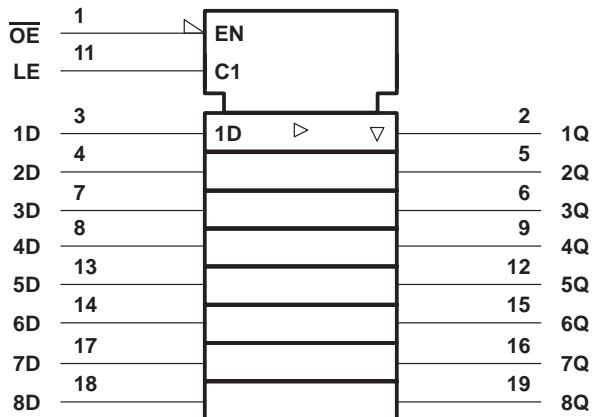
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FUNCTION TABLE  
(each latch)

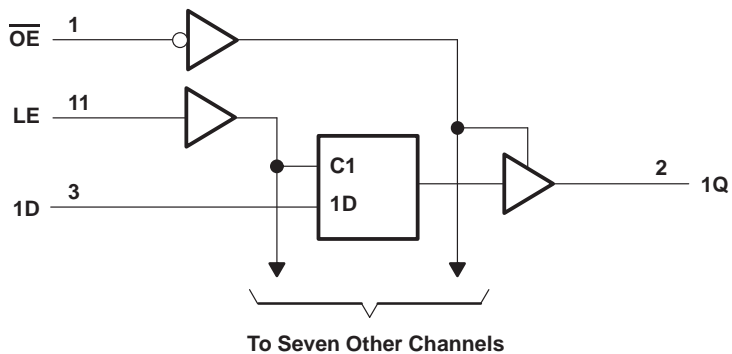
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



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## absolute maximum ratings over operating free-air temperature range†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1) .....	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1) .....	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±35 mA
Continuous current through $V_{CC}$ or GND .....	±70 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package .....	115°C/W
DW package .....	97°C/W
N package .....	67°C/W
PW package .....	128°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions

		SN54HC373			SN74HC373			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	2	5	6	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$		1.5	$V_{CC} = 2\text{ V}$		1.5	V
		$V_{CC} = 4.5\text{ V}$		3.15	$V_{CC} = 4.5\text{ V}$		3.15	
		$V_{CC} = 6\text{ V}$		4.2	$V_{CC} = 6\text{ V}$		4.2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$		0	0.5	$V_{CC} = 2\text{ V}$		V
		$V_{CC} = 4.5\text{ V}$		0	1.35	$V_{CC} = 4.5\text{ V}$		
		$V_{CC} = 6\text{ V}$		0	1.8	$V_{CC} = 6\text{ V}$		
$V_I$	Input voltage	0	$V_{CC}$		0	$V_{CC}$		V
$V_O$	Output voltage	0	$V_{CC}$		0	$V_{CC}$		V
$t_t$	Input transition (rise and fall) time	$V_{CC} = 2\text{ V}$		0	1000	$V_{CC} = 2\text{ V}$		ns
		$V_{CC} = 4.5\text{ V}$		0	500	$V_{CC} = 4.5\text{ V}$		
		$V_{CC} = 6\text{ V}$		0	400	$V_{CC} = 6\text{ V}$		
$T_A$	Operating free-air temperature	–55	125		–40	85		°C



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC373		SN74HC373		UNIT	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		1.9		1.9	V		
			4.5 V	4.4	4.499		4.4		4.4			
			6 V	5.9	5.999		5.9		5.9			
		I <sub>OH</sub> = -6 mA	4.5 V	3.98	4.3		3.7		3.84			
		I <sub>OH</sub> = -7.8 mA	6 V	5.48	5.8		5.2		5.34			
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V		0.002	0.1		0.1		0.1	V	
			4.5 V		0.001	0.1		0.1		0.1		
			6 V		0.001	0.1		0.1		0.1		
		I <sub>OL</sub> = 6 mA	4.5 V		0.17	0.26		0.4		0.33		
		I <sub>OL</sub> = 7.8 mA	6 V		0.15	0.26		0.4		0.33		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V		±0.1	±100		±1000		±1000	nA	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or 0		6 V		±0.01	±0.5		±10		±5	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		6 V				8		160		80	μA
C <sub>i</sub>			2 V to 6 V			3	10		10		10	pF

**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC373		SN74HC373		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high	2 V		80		120		100	ns
		4.5 V		16		24		20	
		6 V		14		20		17	
t <sub>su</sub>	Setup time, data before LE↓	2 V		50		75		63	ns
		4.5 V		10		15		13	
		6 V		9		13		11	
t <sub>h</sub>	Hold time, data after LE↓	2 V		20		26		24	ns
		4.5 V		10		13		12	
		6 V		10		13		12	



**SN54HC373, SN74HC373**  
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switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC373		SN74HC373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	D	Q	2 V		58	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
	LE	Any Q	2 V		73	175		265		220	
			4.5 V		18	35		53		44	
			6 V		15	30		45		38	
$t_{en}$	$\overline{OE}$	Any Q	2 V		65	150		225		190	ns
			4.5 V		17	30		45		38	
			6 V		14	26		38		32	
$t_{dis}$	$\overline{OE}$	Any Q	2 V		50	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
$t_t$		Any Q	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

switching characteristics over recommended operating free-air temperature range,  $C_L = 150$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC373		SN74HC373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	D	Q	2 V		82	200		300		250	ns
			4.5 V		22	40		60		50	
			6 V		19	34		51		43	
	LE	Any Q	2 V		100	225		335		285	
			4.5 V		24	45		67		57	
			6 V		20	38		57		48	
$t_{en}$	$\overline{OE}$	Any Q	2 V		90	200		300		250	ns
			4.5 V		23	40		60		50	
			6 V		19	34		51		43	
$t_t$		Any Q	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics,  $T_A = 25^\circ\text{C}$

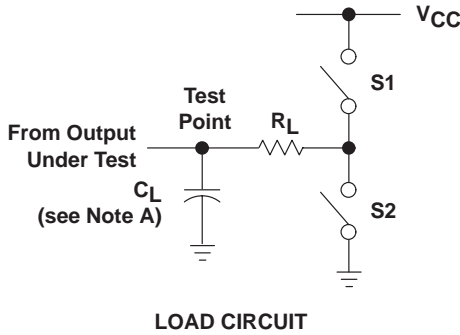
PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance per latch	No load	100	pF



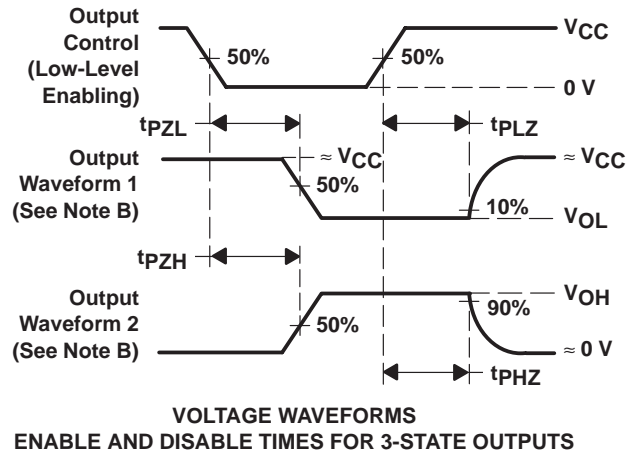
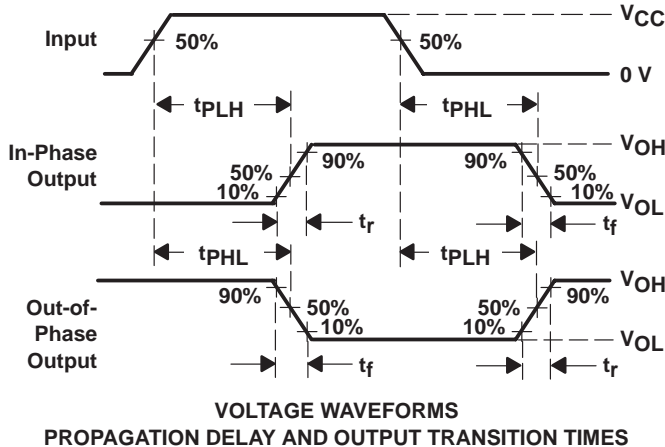
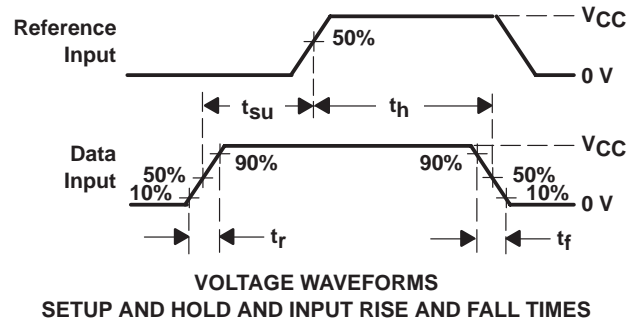
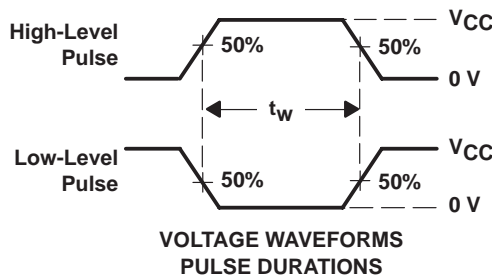
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## PARAMETER MEASUREMENT INFORMATION



PARAMETER	$R_L$	$C_L$	S1	S2
$t_{en}$	1 k $\Omega$	50 pF or 150 pF	Open	Closed
			Closed	Open
$t_{dis}$	1 k $\Omega$	50 pF	Open	Closed
			Closed	Open
$t_{pd}$ or $t_t$	—	50 pF or 150 pF	Open	Open



- NOTES: A.  $C_L$  includes probe and test-fixtue capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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