

MC14194B

4-Bit Bidirectional Universal Shift Register

The MC14194B is a 4-bit static shift register capable of operating in the parallel load, serial shift left, serial shift right, or hold mode. The asynchronous Reset input, when at a low level, overrides all other inputs, resets all stages, and forces all outputs low. When Reset is at a logic 1 level, the two mode control inputs, S0 and S1, control the operating mode as shown in the truth table. Both serial and parallel operation are triggered on the positive-going transition of the Clock input. The Parallel Data, Data Shift, and mode control inputs must be stable for the specified setup and hold times before and after the positive-going Clock transition.

- Synchronous Right/Left Serial Operation
- Synchronous Parallel Load
- Asynchronous Hold (Do Nothing) Mode
- Functional Pin for Pin Equivalent of LS194

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

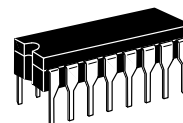
| Symbol | Parameter | Value | Unit |
|------------------------------------|--|--------------------------------|------|
| V _{DD} | DC Supply Voltage | - 0.5 to + 18.0 | V |
| V _{in} , V _{out} | Input or Output Voltage (DC or Transient) | - 0.5 to V _{DD} + 0.5 | V |
| I _{in} , I _{out} | Input or Output Current (DC or Transient), per Pin | ± 10 | mA |
| P _D | Power Dissipation, per Package† | 500 | mW |
| T _{stg} | Storage Temperature | - 65 to + 150 | °C |
| T _L | Lead Temperature (8-Second Soldering) | 260 | °C |

* Maximum Ratings are those values beyond which damage to the device may occur.

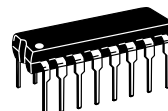
† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



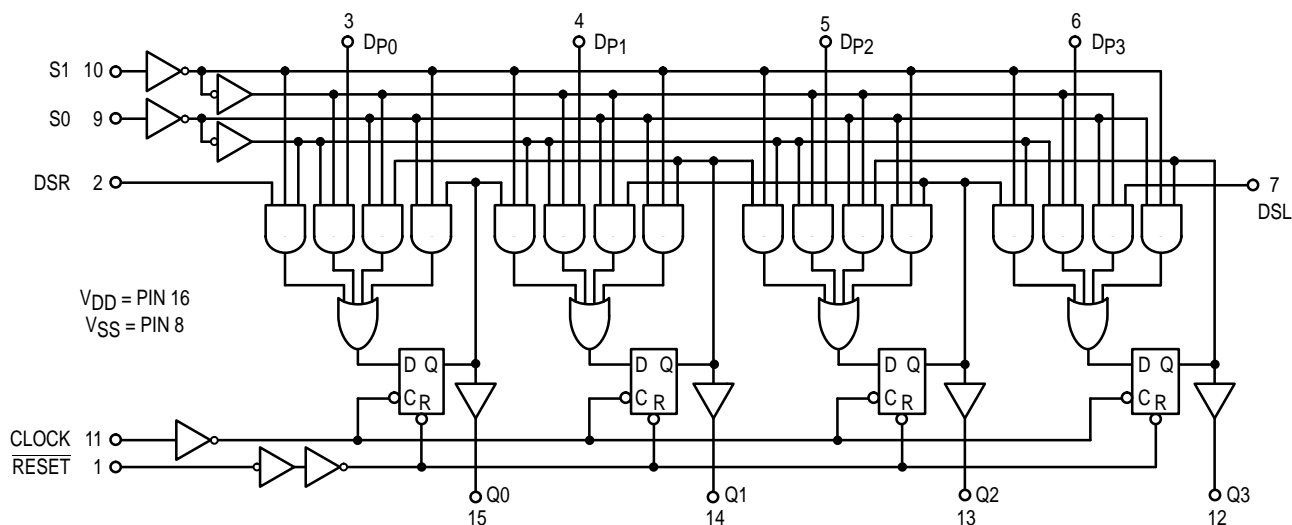
D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = - 55° to 125°C for all packages.

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | Symbol | V _{DD} Vdc | - 55°C | | 25°C | | | 125°C | | Unit | |
|---|---|------------------------|--|-------|--------|-----------|-------|--------|-------|------|-----|
| | | | Min | Max | Min | Typ # | Max | Min | Max | | |
| Output Voltage V _{in} = V _{DD} or 0 | "0" Level V _{OL} | 5.0 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | Vdc | |
| | | 10 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | | |
| | | 15 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | | |
| | "1" Level V _{in} = 0 or V _{DD} | V _{OH} | 5.0 | 4.95 | — | 4.95 | 5.0 | — | 4.95 | — | Vdc |
| | | | 10 | 9.95 | — | 9.95 | 10 | — | 9.95 | — | |
| | | | 15 | 14.95 | — | 14.95 | 15 | — | 14.95 | — | |
| Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) | "0" Level V _{IL} | 5.0 | — | 1.5 | — | 2.25 | 1.5 | — | 1.5 | Vdc | |
| | | 10 | — | 3.0 | — | 4.50 | 3.0 | — | 3.0 | | |
| | | 15 | — | 4.0 | — | 6.75 | 4.0 | — | 4.0 | | |
| | "1" Level (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc) | V _{IH} | 5.0 | 3.5 | — | 3.5 | 2.75 | — | 3.5 | — | Vdc |
| | | | 10 | 7.0 | — | 7.0 | 5.50 | — | 7.0 | — | |
| | | | 15 | 11 | — | 11 | 8.25 | — | 11 | — | |
| Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) | Source I _{OH} | 5.0 | - 3.0 | — | - 2.4 | - 4.2 | — | - 1.7 | — | mAdc | |
| | | 5.0 | - 0.64 | — | - 0.51 | - 0.88 | — | - 0.36 | — | | |
| | | 10 | - 1.6 | — | - 1.3 | - 2.25 | — | - 0.9 | — | | |
| | Sink I _{OL} | 5.0 | 0.64 | — | 0.51 | 0.88 | — | 0.36 | — | mAdc | |
| | | 10 | 1.6 | — | 1.3 | 2.25 | — | 0.9 | — | | |
| | | 15 | 4.2 | — | 3.4 | 8.8 | — | 2.4 | — | | |
| Input Current | I _{in} | 15 | — | ± 0.1 | — | ± 0.00001 | ± 0.1 | — | ± 1.0 | μAdc | |
| Input Capacitance (V _{in} = 0) | C _{in} | — | — | — | — | 5.0 | 7.5 | — | — | pF | |
| Quiescent Current (Per Package) | I _{DD} | 5.0 | — | 5.0 | — | 0.005 | 5.0 | — | 150 | μAdc | |
| | | 10 | — | 10 | — | 0.010 | 10 | — | 300 | | |
| | | 15 | — | 20 | — | 0.015 | 20 | — | 600 | | |
| Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching) | I _T | 5.0 | I _T = (0.95 μA/kHz) f + I _{DD} I _T = (1.90 μA/kHz) f + I _{DD} I _T = (2.90 μA/kHz) f + I _{DD} | | | | | | | μAdc | |

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT

| | | | |
|-----------------|-----|----|-----------------|
| R̄ | 1 ● | 16 | V _{DD} |
| DSR | 2 | 15 | Q ₀ |
| DP ₀ | 3 | 14 | Q ₁ |
| DP ₁ | 4 | 13 | Q ₂ |
| DP ₂ | 5 | 12 | Q ₃ |
| DP ₃ | 6 | 11 | C |
| DSL | 7 | 10 | S ₁ |
| V _{SS} | 8 | 9 | S ₀ |

TRUTH TABLE

| Operating Mode | Inputs (Reset = 1) | | | | | Outputs (@ t _{n+1}) | | | |
|----------------|--------------------|----|-----|-----|-------|-------------------------------|----|----|----|
| | S1 | S0 | DSR | DSL | Dp0-3 | Q0 | Q1 | Q2 | Q3 |
| Hold | 0 | 0 | X | X | X | Q0 | Q1 | Q2 | Q3 |
| Shift Left | 1 | 0 | X | 0 | X | Q1 | Q2 | Q3 | 0 |
| | 1 | 0 | X | 1 | X | Q1 | Q2 | Q3 | 1 |
| Shift Right | 0 | 1 | 0 | X | X | 0 | Q0 | Q1 | Q2 |
| | 0 | 1 | 1 | X | X | 1 | Q0 | Q1 | Q2 |
| Parallel | 1 | 1 | X | X | 0 | 0 | 0 | 0 | 0 |
| | 1 | 1 | X | X | 1 | 1 | 1 | 1 | 1 |

X = Don't Care

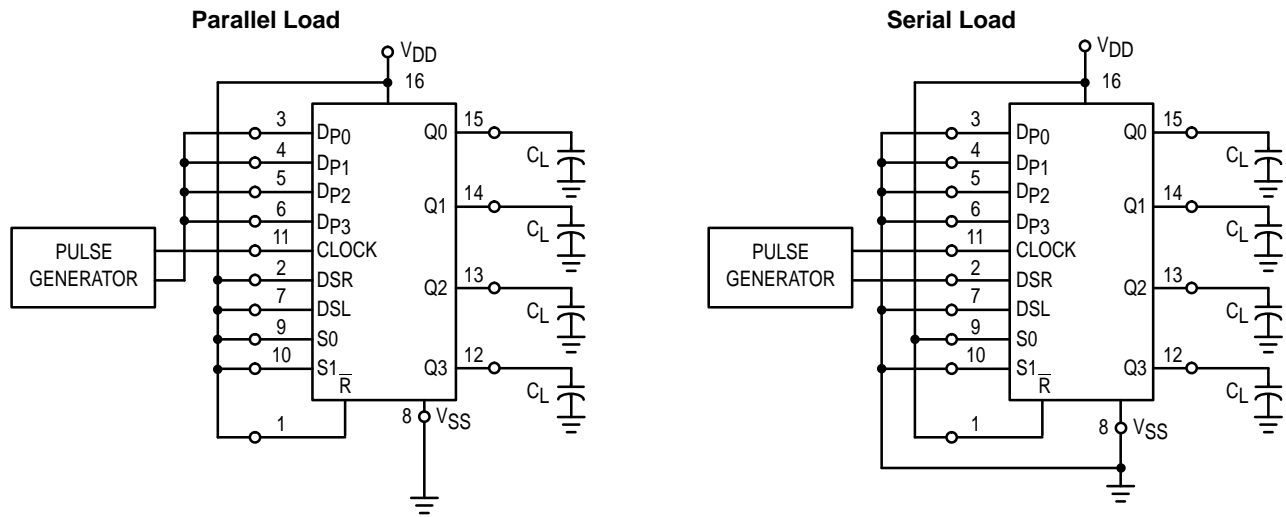
t_{n+1} = State after the next positive-going transition of the clock.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

| Characteristic | Symbol | V _{DD} Vdc | Min | Typ # | Max | Unit |
|--|-------------------------------------|------------------------|------------------|----------------------|-------------------|------|
| Output Rise and Fall Time t _{TLH} , t _{THL} = (1.35 ns/pF) C _L + 32 ns t _{TLH} , t _{THL} = (0.6 ns/pF) C _L + 20 ns t _{TLH} , t _{THL} = (0.4 ns/pF) C _L + 20 ns | t _{TLH} , t _{THL} | 5.0 10 15 | — — — | 100 50 40 | 200 100 80 | ns |
| Propagation Delay Time Clock to Q t _{PLH} , t _{PHL} = (0.9 ns/pF) C _L + 230 ns t _{PLH} , t _{PHL} = (0.36 ns/pF) C _L + 92 ns t _{PLH} , t _{PHL} = (0.26 ns/pF) C _L + 72 ns Reset to Q t _{PHL} = (0.9 ns/pF) C _L + 305 ns t _{PHL} = (0.36 ns/pF) C _L + 122 ns t _{PHL} = (0.26 ns/pF) C _L + 97 ns | t _{PLH} , t _{PHL} | 5.0 10 15 | — — — | 275 110 85 | 550 220 170 | ns |
| | t _{PHL} | 5.0 10 15 | — — — | 350 140 110 | 700 280 220 | ns |
| Clock Pulse Width | t _{WH} | 5.0 10 15 | 280 110 85 | 140 55 40 | — — — | ns |
| Reset Pulse Width | t _{WH} | 5.0 10 15 | 180 70 50 | 90 35 26 | — — — | ns |
| Clock Pulse Frequency (Shift Right or Left Mode) | f _{cl} | 5.0 10 15 | — — — | 3.6 9.0 12 | 1.8 4.5 6.0 | MHz |
| Clock Pulse Rise and Fall Time | t _{TLH} , t _{THL} | 5.0 10 15 | — — — | — — — | 15 5 4 | μs |
| Setup Time Data to Clock Mode Control (S) to Clock | t _{su} | 5.0 10 15 | 10 20 40 | - 8.0 0 9.0 | — — — | ns |
| | | 5.0 10 15 | 200 75 55 | 100 36 27 | — — — | ns |
| Hold Time Data to Clock Mode Control (S) to Clock | t _h | 5.0 10 15 | 180 50 35 | 90 25 10 | — — — | ns |
| | | 5.0 10 15 | 0 0 0 | - 40 - 27 - 20 | — — — | ns |
| Reset Removal Time | t _{rem} | 5.0 10 15 | 300 110 80 | 150 55 40 | — — — | ns |

* The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



NOTE: Interchange DSR with DSL and S0 with S1 for testing shift left.

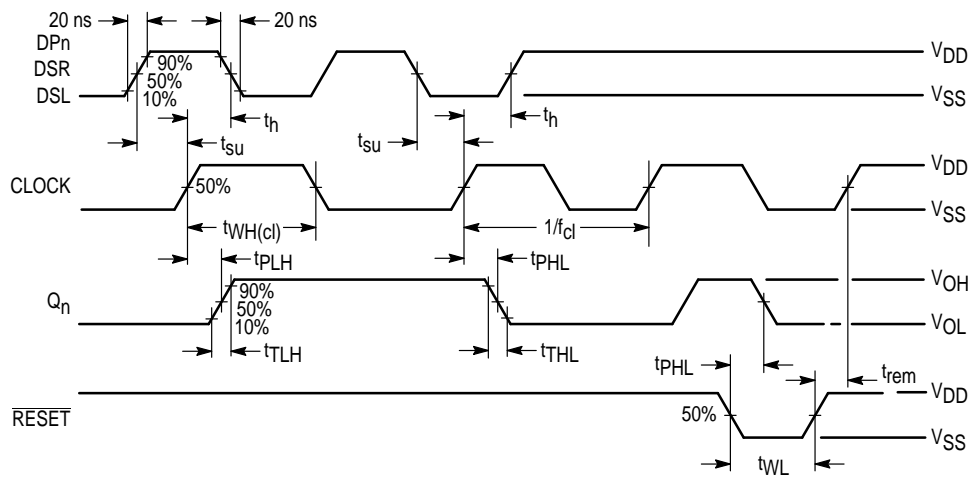


Figure 1. Switching Time Test Circuits and Waveforms

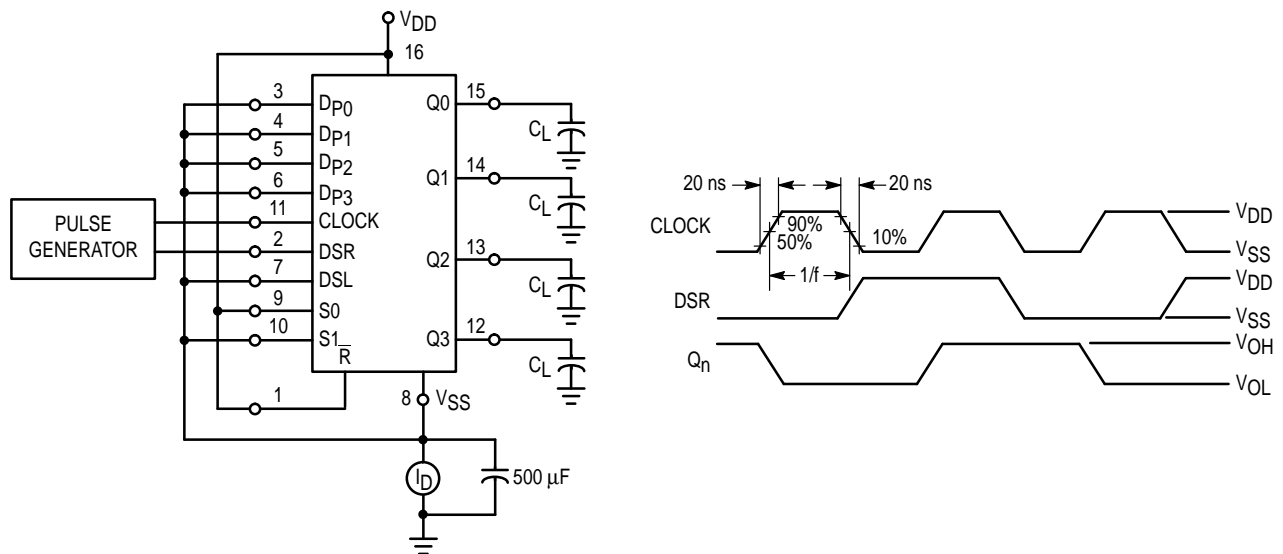
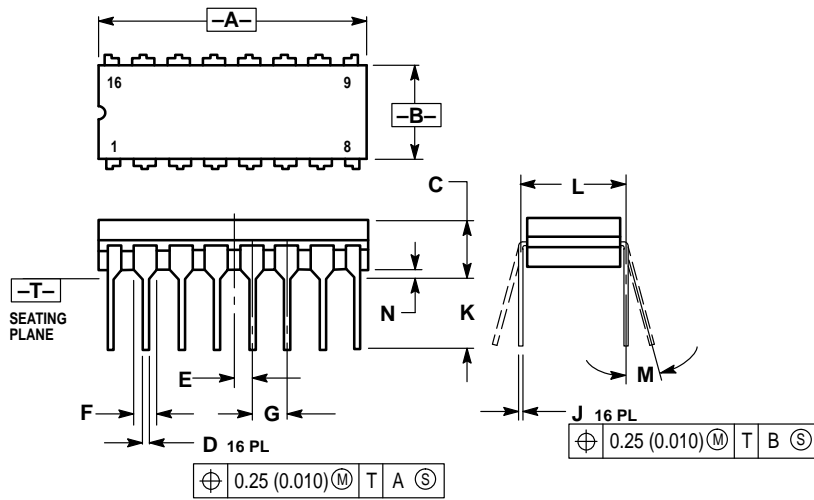


Figure 2. Dynamic Power Dissipation Test Circuit and Waveforms

OUTLINE DIMENSIONS

L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.750 | 0.785 | 19.05 | 19.93 |
| B | 0.240 | 0.295 | 6.10 | 7.49 |
| C | — | 0.200 | — | 5.08 |
| D | 0.015 | 0.020 | 0.39 | 0.50 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.055 | 0.065 | 1.40 | 1.65 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.125 | 0.170 | 3.18 | 4.31 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



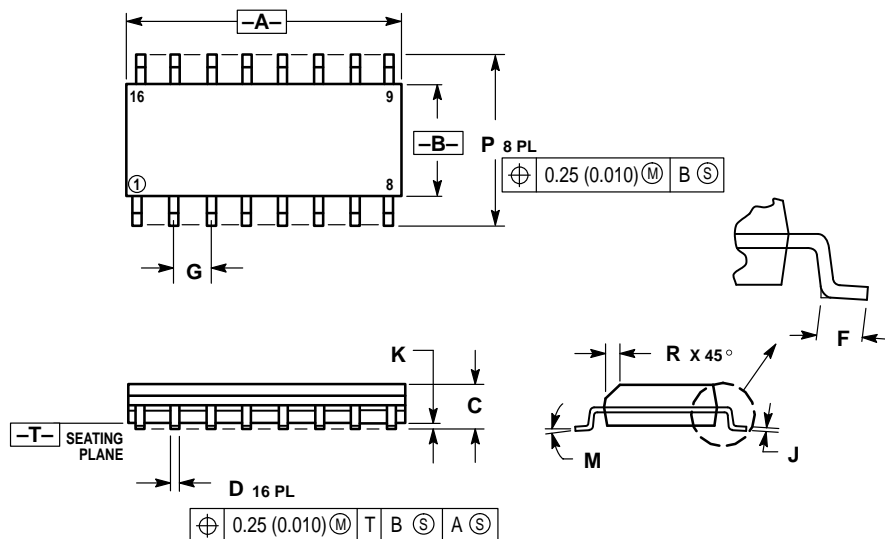
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

OUTLINE DIMENSIONS

D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

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MC14194B/D

