

## Open-Drain Output Sub-Microamp Comparators

### Features

- Low Quiescent Current: 600 nA/comparator (typ.)
- Rail-to-Rail Input:  $V_{SS}-0.3V$  to  $V_{DD}+0.3V$
- Open-Drain Output:  $V_{OUT} \leq 10V$
- Propagation Delay 4  $\mu s$  (typ)
- Wide Supply Voltage Range: 1.6V to 5.5V
- Single available in SOT-23-5, SC-70-5 packages
- Available in Single, Dual and Quad
- Chip Select (CS) with MCP6548
- Low Switching Current
- Internal Hysteresis: 3.3 mV (typ)

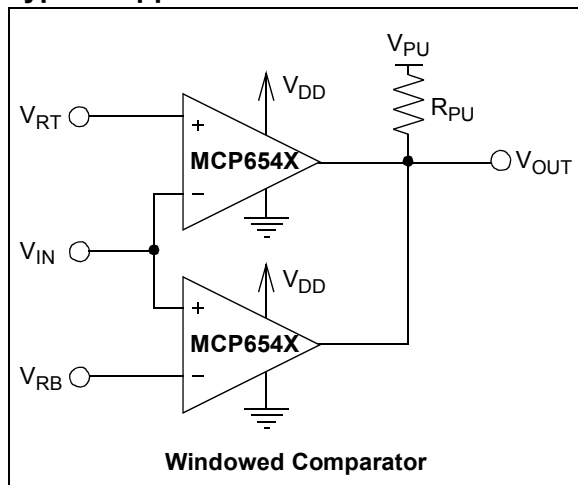
### Typical Applications

- Laptop Computers
- Mobile Phones
- Metering Systems
- Hand-held Electronics
- RC Timers
- Alarm and Monitoring Circuits
- Windowed Comparators
- Multi-vibrators

### Related Devices

- CMOS/TTL Compatible Output: MCP6541/2/3/4

### Typical Application Circuit



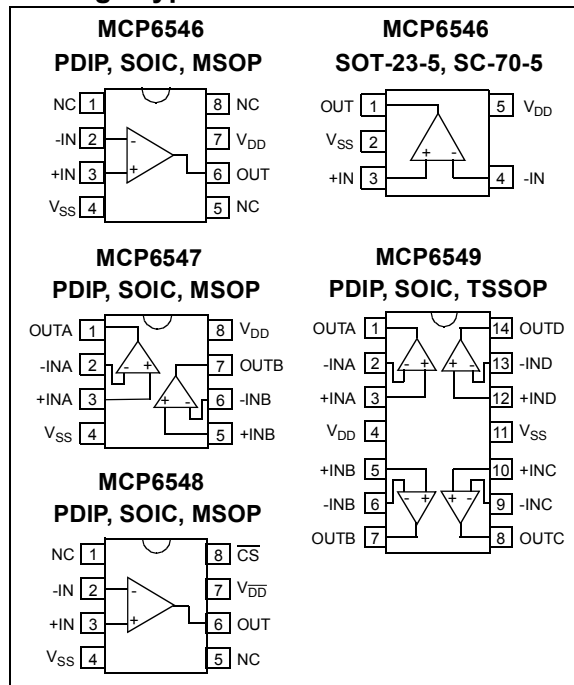
### Description

The Microchip Technology, Inc. MCP6546/7/8/9 family of comparators is offered in single (MCP6546), single with chip select (MCP6548), dual (MCP6547) and quad (MCP6549) configurations. The outputs are open-drain and are capable of driving heavy DC or capacitive loads.

These comparators are optimized for low power, single-supply operation with greater than rail-to-rail input operation. The output limits supply current surges and dynamic power consumption while switching. The open-drain output of the MCP6546/7/8/9 family, with a pull-up resistor, can be used as a level-shifter for any desired voltage up to 10V, and in wired-OR logic. Input hysteresis eliminates output switching due to internal noise voltage, reducing current draw. These comparators operate with a single-supply voltage as low as 1.6V and draw less than 1  $\mu A$ /comparator of quiescent current.

The related MCP6541/2/3/4 family of comparators from Microchip has a push-pull output that supports rail-to-rail output swing and interfaces with CMOS/TTL logic.

### Package Types



# MCP6546/7/8/9

## 1.0 ELECTRICAL CHARACTERISTICS

### 1.1 Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ .....	7.0V
Open-Drain output.....	$V_{SS} + 10.5V$
All inputs and outputs .....	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Difference Input voltage .....	$ V_{DD} - V_{SS} $
Output Short-Circuit Current .....	continuous
Current at Input Pins .....	$\pm 2$ mA
Current at Output and Supply Pins .....	$\pm 30$ mA
Storage temperature .....	$-65^{\circ}C$ to $+150^{\circ}C$
Junction Temperature.....	$+150^{\circ}C$
ESD protection on all pins (HBM); (MM) .....	4 kV; 200V

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### PIN FUNCTION TABLE

NAME	FUNCTION
+IN/+INA/+INB/+INC/+IND	Non-inverting Inputs
-IN/-INA/-INB/-INC/-IND	Inverting Inputs
$V_{DD}$	Positive Power Supply
$V_{SS}$	Negative Power Supply
OUT/OUTA/OUTB/OUTC/OUTD	Outputs
$\overline{CS}$	Chip Select
NC	Not Connected

## DC CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated,  $V_{DD} = +1.6V$  to  $+5.5V$ ,  $V_{SS} = GND$ ,  $T_A = 25^{\circ}C$ ,  $V_{IN+} = V_{DD}/2$ ,  $V_{IN-} = V_{SS}$ ,  $R_{PU} = 2.74$  k $\Omega$  to  $V_{PU} = V_{DD}$ . Refer to Figure 1-3.

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Power Supply</b>						
Supply Voltage	$V_{DD}$	1.6	—	5.5	V	
Quiescent Current per comparator	$I_Q$	0.3	0.6	1	$\mu A$	$I_{OUT} = 0$
<b>Input</b>						
Input Voltage Range	$V_{CMR}$	$V_{SS} - 0.3$	—	$V_{DD} + 0.3$	V	
Common Mode Rejection Ratio	CMRR	55	70	—	dB	$V_{DD} = 5V$ , $V_{CM} = -0.3V$ to $5.3V$
Common Mode Rejection Ratio	CMRR	50	65	—	dB	$V_{DD} = 5V$ , $V_{CM} = 2.5V$ to $5.3V$
Common Mode Rejection Ratio	CMRR	55	70	—	dB	$V_{DD} = 5V$ , $V_{CM} = -0.3V$ to $2.5V$
Power Supply Rejection Ratio	PSRR	63	80	—	dB	$V_{CM} = V_{SS}$
Input Offset Voltage	$V_{OS}$	-7.0	$\pm 1.5$	+7.0	mV	$V_{CM} = V_{SS}$ ( <b>Note 1</b> )
Drift with Temperature	$\Delta V_{OS}/\Delta T$	—	$\pm 3$	—	$\mu V/^{\circ}C$	$T_A = -40^{\circ}C$ to $+85^{\circ}C$ , $V_{CM} = V_{SS}$
Input Hysteresis Voltage	$V_{HYST}$	1.5	3.3	6.5	mV	$V_{CM} = V_{SS}$ ( <b>Note 1</b> )
Drift with Temperature	$\Delta V_{HYST}/\Delta T$	—	10	—	$\mu V/^{\circ}C$	$T_A = -40^{\circ}C$ to $+25^{\circ}C$ , $V_{CM} = V_{SS}$
Drift with Temperature	$\Delta V_{HYST}/\Delta T$	—	5	—	$\mu V/^{\circ}C$	$T_A = +25^{\circ}C$ to $+85^{\circ}C$ , $V_{CM} = V_{SS}$
Input Bias Current	$I_B$	—	1	—	pA	$V_{CM} = V_{SS}$
Over Temperature	$I_B$	—	—	100	pA	$T_A = -40^{\circ}C$ to $+85^{\circ}C$ , $V_{CM} = V_{SS}$ ( <b>Note 3</b> )
Input Offset Current	$I_{OS}$	—	$\pm 1$	—	pA	$V_{CM} = V_{SS}$
Common Mode Input Impedance	$Z_{CM}$	—	$10^{13}  4$	—	$\Omega  pF$	
Differential Input Impedance	$Z_{DIFF}$	—	$10^{13}  2$	—	$\Omega  pF$	
<b>Open-Drain Output</b>						
Output Pull-Up Voltage	$V_{PU}$	$V_{DD}$	—	10	V	( <b>Note 2</b> )
High-Level Output Current	$I_{OH}$	-100	—	—	nA	$V_{DD} = 1.6V$ to $5.5V$ , $V_{PU} = 10V$ ( <b>Note 2</b> )
Low-Level Output Voltage	$V_{OL}$	$V_{SS}$	—	$V_{SS} + 0.2$	V	$I_{OUT} = 2$ mA, $V_{PU} = V_{DD} = 5V$
Short-Circuit Current	$I_{SC}$	—	$\pm 50$	—	mA	$V_{PU} = V_{DD} = 5.0V$ ( <b>Note 2</b> )
Output Pin Capacitance	$C_{OUT}$	—	8	—	pF	

- Note 1:** The input offset voltage is the center of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.
- Note 2:** Do not short the output about  $V_{SS} + 10V$ . Limit the output current to Absolute Maximum Rating of 30 mA. The comparator does not function properly when  $V_{PU} < V_{DD}$ .
- Note 3:** Input bias current over temperature is not tested for the SC-70-5 package.

## AC CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated,  $V_{DD} = +1.6V$  to  $+5.5V$ ,  $V_{SS} = GND$ ,  $T_A = 25^\circ C$ ,  $V_{IN+} = V_{DD}/2$ , Step = 200 mV, Overdrive = 100 mV,  $R_{PU} = 2.74 k\Omega$  to  $V_{PU} = V_{DD}$ , and  $C_L = 36 pF$ . Refer to Figure 1-2 and Figure 1-3.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Fall Time	$t_F$	—	0.7	—	$\mu s$	(Note 1)
Propagation Delay (High-to-Low)	$t_{PHL}$	—	4.0	8.0	$\mu s$	(Note 1)
Propagation Delay (Low-to-High)	$t_{PLH}$	—	3.0	8.0	$\mu s$	
Propagation Delay Skew	$t_{PDS}$	—	-1.0	—	$\mu s$	
Maximum Toggle Frequency	$f_{MAX}$	—	225	—	kHz	$V_{DD} = 1.6V$
	$f_{MAX}$	—	165	—	kHz	$V_{DD} = 5.5V$
Input Noise Voltage	$E_N$	—	200	—	$\mu V_{P-P}$	10 Hz to 100 kHz

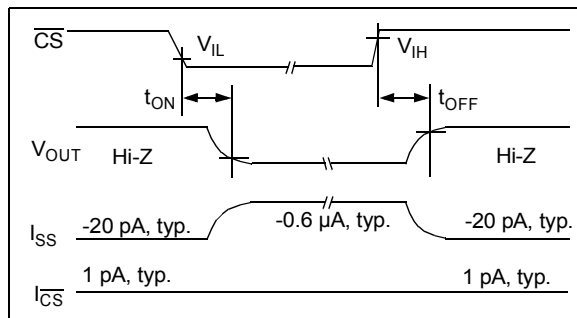
**Note 1:**  $t_R$  and  $t_{PLH}$  depend on the load ( $R_L$  and  $C_L$ ); these specifications are valid for the indicated load only.

**Note 2:** Propagation Delay Skew is defined as:  $t_{PDS} = t_{PLH} - t_{PHL}$ .

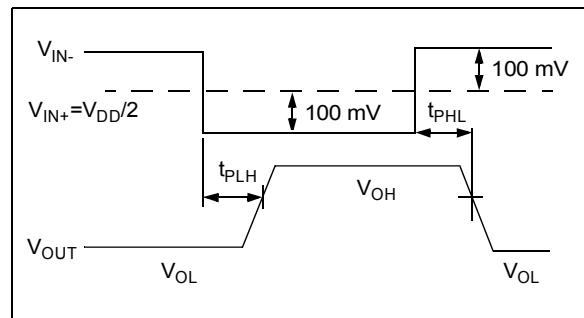
## SPECIFICATIONS FOR MCP6548 CHIP SELECT

**Electrical Specifications:** Unless otherwise indicated,  $V_{DD} = +1.6V$  to  $+5.5V$ ,  $V_{SS} = GND$ ,  $T_A = 25^\circ C$ ,  $V_{IN+} = V_{DD}/2$ ,  $V_{IN-} = V_{SS}$ ,  $R_{PU} = 2.74 k\Omega$  to  $V_{PU} = V_{DD}$ , and  $C_L = 36 pF$ . Refer to Figure 1-3.

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b><math>\overline{CS}</math> Low Specifications</b>						
$\overline{CS}$ Logic Threshold, Low	$V_{IL}$	$V_{SS}$	—	$0.2V_{DD}$	V	
$\overline{CS}$ Input Current, Low	$I_{CSL}$	—	5	—	pA	$\overline{CS} = V_{SS}$
<b><math>\overline{CS}</math> High Specifications</b>						
$\overline{CS}$ Logic Threshold, High	$V_{IH}$	$0.8V_{DD}$	—	$V_{DD}$	V	
$\overline{CS}$ Input Current, High	$I_{CSH}$	—	1	—	pA	$\overline{CS} = V_{DD}$
$\overline{CS}$ Input High, $V_{DD}$ Current	$I_{DD}$	—	18	—	pA	$\overline{CS} = V_{DD}$
$\overline{CS}$ Input High, GND Current	$I_{SS}$	—	-20	—	pA	$\overline{CS} = V_{DD}$
Comparator Output Leakage	$I_{O(LEAK)}$	—	1	—	pA	$V_{OUT} = V_{SS} + 10V$
<b><math>\overline{CS}</math> Dynamic Specifications</b>						
$\overline{CS}$ Low to Comparator Output Low Turn-on Time	$t_{ON}$	—	2	50	ms	$\overline{CS} = 0.2V_{DD}$ to $V_{OUT} = V_{DD}/2$ , $V_{IN-} = V_{DD}$
$\overline{CS}$ High to Comparator Output High Z Turn-off Time	$t_{OFF}$	—	10	—	$\mu s$	$\overline{CS} = 0.8V_{DD}$ to $V_{OUT} = V_{DD}/2$ , $V_{IN-} = V_{DD}$
$\overline{CS}$ Hysteresis	$V_{CS\_HYST}$	—	0.6	—	V	$V_{DD} = 5V$



**FIGURE 1-1:** Timing Diagram for the  $\overline{CS}$  pin on the MCP6548.



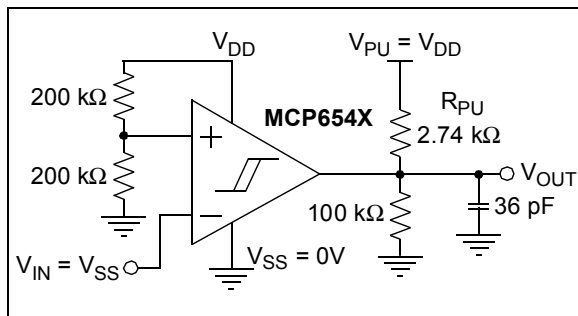
**FIGURE 1-2:** Propagation Delay Timing Diagram.

# MCP6546/7/8/9

## TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, $V_{DD} = +1.6V$ to $+5.5V$ and $V_{SS} = GND$ .						
Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Temperature Ranges</b>						
Specified Temperature Range	$T_A$	-40	—	+85	°C	Note
Operating Temperature Range	$T_A$	-40	—	+125	°C	
Storage Temperature Range	$T_A$	-65	—	+150	°C	
<b>Thermal Package Resistances</b>						
Thermal Resistance, 5L-SC-70	$\theta_{JA}$	—	331	—	°C/W	
Thermal Resistance, 5L-SOT-23	$\theta_{JA}$	—	256	—	°C/W	
Thermal Resistance, 8L-PDIP	$\theta_{JA}$	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	$\theta_{JA}$	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	$\theta_{JA}$	—	206	—	°C/W	
Thermal Resistance, 14L-PDIP	$\theta_{JA}$	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	$\theta_{JA}$	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	$\theta_{JA}$	—	100	—	°C/W	

**Note:** The MCP6546/7/8/9 operates over this extended temperature range, but with reduced performance. In any case, the Junction Temperature ( $T_J$ ) must not exceed the Absolute Maximum specification of  $+150^\circ\text{C}$ .

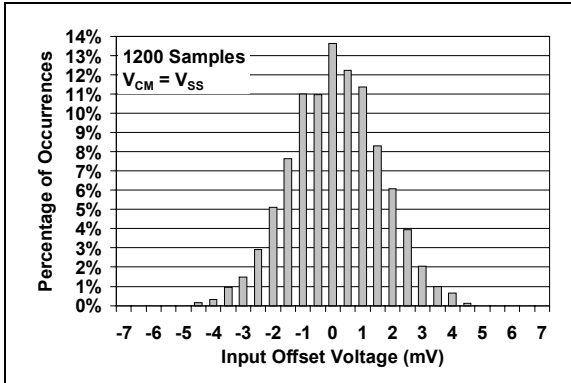


**FIGURE 1-3:** DC Test circuit for the open-drain output comparators.

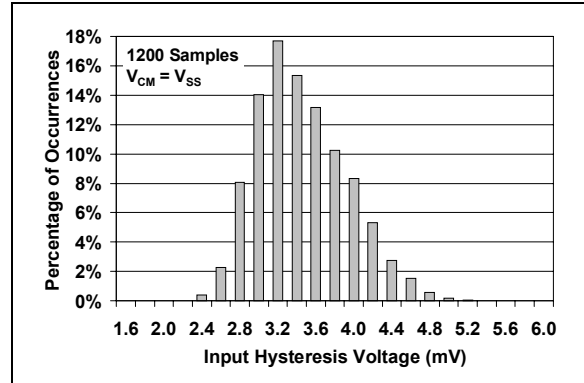
## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

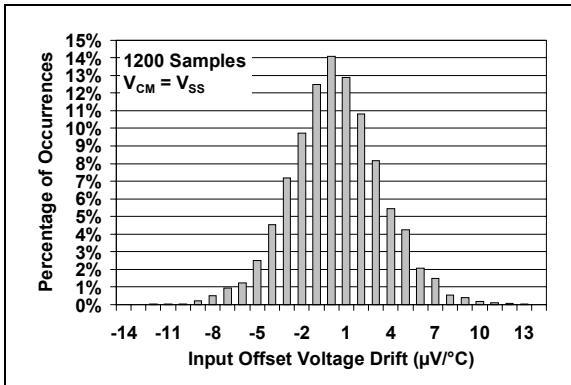
**Note:** Unless otherwise indicated,  $V_{DD} = +5.0V$ ,  $V_{SS} = GND$ ,  $T_A = 25^\circ C$ ,  $V_{IN+} = V_{DD}/2$ ,  $V_{IN-} = GND$ ,  $R_{PU} = 2.74\ k\Omega$  and  $V_{PU} = V_{DD}$ , and  $C_L = 36\ pF$ .



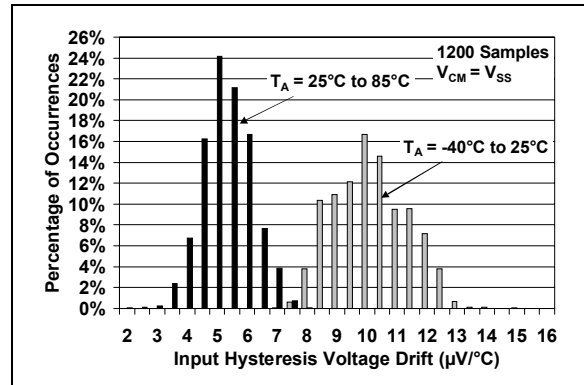
**FIGURE 2-1:** Histogram of Input Offset Voltage with  $V_{CM} = V_{SS}$ .



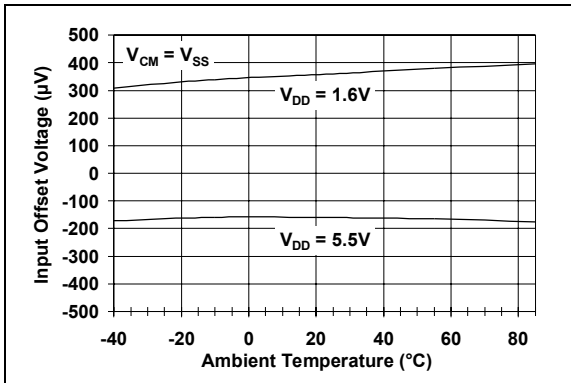
**FIGURE 2-4:** Histogram of Input Hysteresis Voltage with  $V_{CM} = V_{SS}$ .



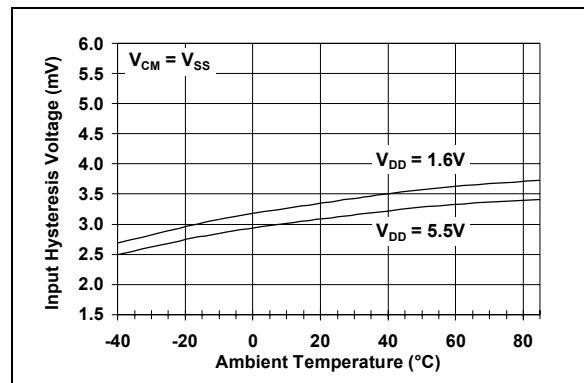
**FIGURE 2-2:** Histogram of Input Offset Voltage Drift with  $V_{CM} = V_{SS}$ .



**FIGURE 2-5:** Histogram of Input Hysteresis Voltage Drift with Temperature =  $-40^\circ C$  to  $25^\circ C$  and  $25^\circ C$  to  $85^\circ C$ ,  $V_{CM} = V_{SS}$ .



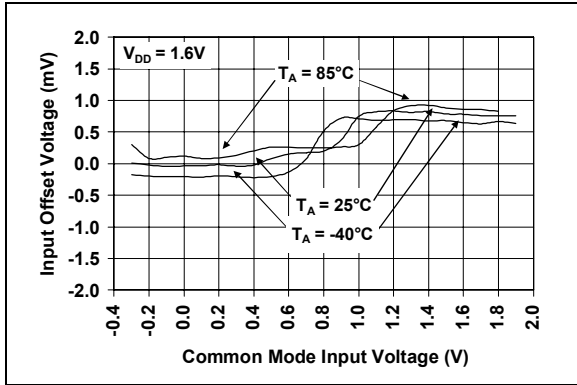
**FIGURE 2-3:** Input Offset Voltage vs. Ambient Temperature vs. Power Supply Voltage with  $V_{CM} = V_{SS}$ .



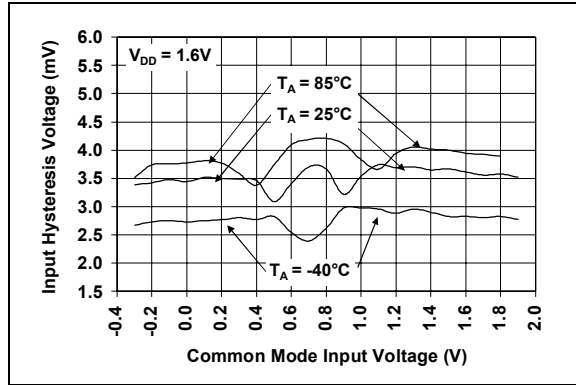
**FIGURE 2-6:** Input Hysteresis Voltage vs. Ambient Temperature vs. Power Supply Voltage with  $V_{CM} = V_{SS}$ .

# MCP6546/7/8/9

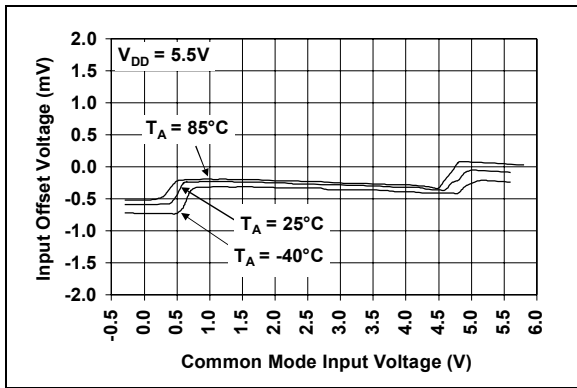
**Note:** Unless otherwise indicated,  $V_{DD} = +5.0V$ ,  $V_{SS} = GND$ ,  $T_A = 25^\circ C$ ,  $V_{IN+} = V_{DD}/2$ ,  $V_{IN-} = GND$ ,  $R_{PU} = 2.74\text{ k}\Omega$  to  $V_{PU} = V_{DD}$ , and  $C_L = 36\text{ pF}$ .



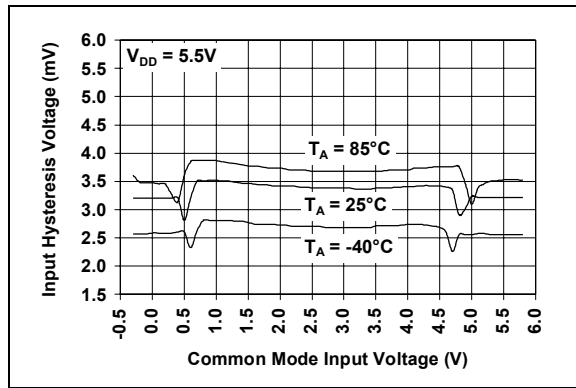
**FIGURE 2-7:** Input Offset Voltage vs. Common Mode Input Voltage vs. Temperature with  $V_{DD} = 1.6V$ .



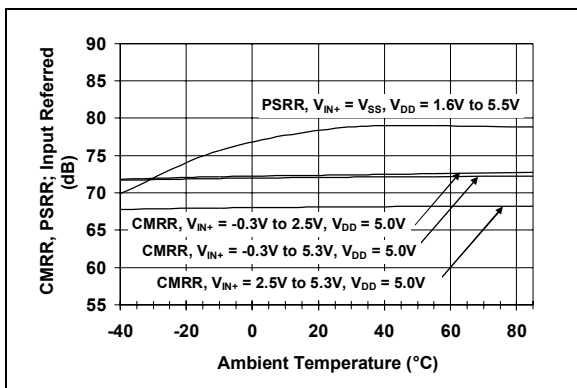
**FIGURE 2-10:** Input Hysteresis Voltage vs. Common Mode Input Voltage vs. Temperature with  $V_{DD} = 1.6V$ .



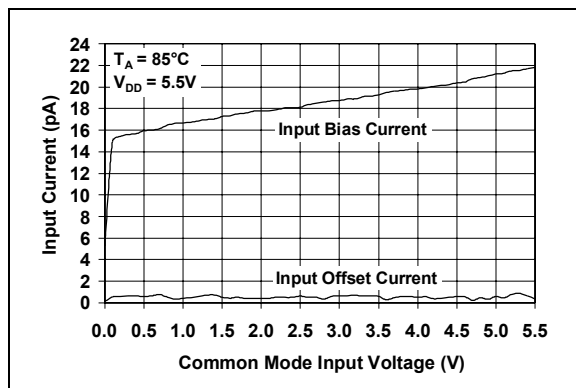
**FIGURE 2-8:** Input Offset Voltage vs. Common Mode Input Voltage vs. Temperature with  $V_{DD} = 5.5V$ .



**FIGURE 2-11:** Input Hysteresis Voltage vs. Common Mode Input Voltage vs. Temperature with  $V_{DD} = 5.5V$ .

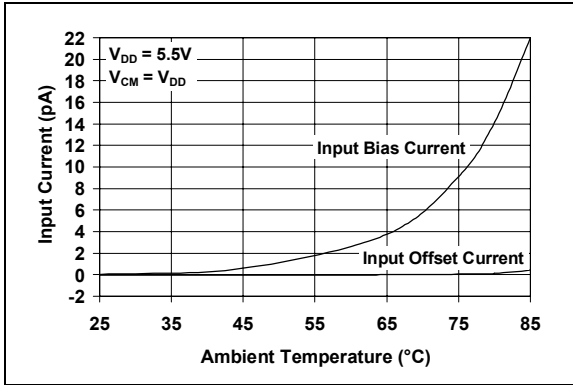


**FIGURE 2-9:** Common Mode Rejection Ratio, Power Supply Rejection Ratio vs. Ambient Temperature with  $V_{CM} = V_{SS}$ .

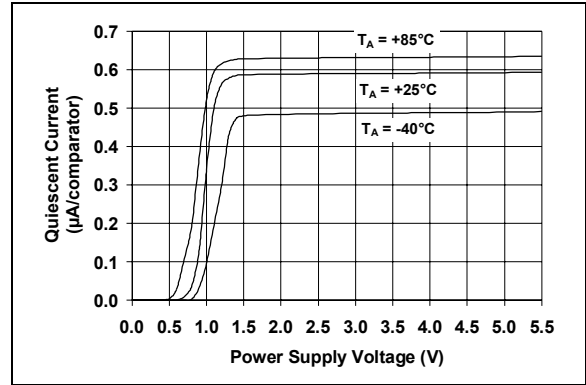


**FIGURE 2-12:** Input Bias Current, Input Offset Current vs. Common Mode Input Voltage with Temperature =  $85^\circ C$ .

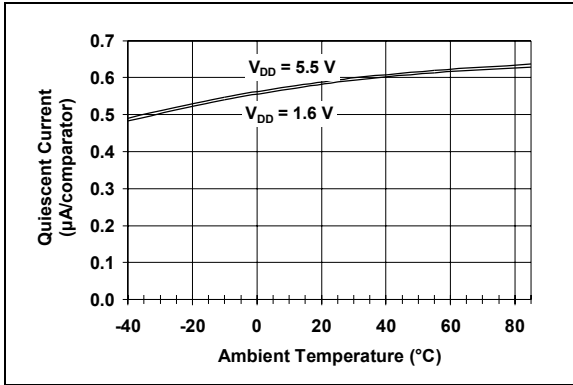
**Note:** Unless otherwise indicated,  $V_{DD} = +5.0V$ ,  $V_{SS} = GND$ ,  $T_A = 25^\circ C$ ,  $V_{IN+} = V_{DD}/2$ ,  $V_{IN-} = GND$ ,  $R_{PU} = 2.74\text{ k}\Omega$  to  $V_{PU} = V_{DD}$ , and  $C_L = 36\text{ pF}$ .



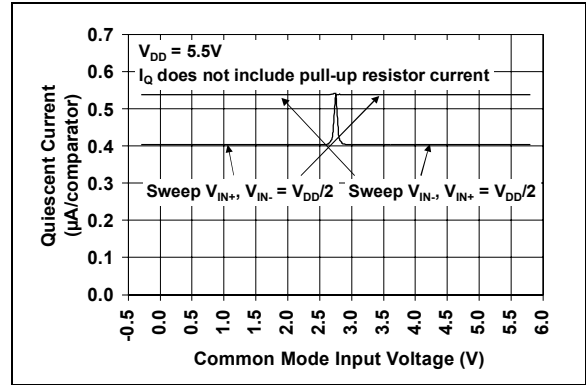
**FIGURE 2-13:** Input Bias Current, Input Offset Current vs. Ambient Temperature.



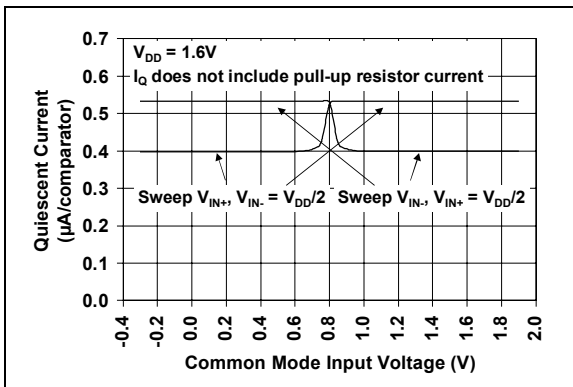
**FIGURE 2-16:** Quiescent Current vs. Power Supply Voltage vs. Temperature.



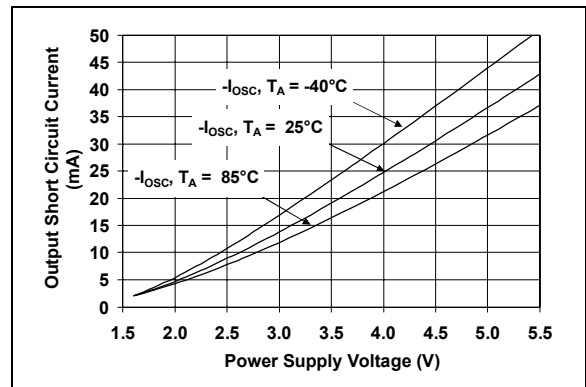
**FIGURE 2-14:** Quiescent Current vs. Ambient Temperature vs. Power Supply Voltage.



**FIGURE 2-17:** Quiescent Current vs. Common Mode Input Voltage with  $V_{DD} = 5V$ .



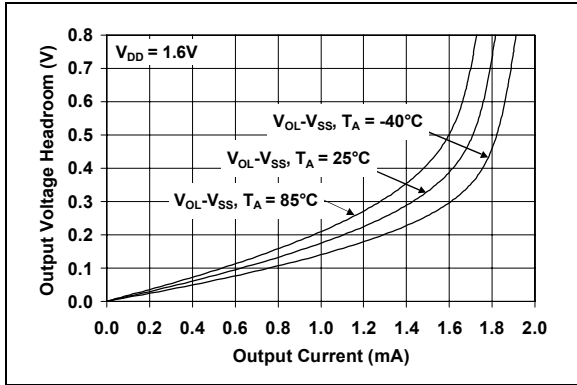
**FIGURE 2-15:** Quiescent Current vs. Common Mode Input Voltage with  $V_{DD} = 1.6V$ .



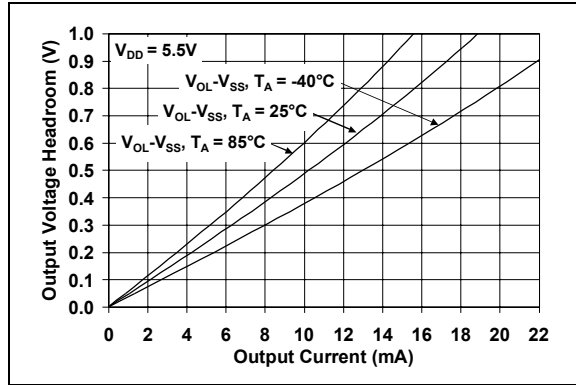
**FIGURE 2-18:** Output Short Circuit Current vs. Power Supply Voltage vs. Temperature.

# MCP6546/7/8/9

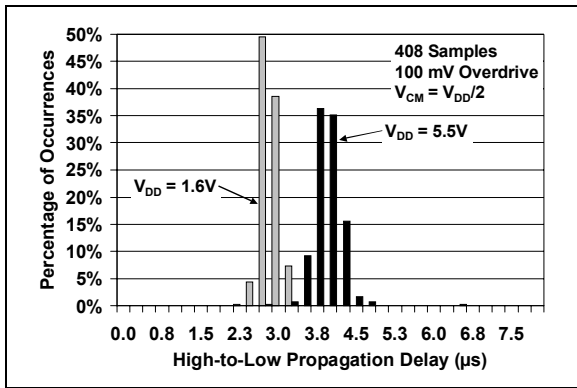
**Note:** Unless otherwise indicated,  $V_{DD} = +5.0V$ ,  $V_{SS} = GND$ ,  $T_A = 25^\circ C$ ,  $V_{IN+} = V_{DD}/2$ ,  $V_{IN-} = GND$ ,  $R_{PU} = 2.74\text{ k}\Omega$  to  $V_{PU} = V_{DD}$ , and  $C_L = 36\text{ pF}$ .



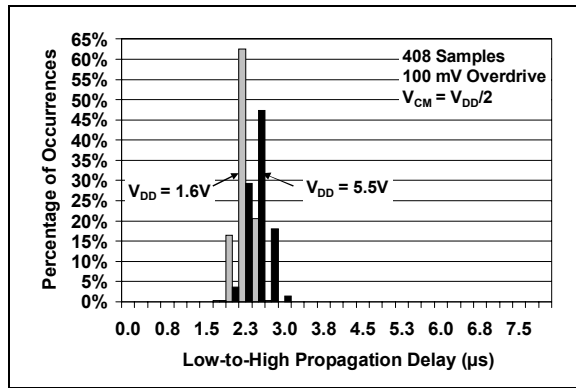
**FIGURE 2-19:** Output Voltage Headroom vs. Output Current vs. Temperature with  $V_{DD} = 1.6V$ .



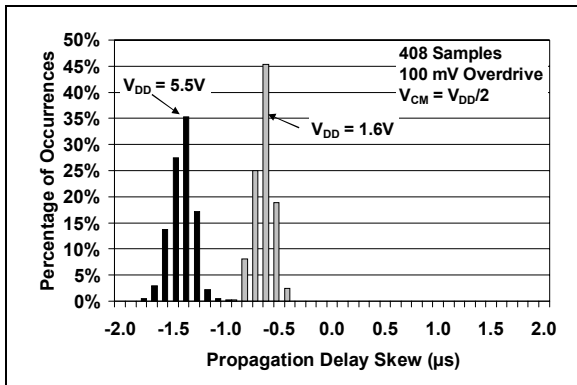
**FIGURE 2-22:** Output Voltage Headroom vs. Output Current vs. Temperature with  $V_{DD} = 5.5V$ .



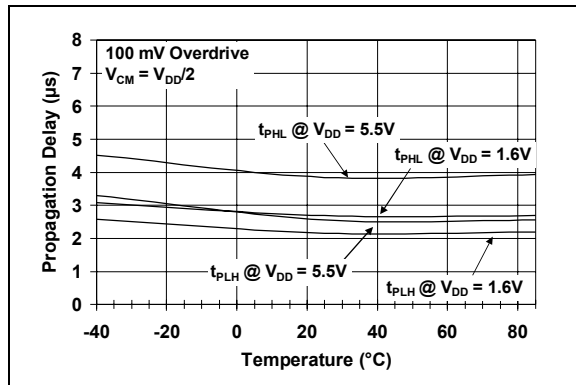
**FIGURE 2-20:** Histogram of High-to-Low Propagation Delay with  $V_{DD} = 1.6V$  and  $5.5V$ .



**FIGURE 2-23:** Histogram of Low-to-High Propagation Delay with  $V_{DD} = 1.6V$  and  $5.5V$ .



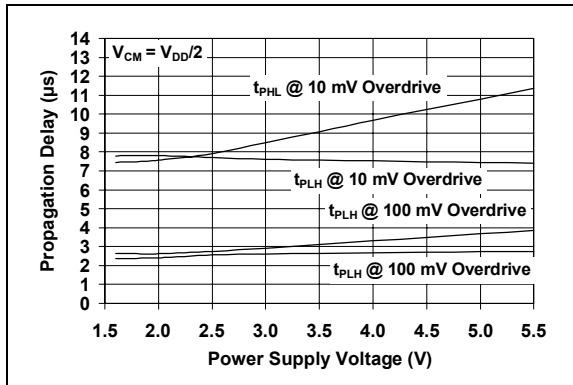
**FIGURE 2-21:** Histogram of Propagation Delay Skew with  $V_{DD} = 1.6V$  and  $5.5V$ .



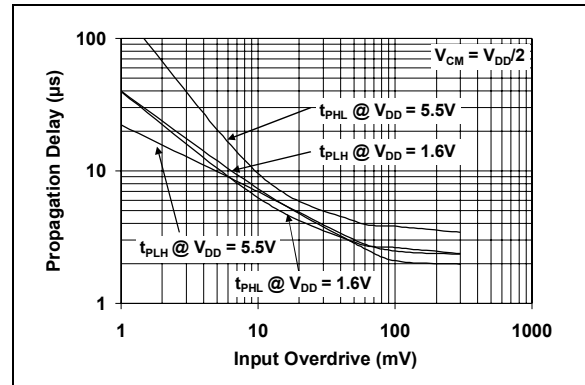
**FIGURE 2-24:** Propagation Delay vs. Temperature vs. Power Supply Voltage.



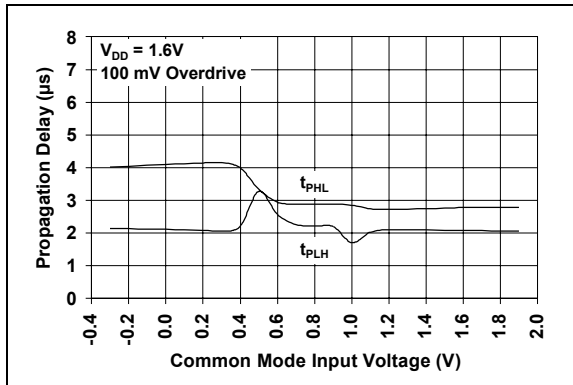
**Note:** Unless otherwise indicated,  $V_{DD} = +5.0V$ ,  $V_{SS} = GND$ ,  $T_A = 25^\circ C$ ,  $V_{IN+} = V_{DD}/2$ ,  $V_{IN-} = GND$ ,  $R_{PU} = 2.74\text{ k}\Omega$  to  $V_{PU} = V_{DD}$ , and  $C_L = 36\text{ pF}$ .



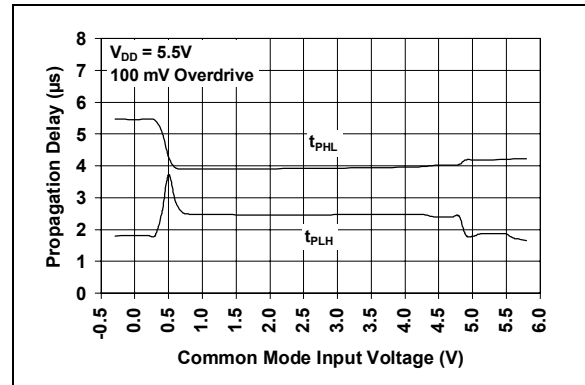
**FIGURE 2-25:** Propagation Delay vs. Power Supply Voltage vs. Input Overdrive.



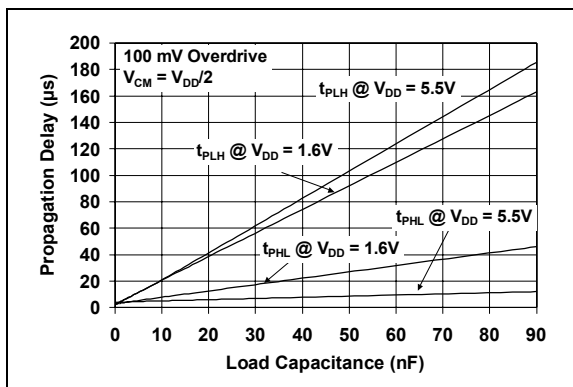
**FIGURE 2-28:** Propagation Delay vs. Input Overdrive vs. Power Supply Voltage.



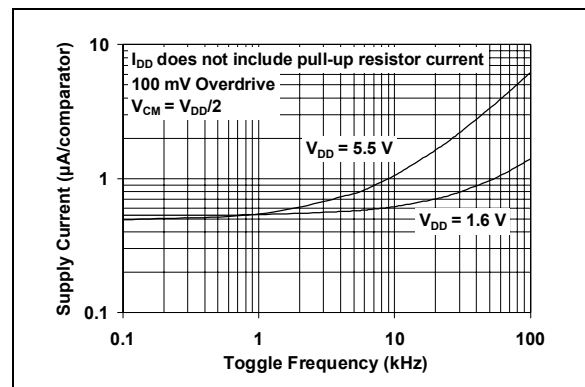
**FIGURE 2-26:** Propagation Delay vs. Common Mode Input Voltage with  $V_{DD} = 1.6V$ .



**FIGURE 2-29:** Propagation Delay vs. Common Mode Input Voltage with  $V_{DD} = 5.5V$ .



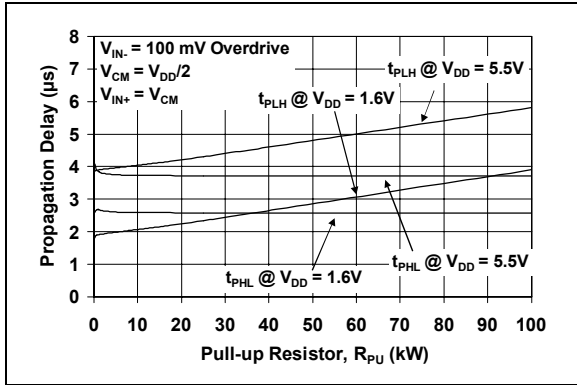
**FIGURE 2-27:** Propagation Delay vs. Load Capacitance vs. Power Supply Voltage.



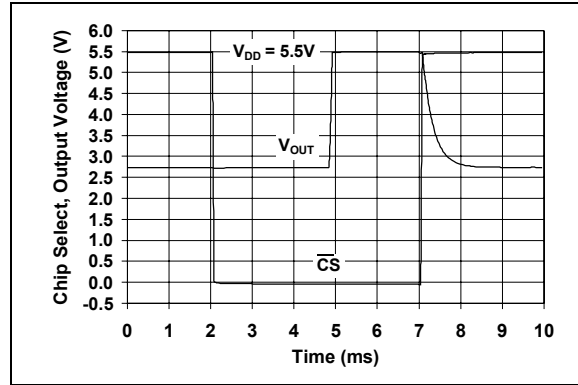
**FIGURE 2-30:** Supply Current vs. Toggle Frequency vs. Power Supply Voltage.

# MCP6546/7/8/9

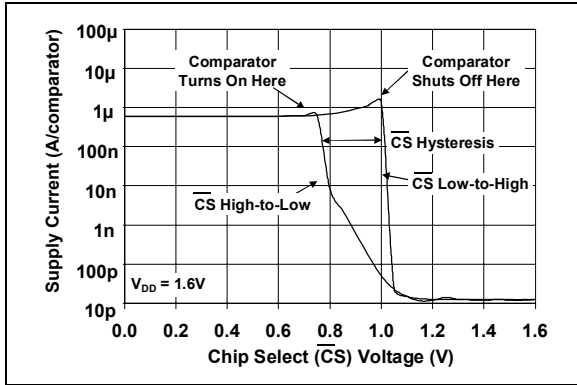
**Note:** Unless otherwise indicated,  $V_{DD} = +5.0V$ ,  $V_{SS} = GND$ ,  $T_A = 25^\circ C$ ,  $V_{IN+} = V_{DD}/2$ ,  $V_{IN-} = GND$ ,  $R_{PU} = 2.74\text{ k}\Omega$  to  $V_{PU} = V_{DD}$ , and  $C_L = 36\text{ pF}$ .



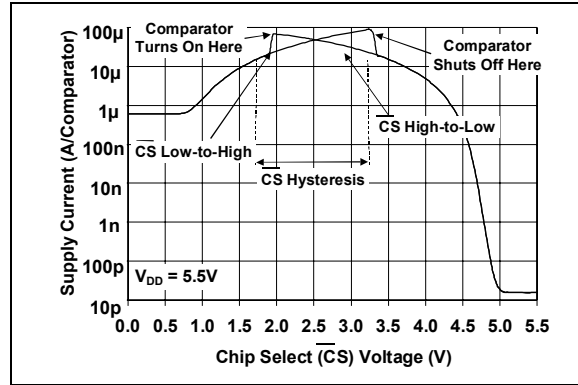
**FIGURE 2-31:** Propagation Delay vs. Pull-up Resistor vs. Power Supply Voltage.



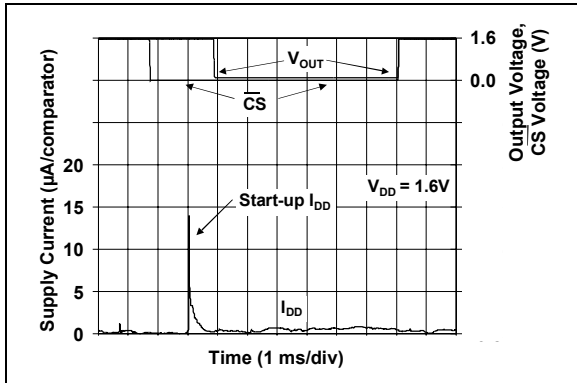
**FIGURE 2-34:** Chip Select ( $\overline{CS}$ ) Step Response (MCP6548 only).



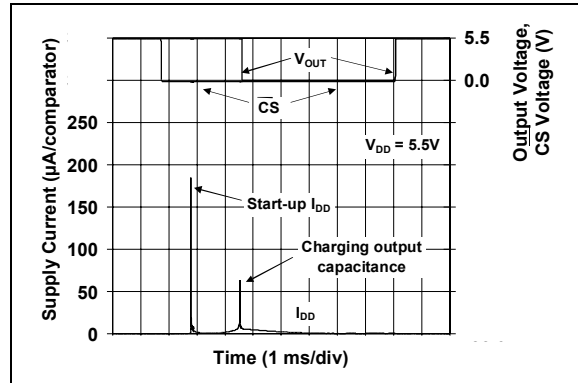
**FIGURE 2-32:** Supply Current (shoot through current) vs. Chip Select ( $\overline{CS}$ ) Voltage with  $V_{DD} = 1.6V$  (MCP6548 only).



**FIGURE 2-35:** Supply Current (shoot through current) vs. Chip Select ( $\overline{CS}$ ) Voltage with  $V_{DD} = 5.5V$  (MCP6548 only).

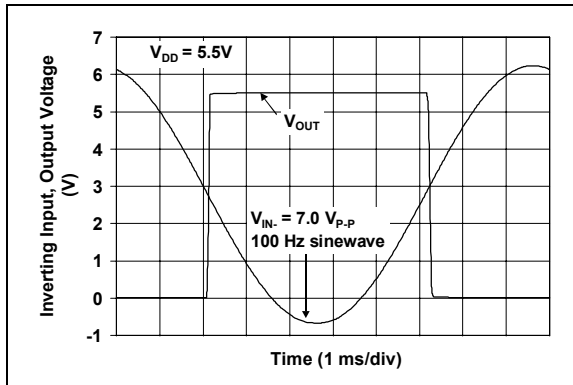


**FIGURE 2-33:** Supply Current (charging current) vs. Chip Select ( $\overline{CS}$ ) pulse with  $V_{DD} = 1.6V$  (MCP6548 only).

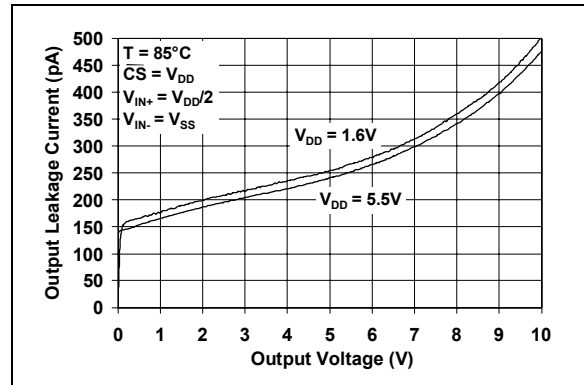


**FIGURE 2-36:** Supply Current (charging current) vs. Chip Select ( $\overline{CS}$ ) pulse with  $V_{DD} = 5.5V$  (MCP6548 only).

**Note:** Unless otherwise indicated,  $V_{DD} = +5.0V$ ,  $V_{SS} = GND$ ,  $T_A = 25^\circ C$ ,  $V_{IN+} = V_{DD}/2$ ,  $V_{IN-} = GND$ ,  $R_{PU} = 2.74\text{ k}\Omega$  to  $V_{PU} = V_{DD}$ , and  $C_L = 36\text{ pF}$ .



**FIGURE 2-37:** The MCP6546/7/8/9 comparators show no phase reversal.



**FIGURE 2-38:** Output Leakage Current ( $\overline{CS} = V_{DD}$ ) vs. Output Voltage vs. Power Supply Voltage (MCP6548 only)

# MCP6546/7/8/9

## 3.0 APPLICATIONS INFORMATION

The MCP6546/7/8/9 family of open-drain output comparators are fabricated on Microchip's state-of-the-art CMOS process. They are suitable for a wide range of applications requiring very low power consumption. A 0.1 mF bypass capacitor from the power supply pin to ground is recommended.

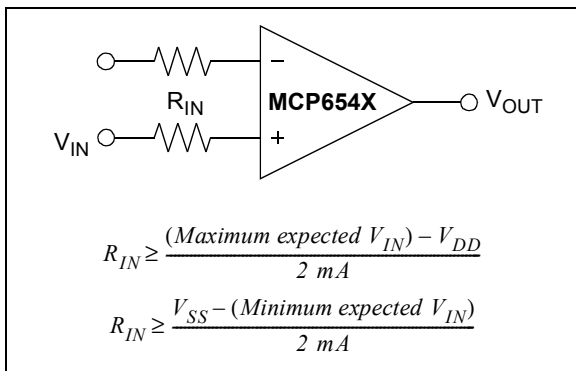
### 3.1 Rail-to-Rail Input

The input stage of this family of devices uses two differential input stages in parallel: one operates at low input voltages and the other at high input voltages. With this topology, the input voltage is +0.3V above  $V_{DD}$  and -0.3V below  $V_{SS}$ . The input offset voltage is measured at both  $V_{SS}-0.3V$  and  $V_{DD}+0.3V$  to ensure proper operation.

### 3.2 Input Voltage and Phase Reversal

The comparator family uses CMOS transistors at the input. They are designed to prevent phase inversion when the input pins exceed the supply voltages. Figure 2-37 shows an input voltage exceeding both supplies with no resulting phase inversion.

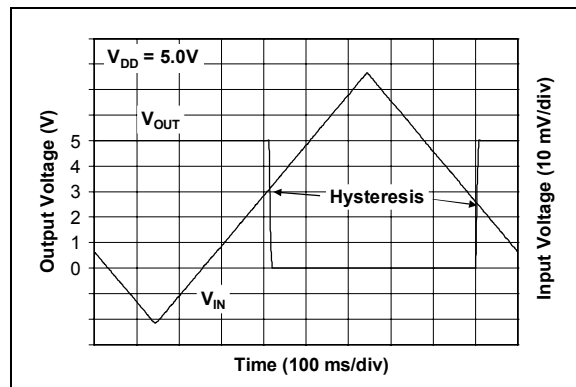
The maximum operating input voltages that can be applied are  $V_{SS}-0.3V$  and  $V_{DD}+0.3V$ . Voltages on the inputs that exceed this absolute maximum rating can cause excessive current to flow and permanently damage the device. In applications where the input pin exceeds the specified range, external resistors can be used to limit the current below  $\pm 2$  mA, as shown in Figure 3-1.



**FIGURE 3-1:** An input resistor ( $R_{IN}$ ) should be used to limit excessive input current if either of the inputs exceeds the Absolute Maximum specification.

## 3.3 Hysteresis

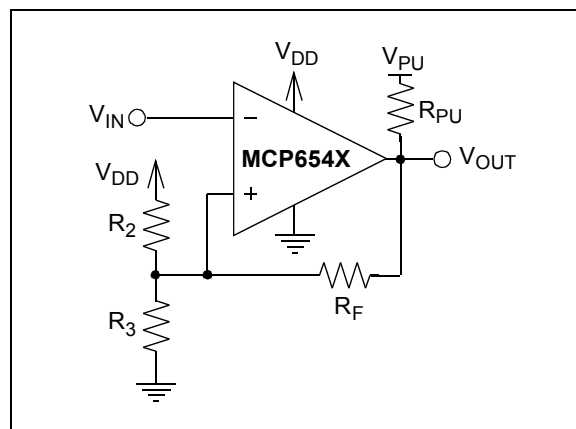
Input offset voltage ( $V_{OS}$ ) is the center (average) of the (input-referred) low-high and high-low trip points. Input hysteresis voltage ( $V_{HYST}$ ) is the difference between the same trip points. Hysteresis reduces output chattering when one input is slowly moving past the other, and thus reduces dynamic supply current. It also helps in systems where it is best not to cycle between states too frequently (e.g., air conditioner thermostatic control). The family has internally set hysteresis which is small enough to maintain input offset accuracy ( $<7$  mV), and large enough to eliminate output chattering caused by the comparator's own input noise voltage ( $200 \mu V_{p-p}$ ).



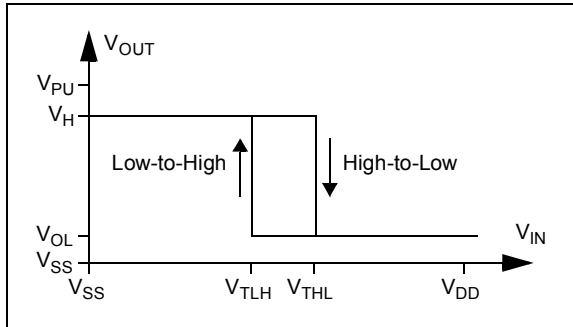
**FIGURE 3-2:** The MCP6546/7/8/9 comparators' internal hysteresis eliminates output chatter caused by input noise voltage.

### 3.3.1 INVERTING CIRCUIT

Figure 3-3 shows an inverting circuit for a single-supply application using three resistors, besides the pull-up resistor. The resulting hysteresis diagram is shown in Figure 3-4.



**FIGURE 3-3:** Inverting circuit with hysteresis.



**FIGURE 3-4:** Hysteresis diagram for the inverting circuit.

The trip points for Figures 3-3 and 3-4 are given by:

### EQUATION

$$R_{23} = R_2 \parallel R_3$$

$$V_{REF} = V_{DD} \left( \frac{R_3}{R_2 + R_3} \right)$$

$$V_H = V_{PU} \left( \frac{R_{23} + R_F}{R_{23} + R_F + R_{PU}} \right)$$

$$V_{THL} = V_{PU} \left( \frac{R_{23}}{R_{23} + R_F + R_{PU}} \right) + V_{REF} \left( \frac{R_F + R_{PU}}{R_{23} + R_F + R_{PU}} \right)$$

$$V_{TLH} = V_{OL} \left( \frac{R_{23}}{R_{23} + R_F} \right) + V_{REF} \left( \frac{R_F}{R_{23} + R_F} \right)$$

The output current required to drive  $V_{OL}$  is:

### EQUATION

$$I_O = \frac{V_{PU} - V_{OL}}{R_{PU}} + \frac{V_{REF} - V_{OL}}{R_{23} + R_F}$$

As explained in Section 3.2, it is important to keep the non-inverting input below  $V_{DD} + 0.3V$  when  $V_{PU} > V_{DD}$ .

## 3.4 The MCP6548 Chip Select ( $\overline{CS}$ ) Option

The MCP6548 is a single comparator with a chip select ( $\overline{CS}$ ) option. When  $\overline{CS}$  is pulled high, the total current consumption drops to 20 pA (typ). 1 pA (typ) flows through the  $\overline{CS}$  pin, 1 pA (typ) flows through the output pin and 18 pA (typ) flows through the  $V_{DD}$  pin, as shown in Figure 1-1. When this happens, the comparator output is put into a high-impedance state. By pulling  $\overline{CS}$  low, the comparator is enabled. If the  $\overline{CS}$  pin is left floating, the comparator will not operate properly. Figure 1-1 shows the output voltage and supply current response to a  $\overline{CS}$  pulse.

The internal  $\overline{CS}$  circuitry is designed to minimize glitches when cycling the  $\overline{CS}$  pin. This helps conserve power, which is especially important in battery-powered applications.

## 3.5 Open-Drain Output

The open-drain output is designed to make level-shifting and wired-OR logic easy to implement. The output can go as high as 10V for 9V battery-powered applications. The output stage minimizes switching current (shoot-through current from supply-to-supply) when the output changes state. See Figures 2-15, 2-17, 2-32 through 2-36 for more information.

## 3.6 Capacitive Loads

Reasonable capacitive loads (e.g., logic gates) have little impact on propagation delay (see Figure 2-27). The supply current increases with increasing toggle frequency (Figure 2-30), especially with higher capacitive loads.

## 3.7 Battery Life

In order to maximize battery life in portable applications, use large resistors and small capacitive loads. Also, avoid toggling the output more than necessary, and do not use chip select ( $\overline{CS}$ ) to conserve power for short periods of time. Capacitive loads will draw additional power at start-up.

## 3.8 Layout Considerations

Good PC board layout techniques will help you achieve the performance shown in the specs and Typical Performance Curves. It will also help you minimize EMC (Electro-Magnetic Compatibility) issues.

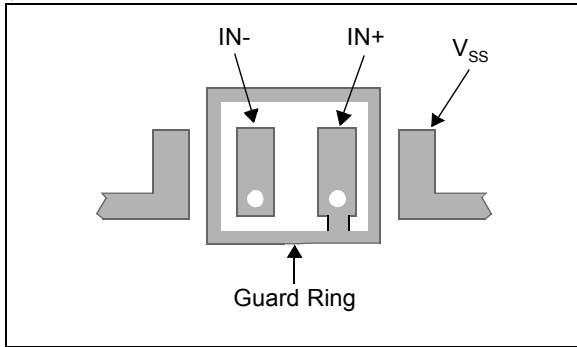
### 3.8.1 SURFACE LEAKAGE

In applications where low input bias current is critical, PC board surface leakage effects and signal coupling from trace-to-trace need to be considered.

Surface leakage is caused by a difference in voltage between traces, combined with high humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is  $10^{12}\Omega$ . A 5V difference would cause 5 pA of current to flow, which is greater than the input current of the family at 25°C (1 pA, typ).

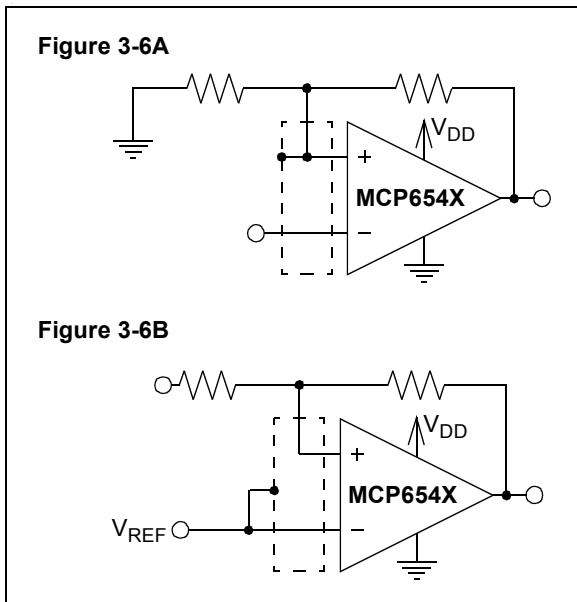
The simplest technique to reduce surface leakage is using a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin or trace. Figure 3-5 shows an example of a typical layout.

# MCP6546/7/8/9



**FIGURE 3-5:** Example of guard ring layout.

Circuit schematics for different guard ring implementations are shown in Figure 3-6. Figure 3-6A biases the guard ring to the input common mode voltage. Figure 3-6B biases the guard ring to a reference voltage ( $V_{REF}$  which can be ground). Place the guard ring on the node that is the most constant.



**FIGURE 3-6:** Two possible guard ring connection strategies to reduce surface leakage effects.

## 3.8.2 COMPONENT PLACEMENT

Separate digital from analog and low-speed from high-speed. This helps prevent crosstalk.

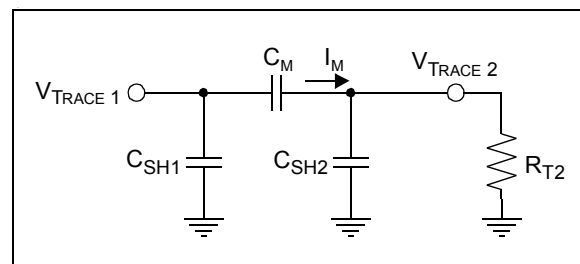
Keep sensitive traces short and straight. Separate them from interfering components and traces. This is especially important for high-frequency (low rise time) signals.

Use a 0.1  $\mu\text{F}$  supply bypass capacitor within 0.1" (2.5 mm) of the  $V_{DD}$  pin. It must connect directly to the ground plane.

## 3.8.3 SIGNAL COUPLING

The input pins of the MCP6546/7/8/9 family of comparators are high-impedance, which allows noise injection. This noise can be capacitively or magnetically coupled. In either case, using a ground plane helps reduce noise injection.

When noise is coupled capacitively, a ground plane reduces the coupling capacitance, and provides shunt capacitance to ground for high-frequency signals. Figure 3-7 shows the equivalent circuit. The coupled current ( $I_M$ ) produces a lower voltage ( $V_{TRACE 2}$ ) on the victim trace when the trace-to-ground plane capacitance ( $C_{SH2}$ ) is large, and the terminating resistor ( $R_{T2}$ ) is small. Increasing the distance between traces, and using wider traces, also helps.



**FIGURE 3-7:** Equivalent circuit for capacitive coupling between traces on a PC board (with ground plane).

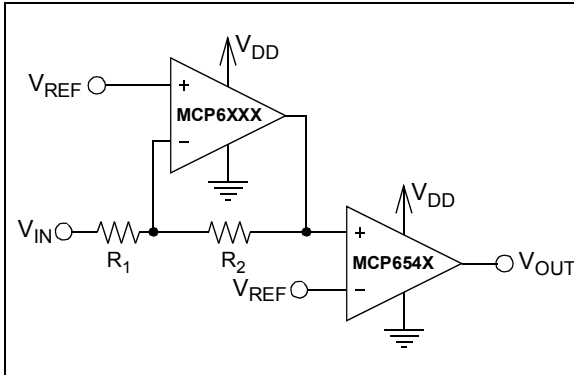
When noise is coupled magnetically, ground plane reduces the mutual inductance between traces. This occurs because the ground return current at high frequencies will follow a path directly beneath the signal trace. Increasing the separation between traces makes a significant difference. Changing the direction of one of the traces can also reduce magnetic coupling.

If these techniques are not enough, it may help to place guard traces next to the victim trace. They should be on both sides of the victim trace and be as close as possible. Connect the guard traces to ground plane at both ends, and in the middle for long traces.

## 3.9 Typical Applications

### 3.9.1 PRECISE COMPARATOR

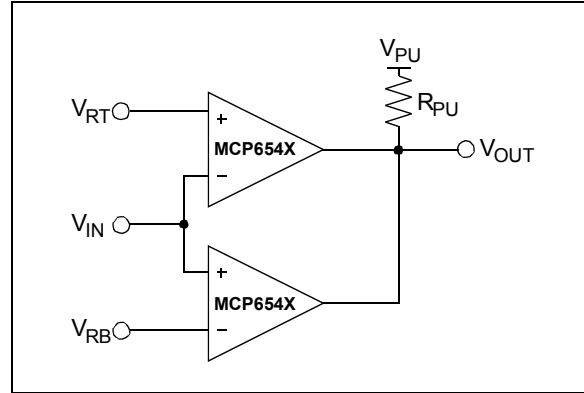
Some applications require higher DC precision. An easy way to solve this problem is to use an amplifier to gain up the input signal before it reaches the comparator. Figure 3-8 shows an example of this approach.



**FIGURE 3-8:** *Precise Inverting Comparator.*

### 3.9.2 WINDOWED COMPARATOR

Figure 3-9 shows one approach to designing a windowed comparator. The wired-OR connection produces a high output (logic 1) when the input voltage is between  $V_{RB}$  and  $V_{RT}$  (where  $V_{RT} > V_{RB}$ ).



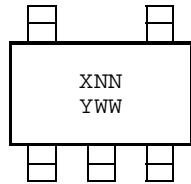
**FIGURE 3-9:** *Windowed comparator.*

# MCP6546/7/8/9

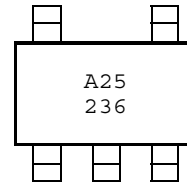
## 4.0 PACKAGING INFORMATION

### 4.1 Package Marking Information

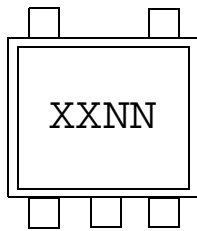
5-Lead SC-70 (MCP6546)



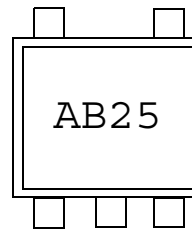
Example:



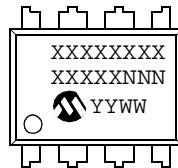
5-Lead SOT-23 (MCP6546)



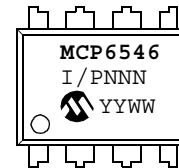
Example:



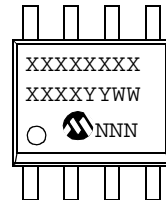
8-Lead PDIP (300 mil)



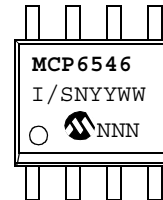
Example:



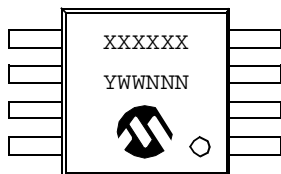
8-Lead SOIC (150 mil)



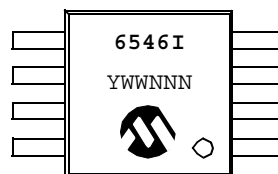
Example:



8-Lead MSOP



Example:



**Legend:** XX...X Customer specific information\*  
 YY Year code (last 2 digits of calendar year)  
 WW Week code (week of January 1 is week '01')  
 NNN Alphanumeric traceability code

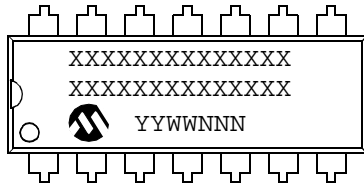
**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

\* Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

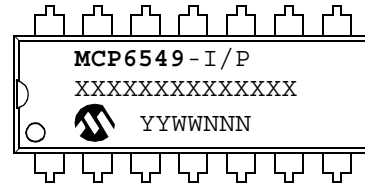


## Package Marking Information (Continued)

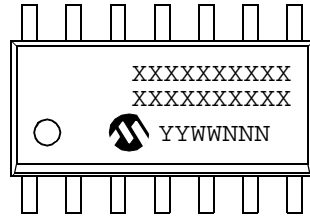
14-Lead PDIP (300 mil) (MCP6549)



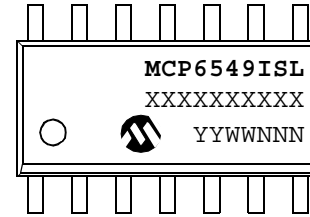
Example:



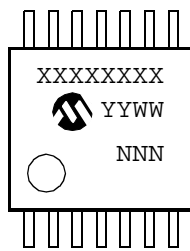
14-Lead SOIC (150 mil) (MCP6549)



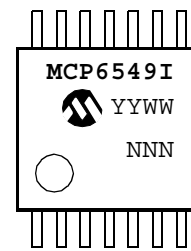
Example:



14-Lead TSSOP (MCP6549)

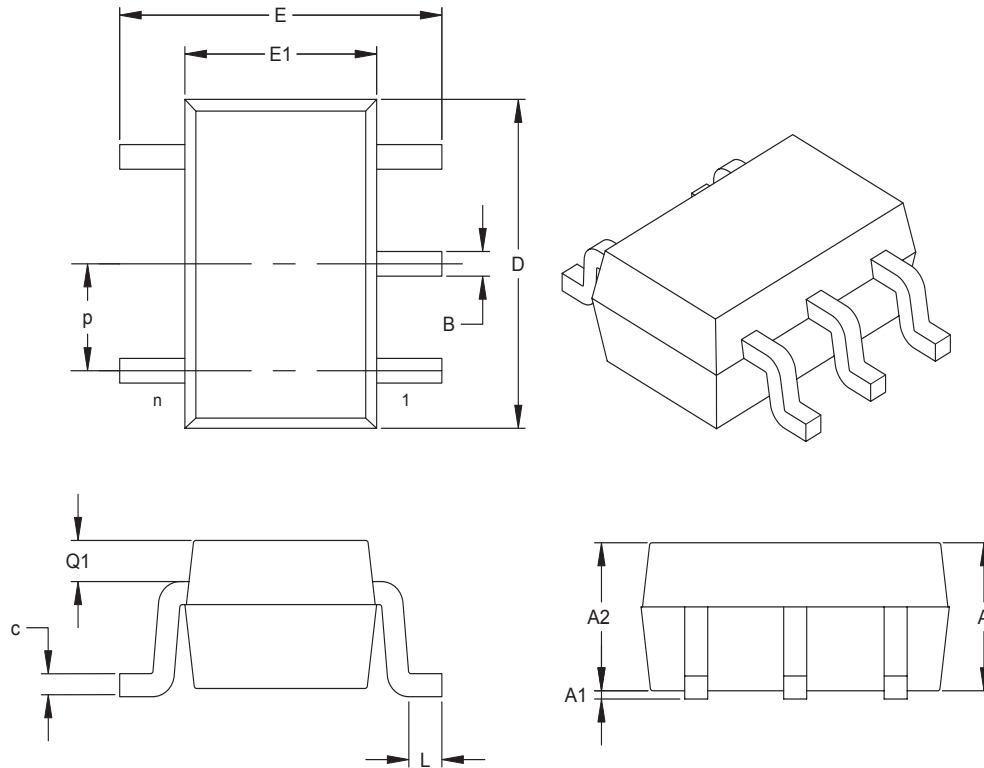


Example:



# MCP6546/7/8/9

## 5-Lead Plastic Package (LT) (SC-70)



Dimension Limits	Units	INCHES			MILLIMETERS*		
	n	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	5			5		
Pitch	p	.026 (BSC)			0.65 (BSC)		
Overall Height	A	.031		.043	0.80		1.10
Molded Package Thickness	A2	.031		.039	0.80		1.00
Standoff	A1	.000		.004	0.00		0.10
Overall Width	E	.071		.094	1.80		2.40
Molded Package Width	E1	.045		.053	1.15		1.35
Overall Length	D	.071		.087	1.80		2.20
Foot Length	L	.004		.012	0.10		0.30
Top of Molded Pkg to Lead Shoulder	Q1	.004		.016	0.10		0.40
Lead Thickness	c	.004		.007	0.10		0.18
Lead Width	B	.006		.012	0.15		0.30

\*Controlling Parameter

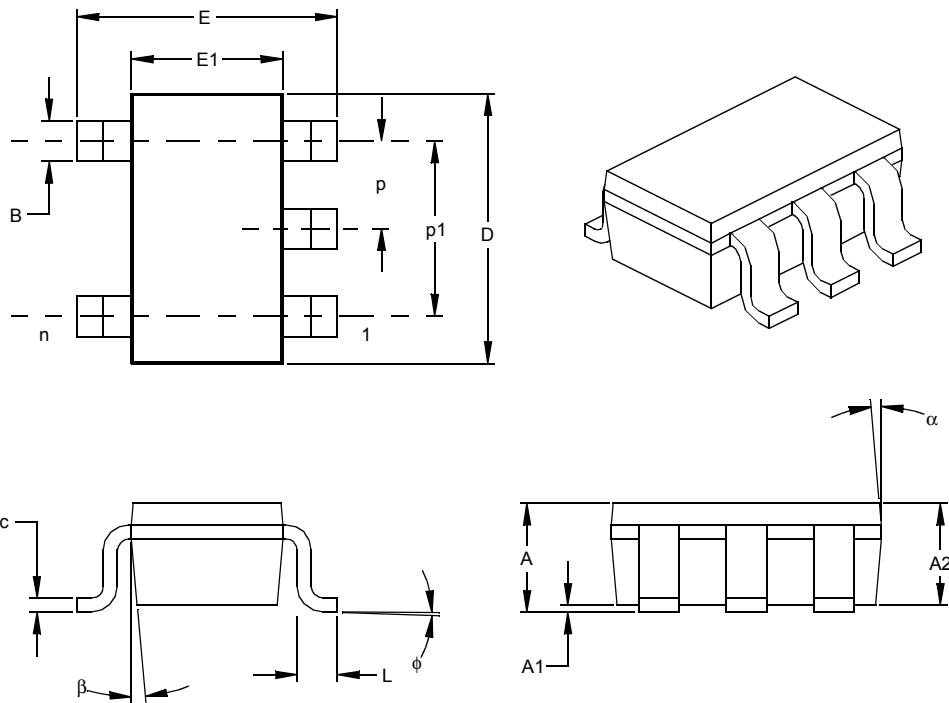
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEITA (EIAJ) Standard: SC-70

Drawing No. C04-061

## 5-Lead Plastic Small Outline Transistor (OT) (SOT23)



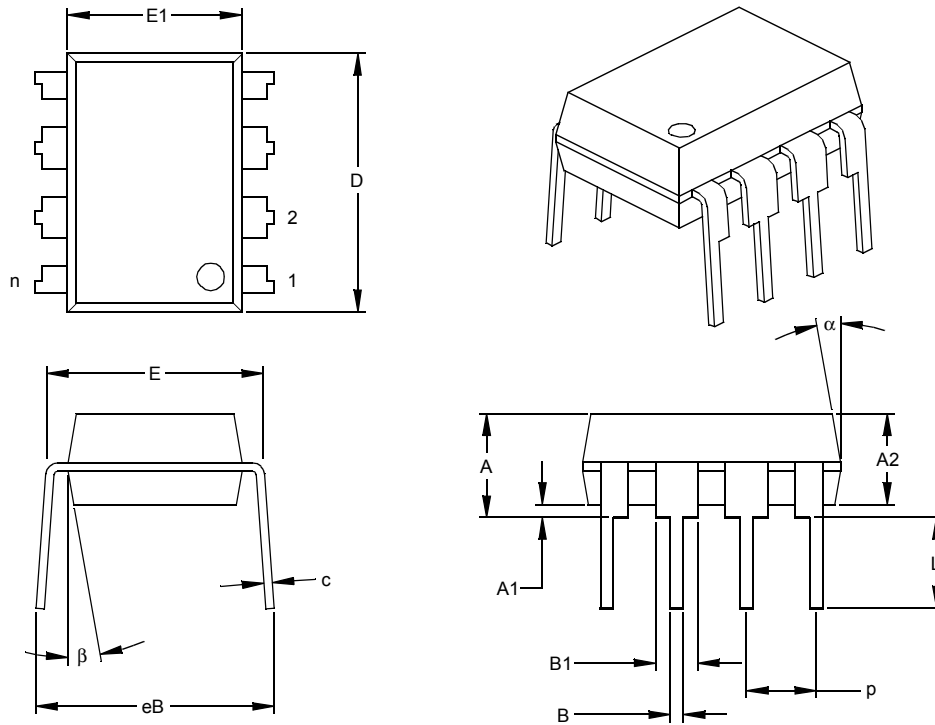
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		5			5	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff §	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	φ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

\* Controlling Parameter  
 § Significant Characteristic

Notes:  
 Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.  
 JEDEC Equivalent: MO-178  
 Drawing No. C04-091

# MCP6546/7/8/9

## 8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	a	5	10	15	5	10	15
Mold Draft Angle Bottom	b	5	10	15	5	10	15

\* Controlling Parameter

§ Significant Characteristic

### Notes:

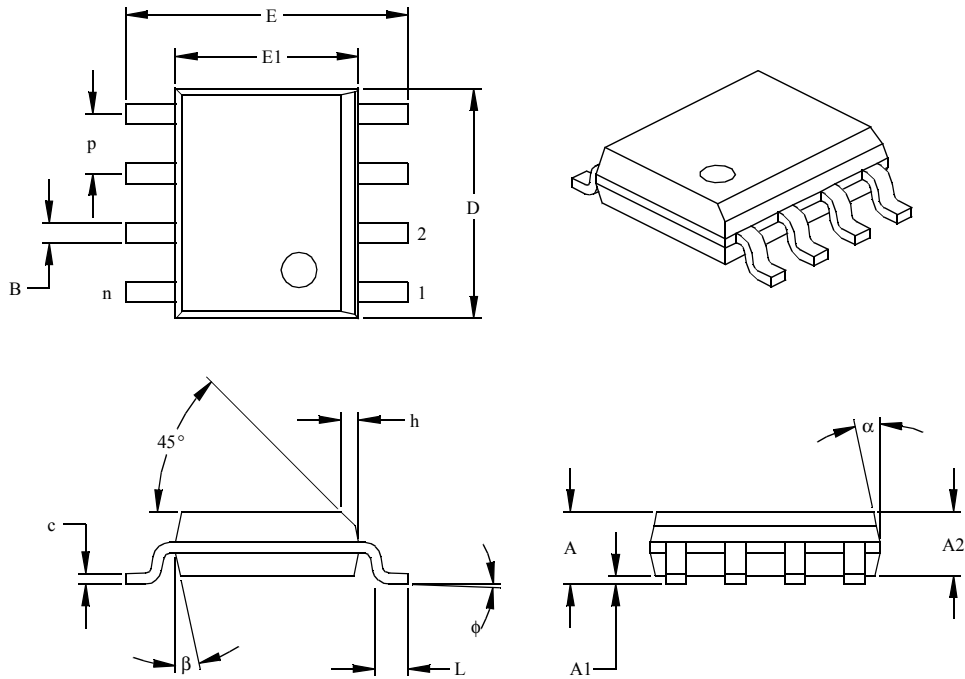
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-018

# MCP6546/7/8/9

## 8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

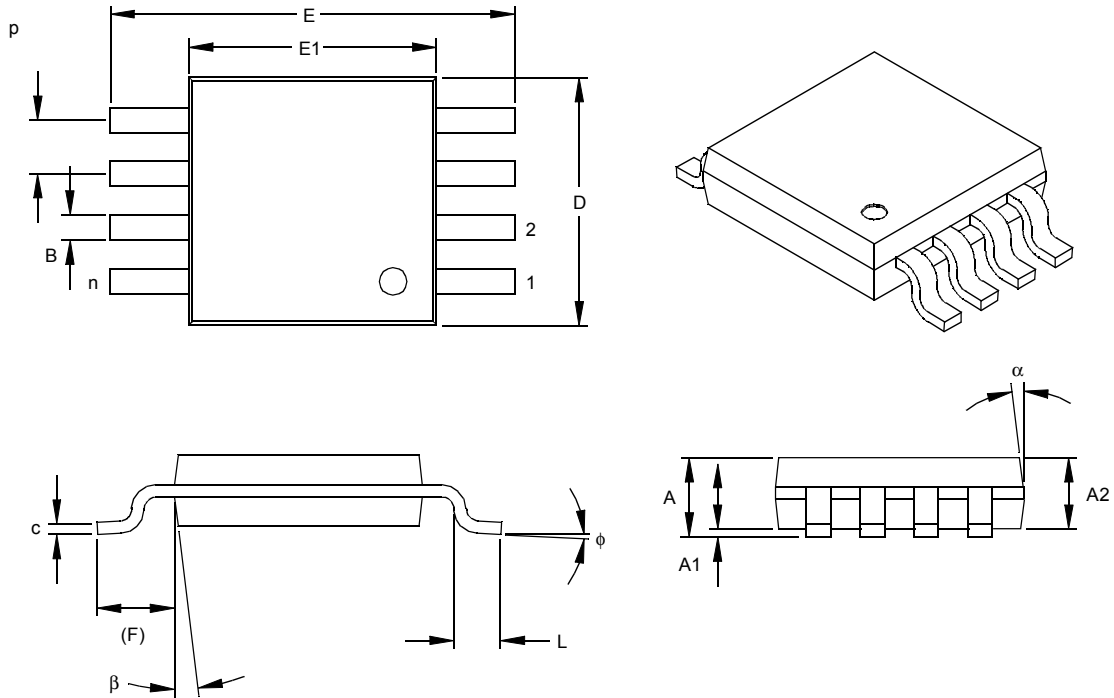
\* Controlling Parameter  
 § Significant Characteristic

**Notes:**

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.  
 JEDEC Equivalent: MS-012  
 Drawing No. C04-057

# MCP6546/7/8/9

## 8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8				8
Pitch	p	.026			0.65		
Overall Height	A			.044			1.18
Molded Package Thickness	A2	.030	.034	.038	0.76	0.86	0.97
Standoff §	A1	.002		.006	0.05		0.15
Overall Width	E	.184	.193	.200	4.67	4.90	5.08
Molded Package Width	E1	.114	.118	.122	2.90	3.00	3.10
Overall Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.016	.022	.028	0.40	0.55	0.70
Footprint (Reference)	F	.035	.037	.039	0.90	0.95	1.00
Foot Angle	φ	0		6	0		6
Lead Thickness	c	.004	.006	.008	0.10	0.15	0.20
Lead Width	B	.010	.012	.016	0.25	0.30	0.40
Mold Draft Angle Top	α		7			7	
Mold Draft Angle Bottom	β		7			7	

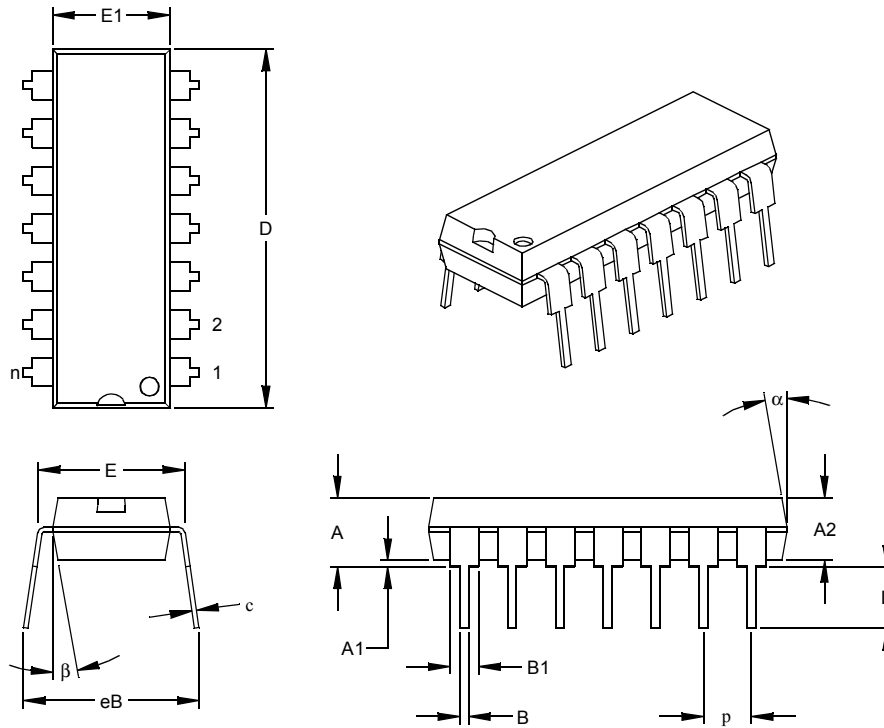
\*Controlling Parameter  
 § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

Drawing No. C04-111

## 14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

\* Controlling Parameter

§ Significant Characteristic

Notes:

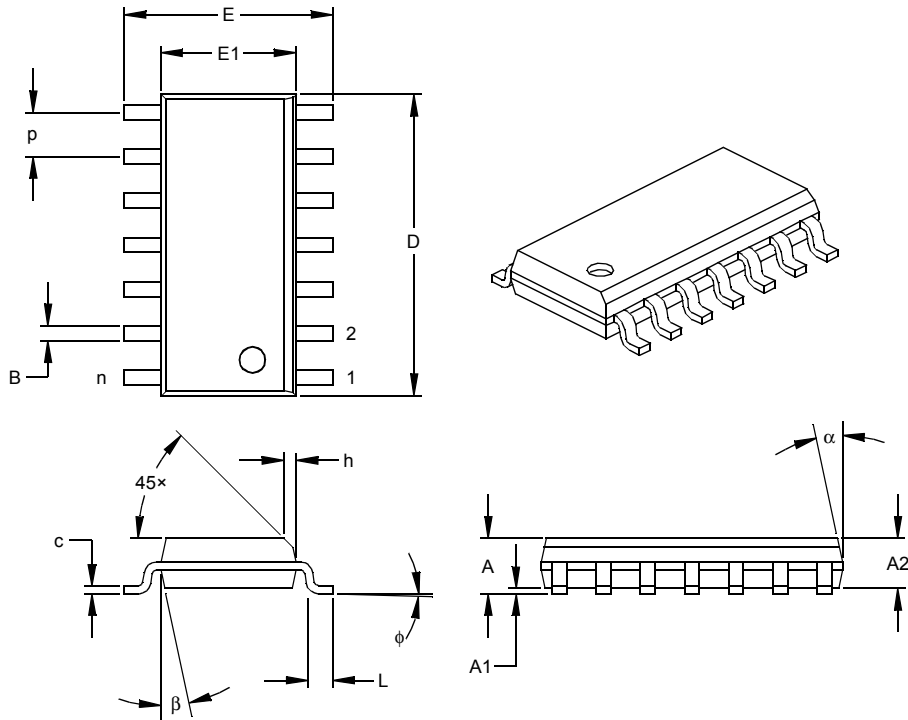
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-005

# MCP6546/7/8/9

## 14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter

§ Significant Characteristic

Notes:

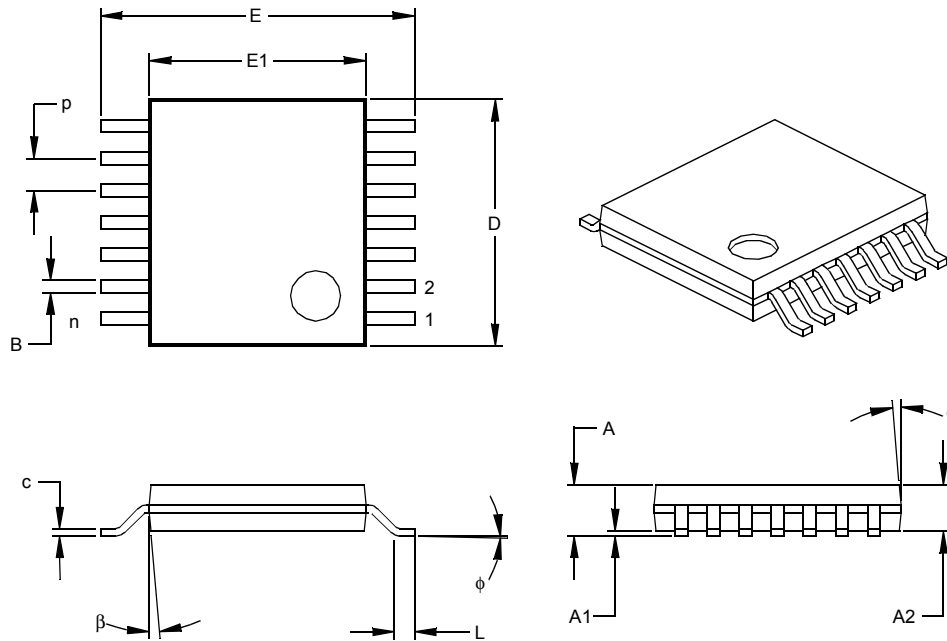
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-065



## 14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Dimension Limits	Units	INCHES			MILLIMETERS*		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B1	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

\* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEDEC Equivalent: MO-153

Drawing No. C04-087

# MCP6546/7/8/9

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>-X</u>	<u>/XX</u>	
Device	Temperature Range	Package	
Device:	MCP6546:	Single Comparator	
	MCP6546T:	Single Comparator (Tape and Reel) (SC-70, SOT-23, SOIC, MSOP)	
	MCP6547:	Dual Comparator	
	MCP6547T:	Dual Comparator (Tape and Reel for SOIC and MSOP)	
	MCP6548:	Single Comparator with <u>CS</u>	
	MCP6548T:	Single Comparator with <u>CS</u> (Tape and Reel for SOIC and MSOP)	
	MCP6549:	Quad Comparator	
	MCP6549T:	Quad Comparator (Tape and Reel for SOIC and TSSOP)	
Temperature Range:	I	= -40°C to +85°C	
Package:	LT	= Plastic Package (SC-70), 5-lead	
	OT	= Plastic Small Outline Transistor (SOT-23), 5-lead	
	MS	= Plastic MSOP, 8-lead	
	P	= Plastic DIP (300 mil Body), 8-lead, 14-lead	
	SN	= Plastic SOIC (150 mil Body), 8-lead	
	SL	= Plastic SOIC (150 mil Body), 14-lead (MCP6549)	
	ST	= Plastic TSSOP (4.4mm Body), 14-lead (MCP6549)	
			<b>Examples:</b>
			a) MCP6546T-I/LT: 5LD SC-70, Tape and Reel.
			b) MCP6546T-I/OT: 5LD SOT-23, Tape and Reel.
			c) MCP6546-I/P: 8LD PDIP.
			a) MCP6547-I/MS: 8LD MSOP.
			b) MCP6547T-I/MS: 8LD MSOP, Tape and Reel.
			c) MCP6547-I/P: 8LD PDIP.
			a) MCP6548-I/SN: 8LD SOIC.
			b) MCP6548T-I/SN: 8LD SOIC, Tape and Reel.
			c) MCP6548-I/P: 8LD PDIP.
			a) MCP6549T-I/SL: 14LD SOIC, Tape and Reel.
			b) MCP6549T-I/SL: 14LD SOIC, Tape and Reel.
			c) MCP6549-I/P: 14LD PDIP.

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# MCP6546/7/8/9

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NOTES:

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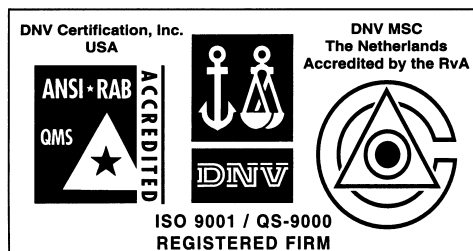
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