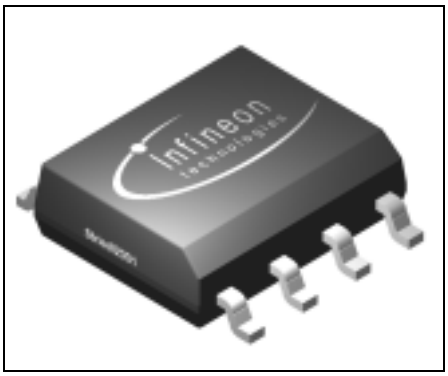
Smart Dual Lowside Power Switch HITFET® BTS3408G

Data Sheet V1.0

Features



- Logic Level Input
- Compatible to 3V micro controllers
- ESD protection
- Thermal shutdown with auto restart
- Overload protection
- Short circuit protection
- Over voltage protection
- Open load detection (during Off)
- Current limitation
- Direct parallel control of the inputs
- FREEZE functionality for multiplexing
- General fault flag
- Very low standby quiescent current
- Switching frequencies up to 50kHz

Application

- All kinds of resistive, inductive and capacitive loads in switching applications
- µC compatible power switch for 12 V, 24 V and 42 V applications
- Replaces electromechanical relays and discrete circuits
- Line, stepper motor, lamp and relay driver

General Description

The BTS3408G is a dual channel Low-Side Switch with D-MOS output stages for driving resistive, capacitive and inductive loads. The design is based on Infineons Smart Power Technology (SPT) which allows bipolar, CMOS and power D-MOS devices on the same monolithic circuit.

The BTS3408RS is protected by embedded protection functions and designed for automotive and industrial applications. It is especially suited for driving stepper motors and lines.

Type	Ordering Code	Package
HITFET® BTS3408G	Q67006-A9570-A001	P-DSO-8-3

Product Summary

Parameter	Symbol	Value	Unit
Supply voltage	V_S	4.5 - 60	V
Continuous drain source voltage	V_{DS}	60	V
On-state resistance	$R_{DS(ON)}$	550	mΩ
Current limitation	$I_{D(lim)}$	1	A
Nominal output current (individual channel)	$I_{D(Nom)}$	0.55	A
Clamping energy	E_{AS}	800	mJ

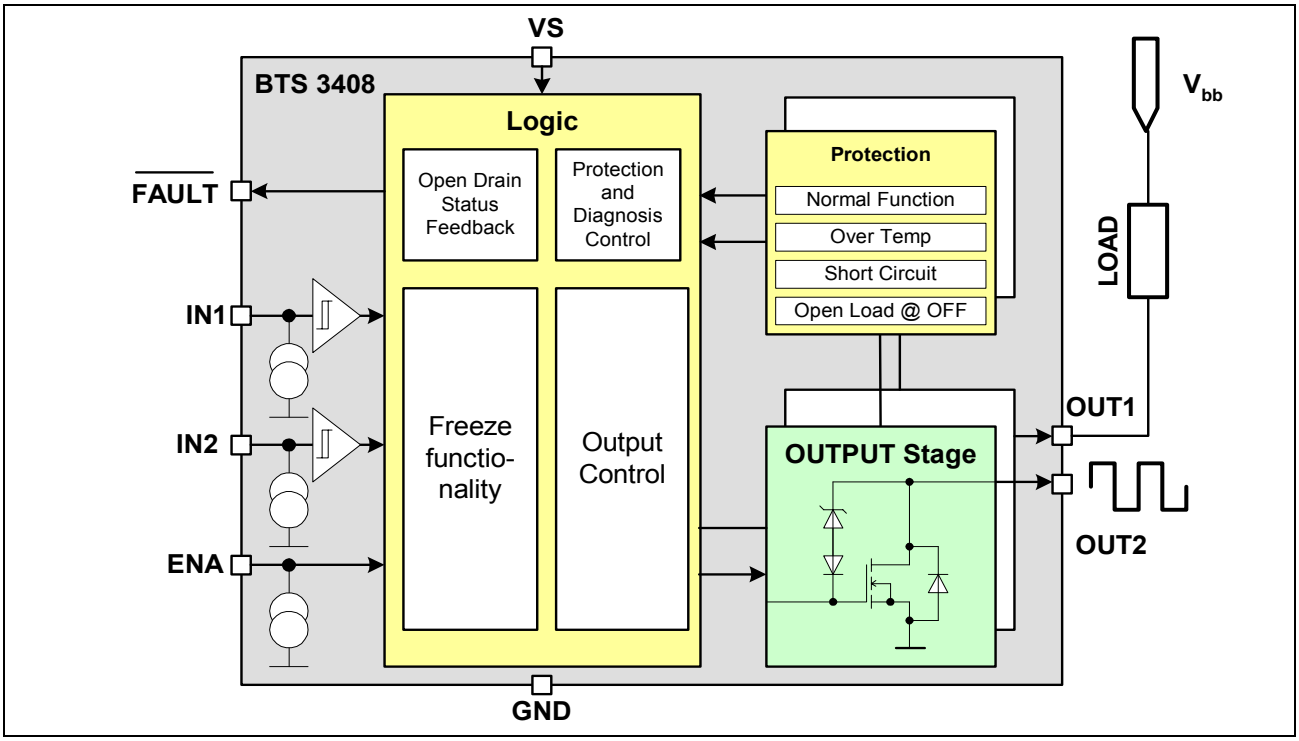


Figure 1 Block Diagram

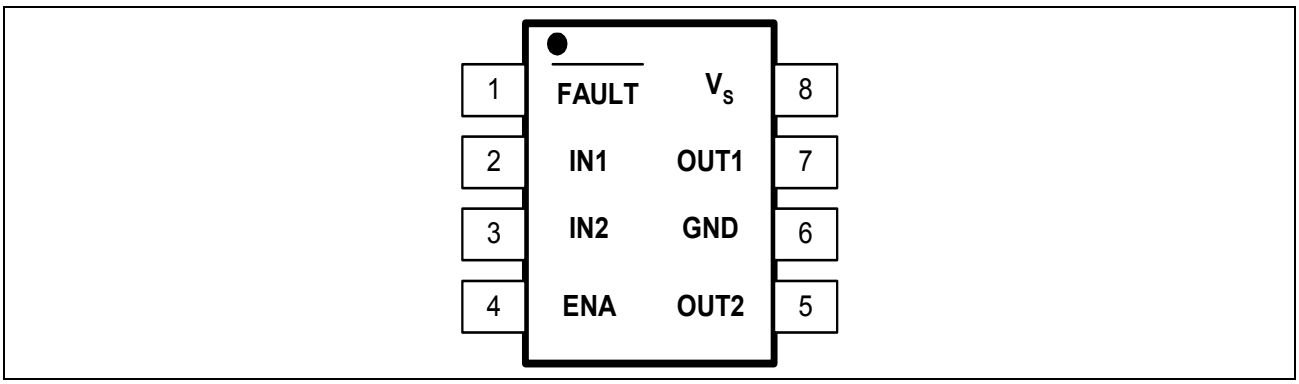


Figure 2 Pin Configuration

Pin Definitions and Functions

Pin	Symbol	Function
1	$\overline{\text{FAULT}}$	**General Fault Flag**; see Table 2 for operation mode.
2	IN1	**Input 1**; input of channel 1; has an internal pull down; TTL/ CMOS compatible input.
3	IN2	**Input 2**; input of channel 2; has an internal pull down; TTL/ CMOS compatible input.
4	ENA	**Enable/Freeze**; has an internal pull down; device is enabled when voltage is higher then 1.2 Volts; if the voltage is below 1.7 Volts the output is freezed, input signals will be ignored; if the voltage is above 2 Volts input signals will be output ; see Table 1 for detailed information.
5	OUT2	**Output 2**; output of D-MOS stage 2.
6	GND	**Ground.**
7	OUT1	**Output 1**; output of D-MOS stage 1.
8	V_S	**Power supply**.

Circuit Description

Logic Supply

The logic is supplied with 4.5 up to 60 Volt by the V_S pin. If V_S falls below max. 4.5 Volts the logic is shut down and the output stages are switched off.

Direct Inputs

ENA

The ENA/FREEZE input can be used to enable and/or to freeze the output control of the IC or to cut off the complete IC.

By pulling the ENA input to low, i.e. applying a Voltage V_{ENAL} , the IC is in disable mode. The power stages are switched off and the current consumption is reduced to $I_{S(stby)}$.

By applying a Voltage V_{ENAFZ}, the IC is in FREEZE mode. The output signals will remain in their former state. All input signals will be ignored.

By pulling the input to high, the IC is in Enable mode. All input signals are output.

The ENA - pin has an internal pull-down.

IN1 / IN2

Each output is independently controlled via the respective input pin. The input pins are high active. If the common enable pin is high, the individual input signals are output. The input pins have an internal pull-down.

Table 1 Functional Table

V_{ENA}	Mode	IN1	IN2	IN1(-1)	IN2(-1)	OUT1	OUT2	Comment
≤0.8V	Disable	X [1]	X [1]	X [1]	X [1]	L	L	all outputs OFF
1.2 .. 1.7V	Freeze	X [1]	X [1]	L	L	L	L	former output state
1.2 .. 1.7V	Freeze	X [1]	X [1]	L	H	L	H	former output state
1.2 .. 1.7V	Freeze	X [1]	X [1]	H	L	H	L	former output state
1.2 .. 1.7V	Freeze	X [1]	X [1]	H	H	H	H	former output state
≥2.0V	Enable	L	L	X [1]	X [1]	L	L	input is output
≥2.0V	Enable	L	H	X [1]	X [1]	L	H	input is output
≥2.0V	Enable	H	L	X [1]	X [1]	H	L	input is output
≥2.0V	Enable	H	H	X [1]	X [1]	H	H	input is output

[1] X = not relevant

Power stages

Each output is protected by embedded protection functions. In the event of an overload or short to supply, the current is internally limited. The current limit is set to $I_{D(lim)}$. If this operation leads to an overtemperature condition, a second protection level (about 165 °C) will turn the effected output into a PWM-mode (selective thermal shutdown with restart) to prevent critical chip temperatures. The temperature hysteresis is typically 10K.

Zener clamping is implemented to limit voltages at the power transistors when inductive loads are switched off.

Diagnostic

The general $\overline{\text{FAULT}}$ pin is an open drain output. The $\overline{\text{FAULT}}$ pin is low active. It signals fault conditions of any of the two output stages. By doing so, single and/or dual fault conditions can be monitored. Single fault conditions can be assigned.

Table 2 Diagnostic Table

Operating Condition	ENA	IN_X	OUT_X	$\overline{\text{FAULT}}$
Standby	L	X [1]	OFF	H
Normal function	H	H	ON	H
Over temperature	H	H	OFF [2]	L
Open load / short to ground	H	L	OFF	L

[1] X = not relevant

[2] selective thermal shutdown for each channel at overtemperature

Fault Distinction

Open load / short to ground is recognized during OFF-state. Overtemperature as a result of an overload or short to battery can only arise during ON-state. If there is only one fault at a time, it is possible to distinguish which channel is affected with which fault.

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Absolute Maximum Ratings [1)]

T_j = -40°C to 150°C , unless otherwise specified

Parameter	Symbol	Values	Unit	Remarks
Supply Voltage	V_S	+4.5 .. +60	V	–
Drain source voltage (OUT1, OUT2)	V_{DS}	-0.3 .. +60	V	–
Input voltage (IN1, IN2, ENA)	V_{IN}	-0.3 … +7	V	–
Continuous input current V_{IN}>7V	I_{IN}	1	mA	–
$\overline{\text{FAULT}}$ output voltage	V_{Fault}	-0.3 … +7	V	–
Operating temperature range Storage temperature range	T_j T_{stg}	-40 … +150 -55 … +150	°C °C	–
Power dissipation (DC) [2)]	P_{tot}	0.88	W	–
Nominal load current [2)] one channel active both channel active	$I_{D(Nom)}$	 0.55 0.45	A	V_{DS}≤0.5V, T_j≤150°C, T_A=85°C, V_{IN}=5V
Unclamped single pulse inductive energy one channel active	E_{AS}	800	mJ	I_D=0.7A, $T_{j(start)}$=25°C
Electro**s**tatic **d**ischarge voltage (Human Body Model) according to MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1 - 1993	V_{ESD}	2000	V	–
DIN humidity category, DIN 40 040	–	E	–	–
IEC climatic category, DIN IEC 68-1	–	40/150/56	–	–

Thermal Resistance

Junction soldering point	R_{thJS}	≤ 10	K/W	–
Junction - ambient @ min. footprint Junction - ambient @ 6cm² cooling area [2)]	R_{thJA}	≤ 185 ≤ 142	K/W	–

1) Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2) Device on epoxy pcb 40 mm × 40 mm × 1.5 mm with 6 cm² copper area for pin 4 connection.

Electrical Characteristics

V_S = 4.5 to 18V; T_j = -40 to 150°C; unless otherwise specified

Parameter	Sym-bol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Power supply						
Supply voltage	V_S	4.5	–	60	V	–
Supply current in enable mode	$I_{S(ON)}$	–	1.5	4	mA	ENA=High, OUT1=OUT2=On
Supply current in standby mode [1]	$I_{S(stby)}$	–	–	16	µA	ENA=Low
Power outputs						
Drain source clamp voltage	$V_{DS(AZ)}$	60	–	75	V	I_D = 1 mA
Output leakage current [2]	I_{DSS}	–	1	5	µA	ENA=Low, IN=Low, V_{DS} = 60 V
Output pull down current	$I_{PD(OL)}$	50	100	200	µA	ENA=High, IN=Low, V_{DS} = 42 V
On-state resistance T_j = 25 °C T_j = 150 °C	$R_{DS(on)}$	 – –	 480 800	 550 1000	mΩ	I_D = 0.2 A, V_S = 5 V
Current limit	$I_{D(lim)}$	1	1.5	2	A	–
Turn-on time IN=High to 90% I_D:	t_{on}	–	2	8	µs	R_L=2kΩ, V_{BB}=12V, V_S=5V
Turn-off time IN=Low to 10% I_D:	t_{on}	–	2	8	µs	R_L=2kΩ, V_{BB}=12V, V_S=5V
Digital inputs (IN1, IN2, ENA)						
Input 'Low' voltage IN1, IN2: ENA:	 V_{INL} V_{ENAL}	 -0.3 -0.3	 – –	 0.8 0.8	V	–
ENA voltage for 'FREEZE' functionality	V_{ENAFZ}	1.2	–	1.7	V	–

Electrical Characteristics (cont'd)
V_S = 4.5 to 18V; T_j = -40 to 150°C; unless otherwise specified

Parameter	Sym-bol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Input 'High' voltage IN1, IN2: ENA:	 V_{INH} V_{ENAH}	 2.0 2.0	 – –	 – –	V	–
Input voltage hysteresis	V_{INhys}	–	300	–	mV	–
Input pull down current IN1, IN2: ENA:	 I_{INPD} I_{ENAPD}	 20 20	 50 50	 100 100	µA	–
Digital Output ($\overline{FAULT}$)						
Output 'Low' voltage	V_{FLTL}	–	–	0.4	V	I_{FLTL}=1.6mA,
Diagnostic Functions						
Open load / short to ground detection voltage	$V_{DS(OL)}$	0.5*V_S	0.7*V_S	0.9*V_S	V	–
Fault filter time for open load	$t_{filter(OL)}$	30	100	200	µs	V_S=5V
Protection Functions [3]						
Thermal overload trip temperature	T_{jt}	150	165	180	°C	–
Thermal hysteresis	ΔT_{jt}	–	10	–	K	–
Unclamped single pulse inductive energy one channel active, $T_{j(start)}$=25°C both channel active, $T_{j(start)}$=25°C one channel active, $T_{j(start)}$=150°C both channel active, $T_{j(start)}$=150°C	E_{AS}			 800 550 240 240	mJ	I_D=0.7 A

[1] See also diagram 4 on page 14.

[2] See also diagram 5 on page 14.

[3] Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

EMC-Characteristics

The following EMC-Characteristics outline the behavior of typical devices. They are not part of any production test.

Table 3 Test Conditions

Parameter	Symbol	Value	Unit	Remark
Temperature	T_A	23 ±5	°C	–
Supply Voltage	V_{BB}	13.5	V	–
Input Voltage (ENA, IN1, IN2)	V_{INx}	5	V	–
Load	R_{L1} , R_{L2}	27	Ω	ohmic
Operation mode	PWM DC	– –	– –	f_{INx}=100Hz, D=0.5 ON / OFF
DUT specific	all tests with ENA=HIGH			

Fast electrical transients

acc. to ISO 7637

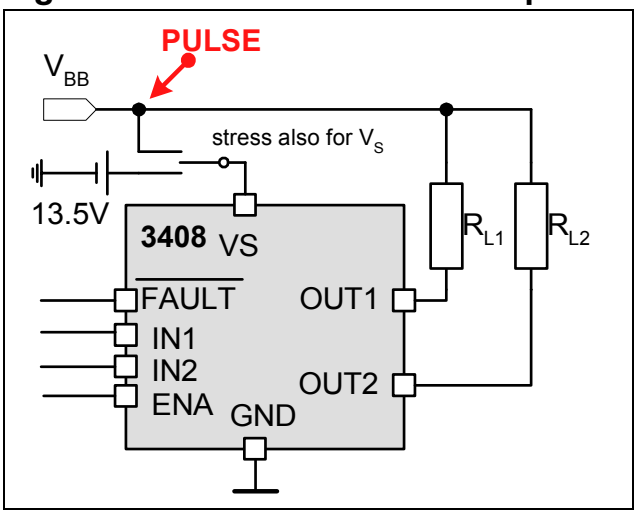
Test[1] Pulse	Max. Test Level	Test Result				Pulse Cycle Time and Generator Impedance
		V_S and OUT_x stressed		OUT_x stressed		
		ON	OFF	ON	OFF	
1	-200V	E(-120V)	E(-120V)	C	C	500ms ; 10Ω
2	+200V	E(+120V	E(+120V	C	C	500ms ; 10Ω
3a	-200V	C	C	C	C	100ms ; 10Ω
3b	+200V	C	C	C	C	100ms ; 10Ω
4	-7V	C	C	C	C	0.01Ω
5	175V	E(50V)	E(65V)	E(70V)	E(75V)	400ms ; 2Ω

[1] The test pulses are applied at V_{BB}

Definition of functional status

Class	Content
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more function of a device does not perform as designed after exposure and can not be returned to proper operation without repairing or replacing the device. The value after the character shows the limit.

Figure 3 Test circuit for ISO pulse



Conducted Emissions

Acc. IEC 61967-4 (1Ω/150Ω method)

Typ. OUT_x Emissions at PWM-mode with 150Ω-matching network

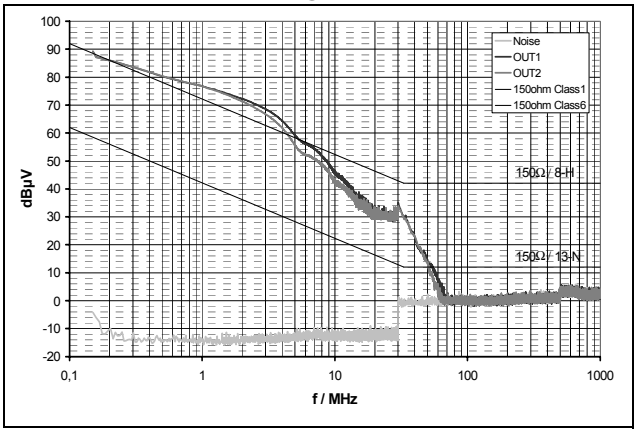
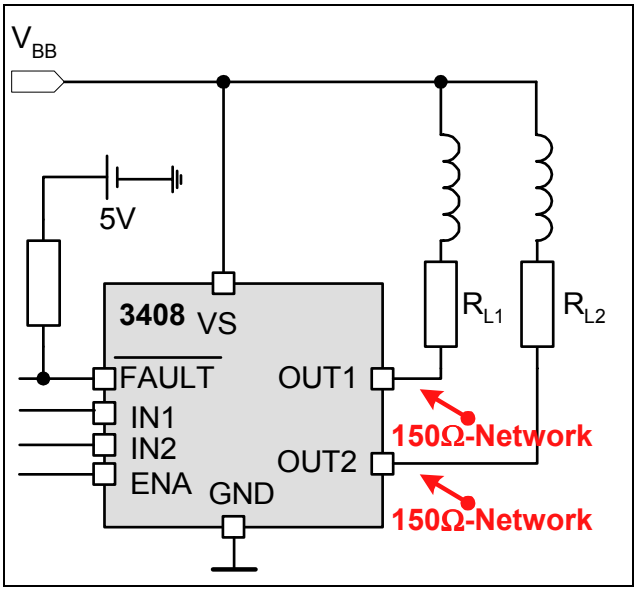


Figure 4 Test circuit for conducted emission [1)]



Conducted Susceptibility

Acc. I47A/658/CD IEC 62132-4 (Direct Power Injection)

Direct Power Injection: Forward Power CW

Failure Criteria: Amplitude or frequency variation max. 10% at OUT

Typ. OUT_x Susceptibility at DC-ON/OFF and at PWM

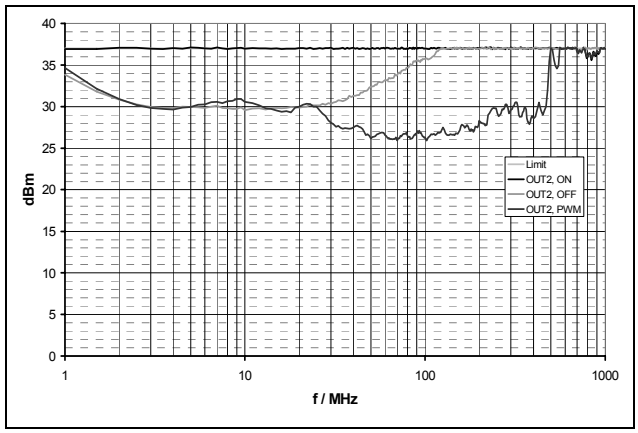
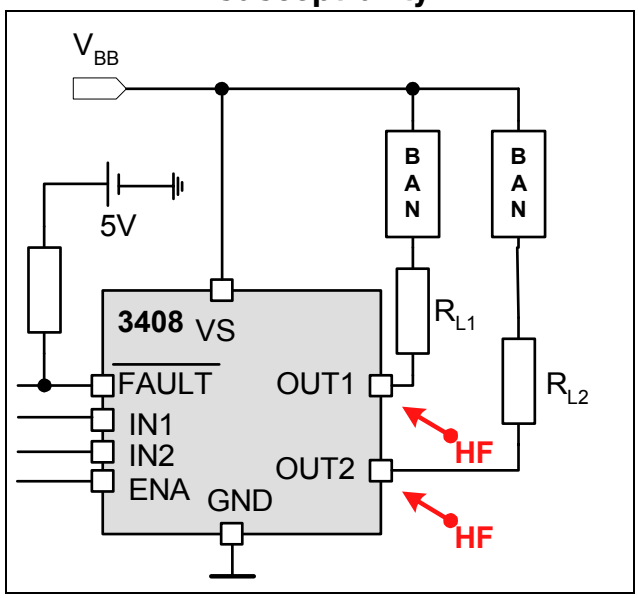


Figure 5 Test circuit for conducted susceptibility [2)]



[1)] For defined decoupling and high reproducibility a defined choke (5µH at 1 MHz) is inserted between Vbb and Out-Pin.

[2)] Broadband Artificial Network (short BAN) consists of the same choke (5µH at 1 MHz) and the same 150ohm-matching network as for emission measurement for defined decoupling and high reproducibility.

Terms

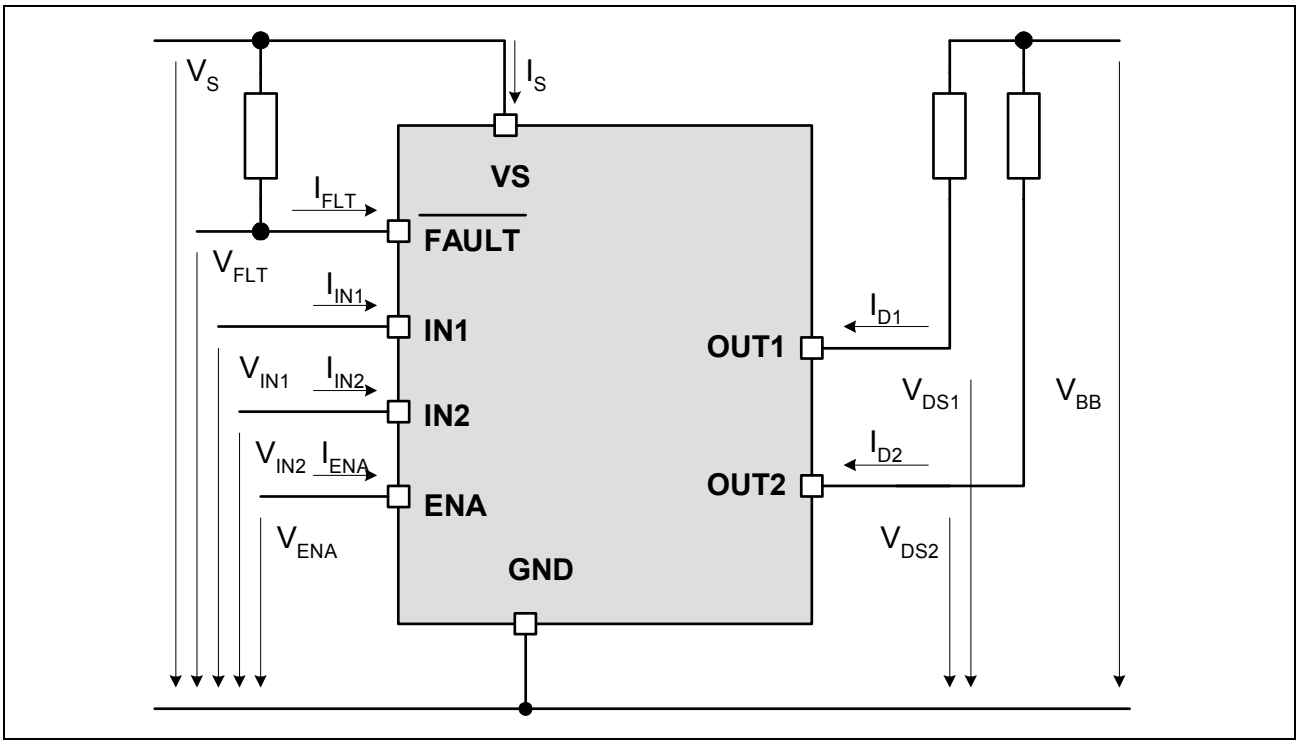
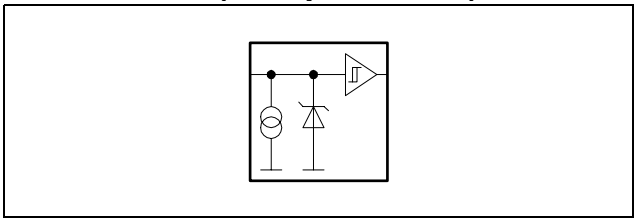


Figure 6 Input circuit (ESD protection)



ESD zener diodes are not designed for DC current.

Figure 7 Inductive and over voltage output clamp

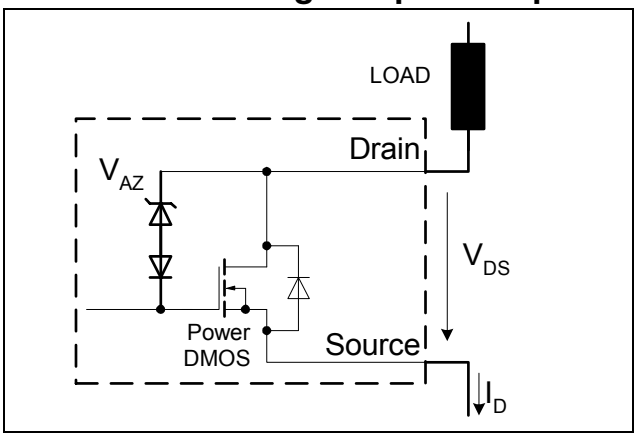
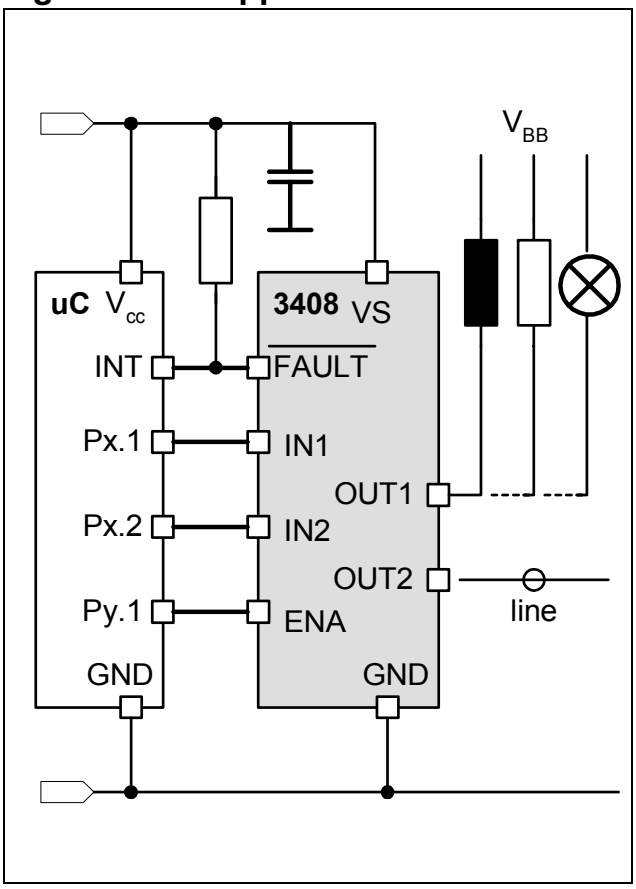


Figure 8 Application Circuit



Timing diagrams

Figure 9 Switching a resistive load

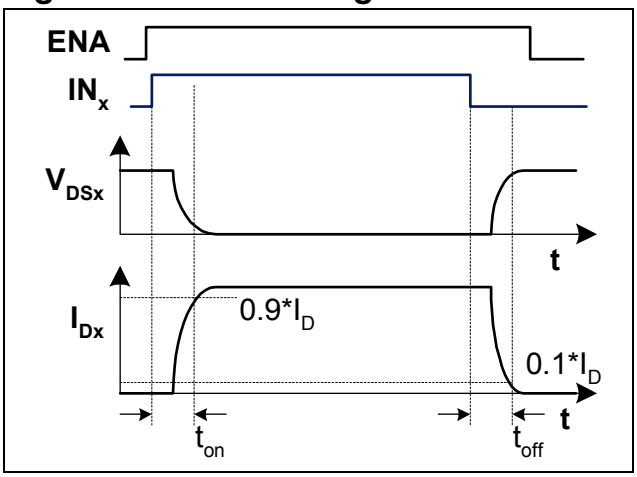


Figure 10 Switching an inductive load

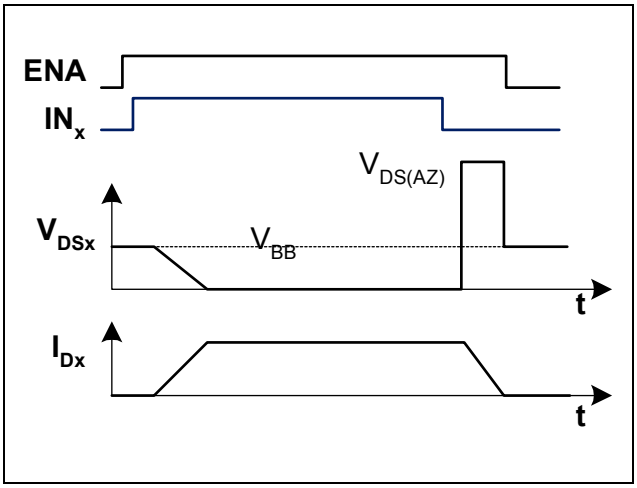
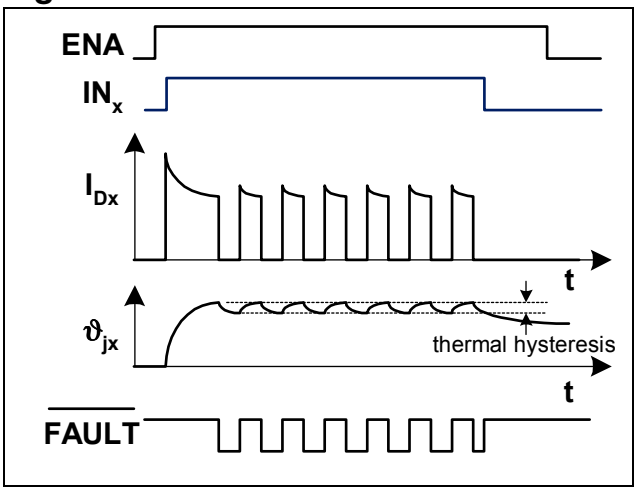
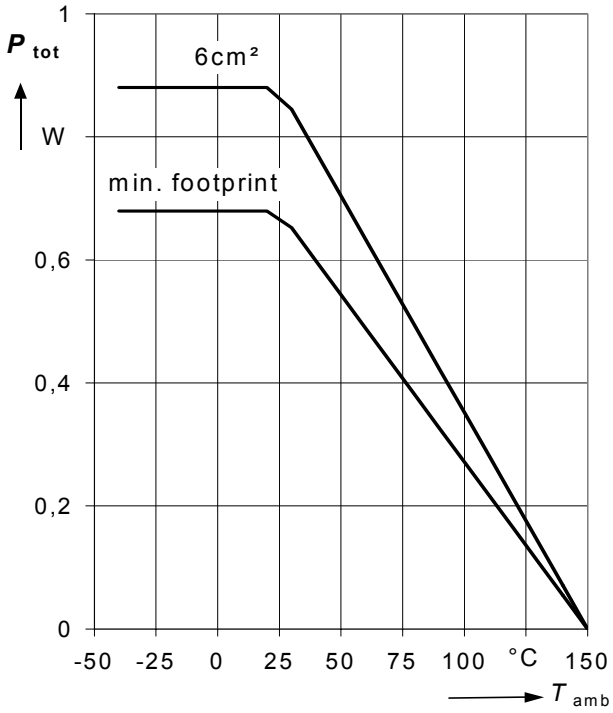


Figure 11 Short circuit

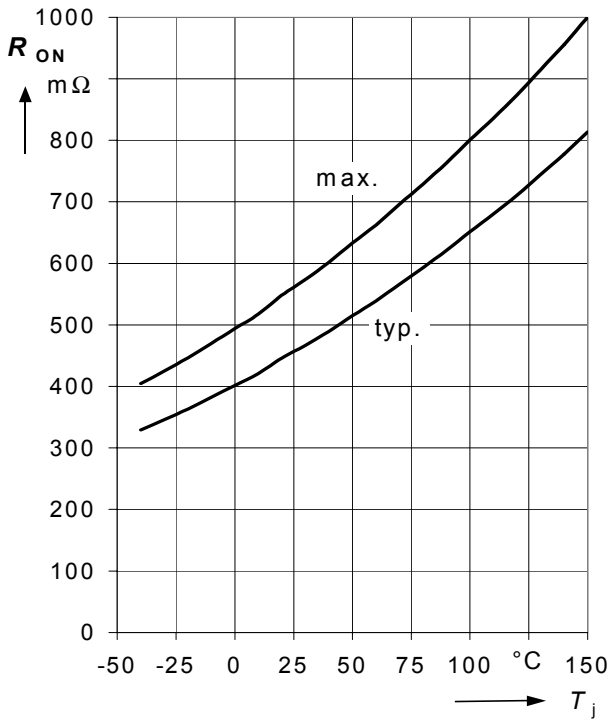


Characteristics

1. Max. allowable Power Dissipation
$P_{tot} = f(T_{amb})$

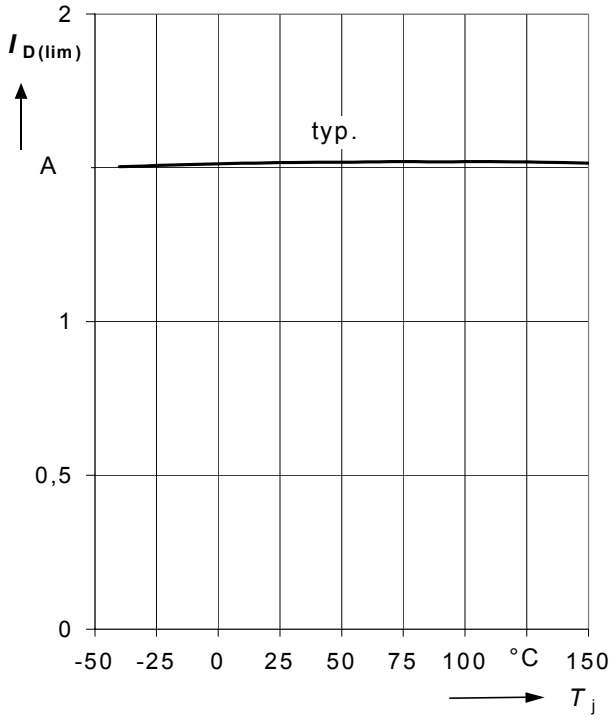


2. On-state Resistance $R_{ON} = f(T_j)$;
I_D = 0.2 A; V_S = 5 V



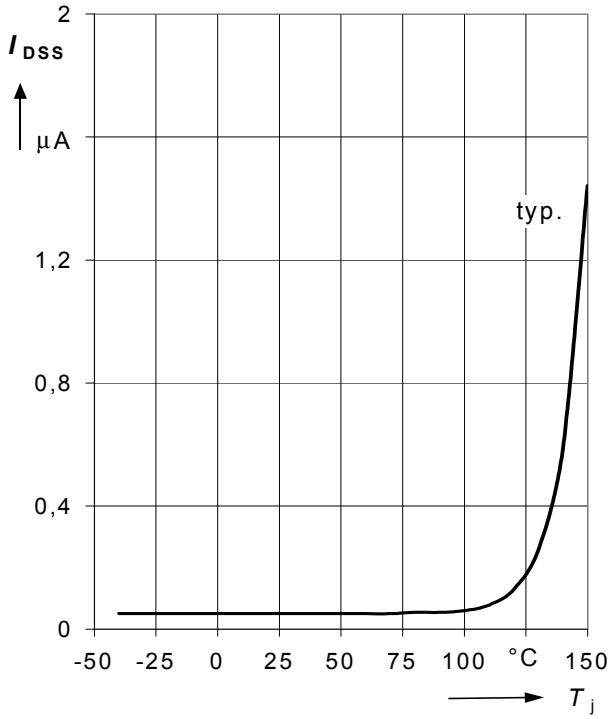
3. Typ. Short Circuit Current

$I_{D(lim)} = f(T_j)$



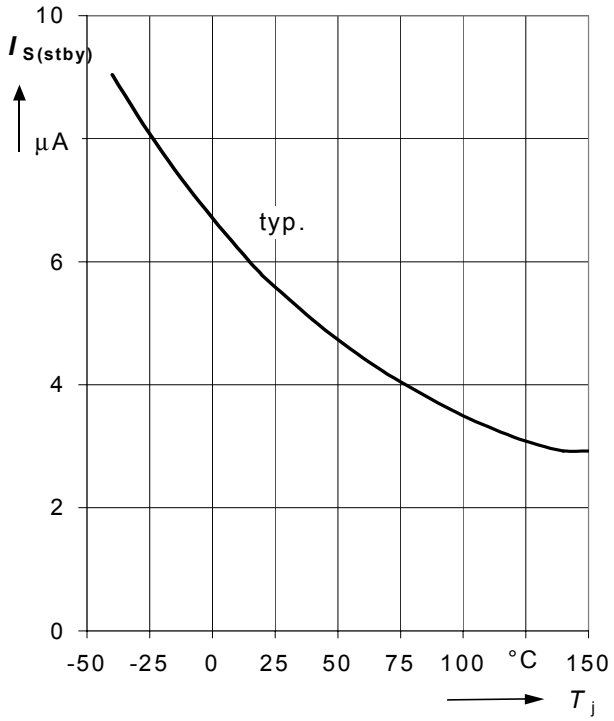
5. Typ. Output leakage current

$I_{DSS} = f(T_j); V_S$ = 18 V; V_{DS} = 60 V



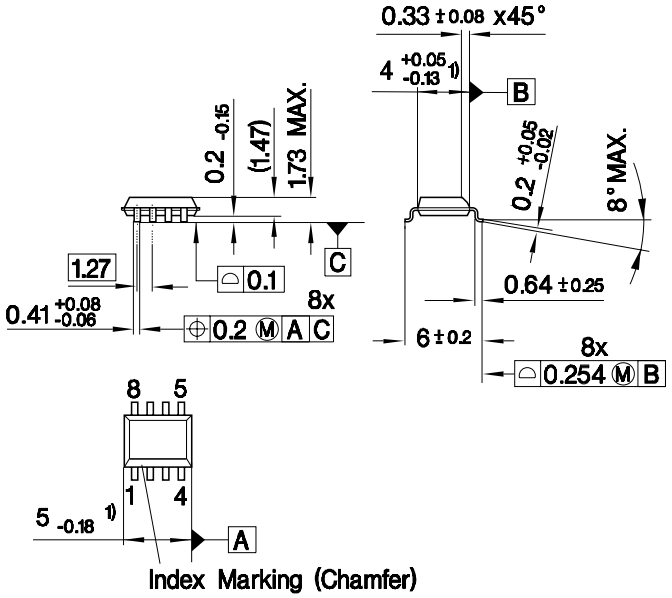
4. Typ. Supply current in Standby mode

$I_{S(stby)} = f(T_j); V_S$ = 5 V



Package Outlines

P-DSO-8-3
(Small Outline Transistor)



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPS05560

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm

Published by

Infineon Technologies AG,

Bereichs Kommunikation

St.-Martin-Strasse 76,

D-81541 München

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