

Description

The μ PD65000 (CMOS-2) series of gate arrays are low-power, high-speed devices featuring 3-micron silicon gate CMOS technology. The basic cell on the chip consists of four transistors, two P-channel and two N-channel, with double-layer metal interconnects. See figures 1 and 2.

Gate arrays are available in a variety of sizes (400 to 2,000 cells) and package types.

Gate arrays are intended for customers seeking cost effective alternatives. With gate arrays, customers can reduce component count and board size so that they can be more competitive in the markets they serve. NEC's gate array program allows a customized IC to be developed quickly and at a small fraction of the cost of a full custom development program.

NEC's comprehensive CAD support system and master slice system significantly reduce the time and expense usually associated with semicustom devices. Normal turnaround time, after logic validation, is only 8 to 12 weeks. Advanced CAD tools, such as logic simulation, automatic placement and routing, delay simulation, and test program generation ensure accurate error-free designs of all NEC gate arrays.

Features

- High speed: 3.0 ns/gate (with fan-out of 3 and 3-mm wiring)
- Low power: 30 μ W/gate/MHz
- Quick turnaround time: 8 - 12 weeks
- Simple interface to customer's circuit diagram and test pattern sheets
- Fully supported by advanced CAD
 - Logic simulation
 - Automatic placement and routing
 - Test program generation
 - Delay simulation
- Direct access to CAD simulation
 - Designers can use their own terminals through a local network to an NEC design center for logic simulation
- Four types of output buffers
 - Normal
 - Open-drain
 - Three-state
 - Bidirectional
- Wide choice of DIP, QIP, PGA, and flat packages to suit unique applications

Figure 1. CMOS Gate Array Chip Layout

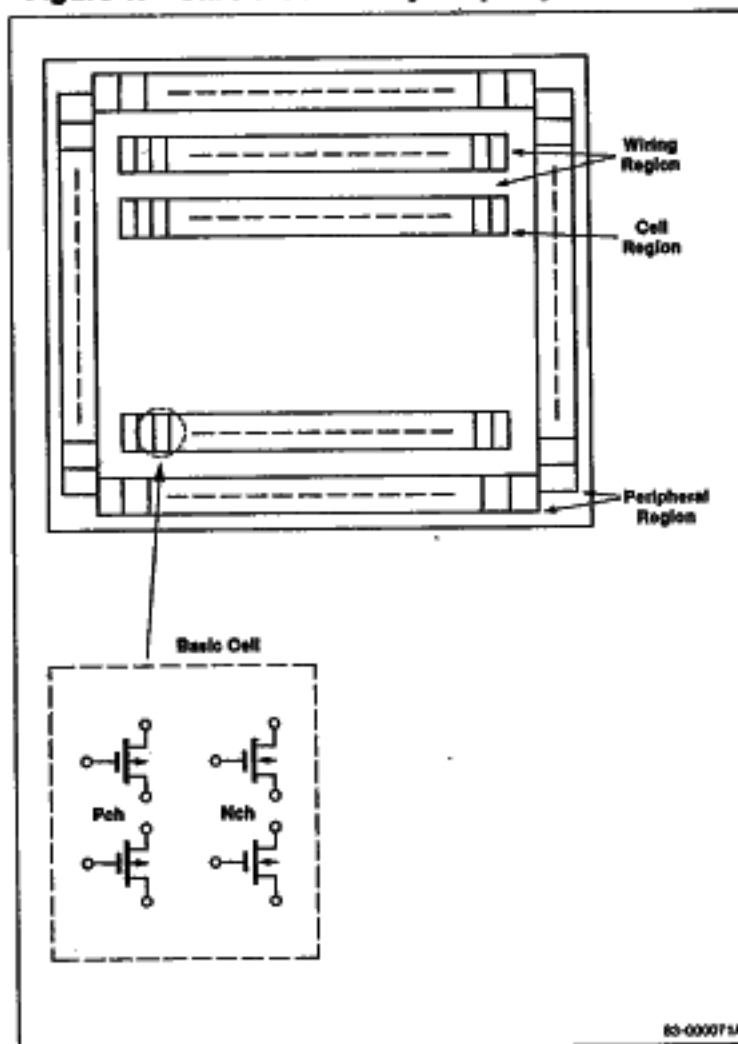
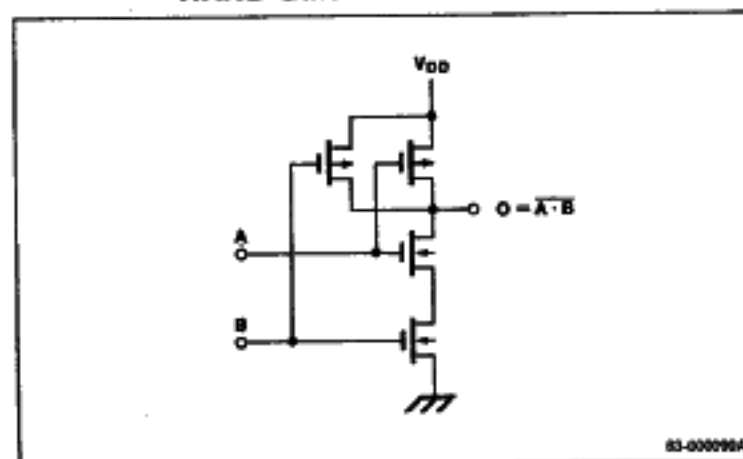


Figure 2. Cell Configured as a Two-Input NAND Gate



Absolute Maximum Ratings

$T_A = +25^\circ\text{C}$

| | |
|---------------------------------|----------------------------|
| Power supply voltage, V_{DD} | -0.5 to +7.0 V |
| Input voltage, V_I | -0.5 V to $V_{DD} + 0.5$ V |
| Output current, I_O | 10 mA |
| Operating temperature, T_{OP} | -40 to +85°C |
| Storage temperature, T_{STG} | -65 to +150°C |

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated outside the Recommended Operating Conditions below. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

$T_A = -40$ to $+85^\circ\text{C}$

| Parameter | Symbol | Limits | | | Unit | Test Conditions |
|--------------------------|------------|--------------|-----|--------------|------|------------------------|
| | | Min | Typ | Max | | |
| Power supply voltage | V_{DD} | 4.5 | 5 | 5.5 | V | |
| Input voltage | V_I | 0 | | V_{DD} | V | |
| Low-level input voltage | V_{IL} | 0 | | 0.3 V_{DD} | V | CMOS level |
| High-level input voltage | V_{IH} | 0.7 V_{DD} | | V_{DD} | V | CMOS level |
| Low-level input voltage | V_{IL} | 0 | | 0.8 | V | TTL level ¹ |
| High-level input voltage | V_{IH} | 2.0 | | V_{DD} | V | TTL level ¹ |
| Input rise, fall times | t_R, t_F | 0 | | 10 | μs | |

Note: 1. $T_A = 0$ to $+70^\circ\text{C}$, $V_{DD} = 5$ V $\pm 5\%$

Configuration Data

| | μPD65003 | μPD65002 | μPD65010 | μPD65020 |
|--------------------------|---------------------|----------------------|----------------------|----------------------|
| Number of cells | 427 | 858 | 1,368 | 2,112 |
| Configuration | 61 rows x 7 columns | 66 rows x 13 columns | 76 rows x 18 columns | 96 rows x 22 columns |
| Number of input buffers | 38 | 48 | 64 | 78 |
| Number of output buffers | 36 | 48 | 64 | 78 |

DC Characteristics

$T_A = -40$ to $+85^\circ\text{C}$; $V_{DD} = 5$ V $\pm 10\%$

| Parameter | Symbol | Limits | | | Unit | Test Conditions |
|---------------------------|----------|----------------|-----------|-----|------|---------------------------|
| | | Min | Typ | Max | | |
| Static current | I_L | | 0.1 | 200 | μA | $V_I = V_{DD}$ or GND |
| Dynamic current | I_{DD} | | 6 | | μA | 1 MHz |
| Input current | I_I | | 10^{-5} | 10 | μA | $V_I = V_{DD}$ or GND |
| Low-level output current | I_{OL} | 3.2 | 6 | | mA | $V_{OL} = 0.4$ V |
| High-level output current | I_{OH} | 1 | 2 | | mA | $V_{OH} = V_{DD} - 0.4$ V |
| Low-level output voltage | V_{OL} | | | 0.1 | V | $I_O = 0$ |
| High-level output voltage | V_{OH} | $V_{DD} - 0.1$ | | | V | $I_O = 0$ |

AC Characteristics

$T_A = -40$ to $+85^\circ\text{C}$; $V_{DD} = 5$ V $\pm 10\%$

| Parameter | Symbol | Limits | | | Unit | Test Conditions |
|-----------------------------|-----------|--------|-----|-----|------|------------------------------------|
| | | Min | Typ | Max | | |
| Maximum operating frequency | f_{MAX} | 10 | 25 | | MHz | |
| Delay time ¹ | t_{pD} | | 3 | | ns | Gate Output buffer ² |
| | t_{pD} | | 12 | | ns | |
| Output rise time | t_R | | 15 | | ns | $C_L = 15$ pF |
| Output fall time | t_F | | 8 | | ns | $C_L = 15$ pF |

Note: 1. With fan-out of 3 and 3 mm wiring.
2. With $C_L = 15$ pF

Figure 3. Example of a Circuit Diagram

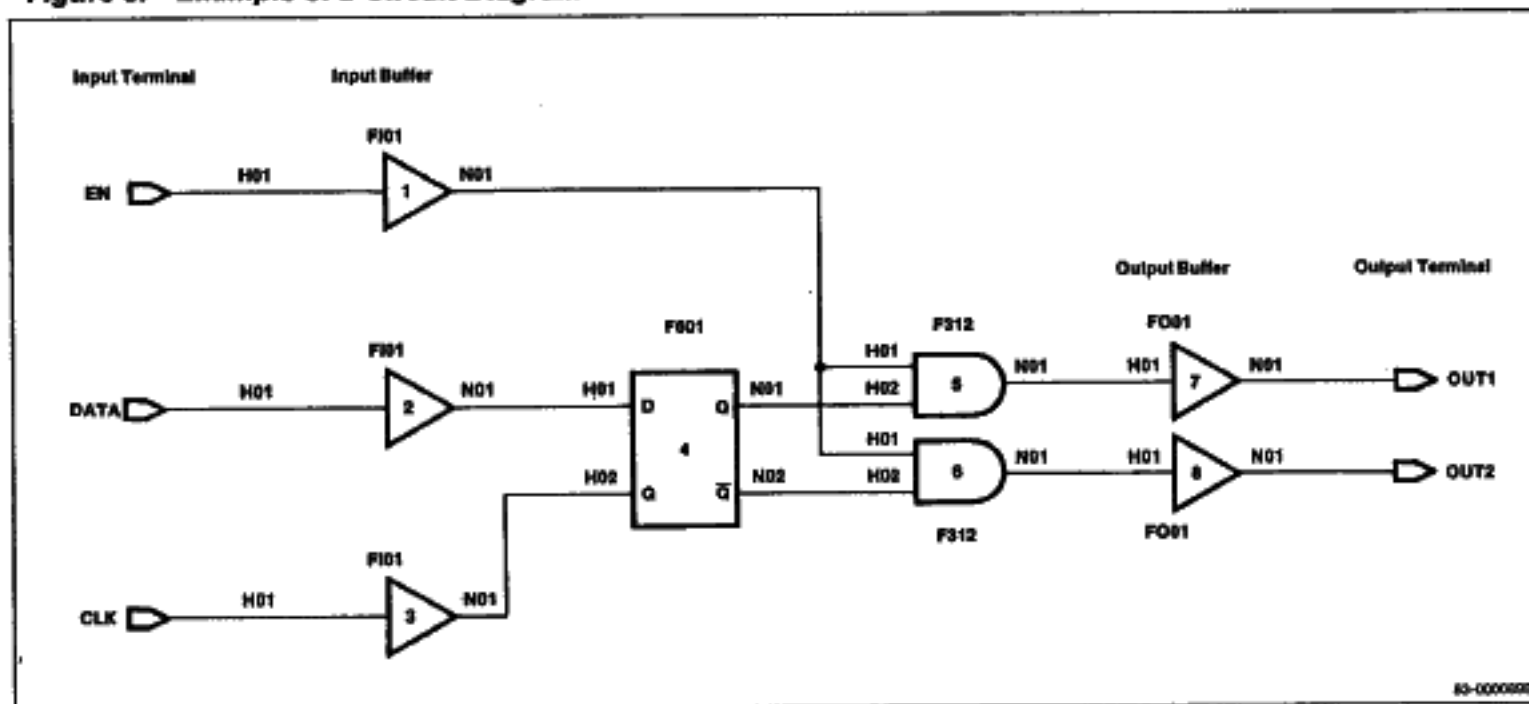
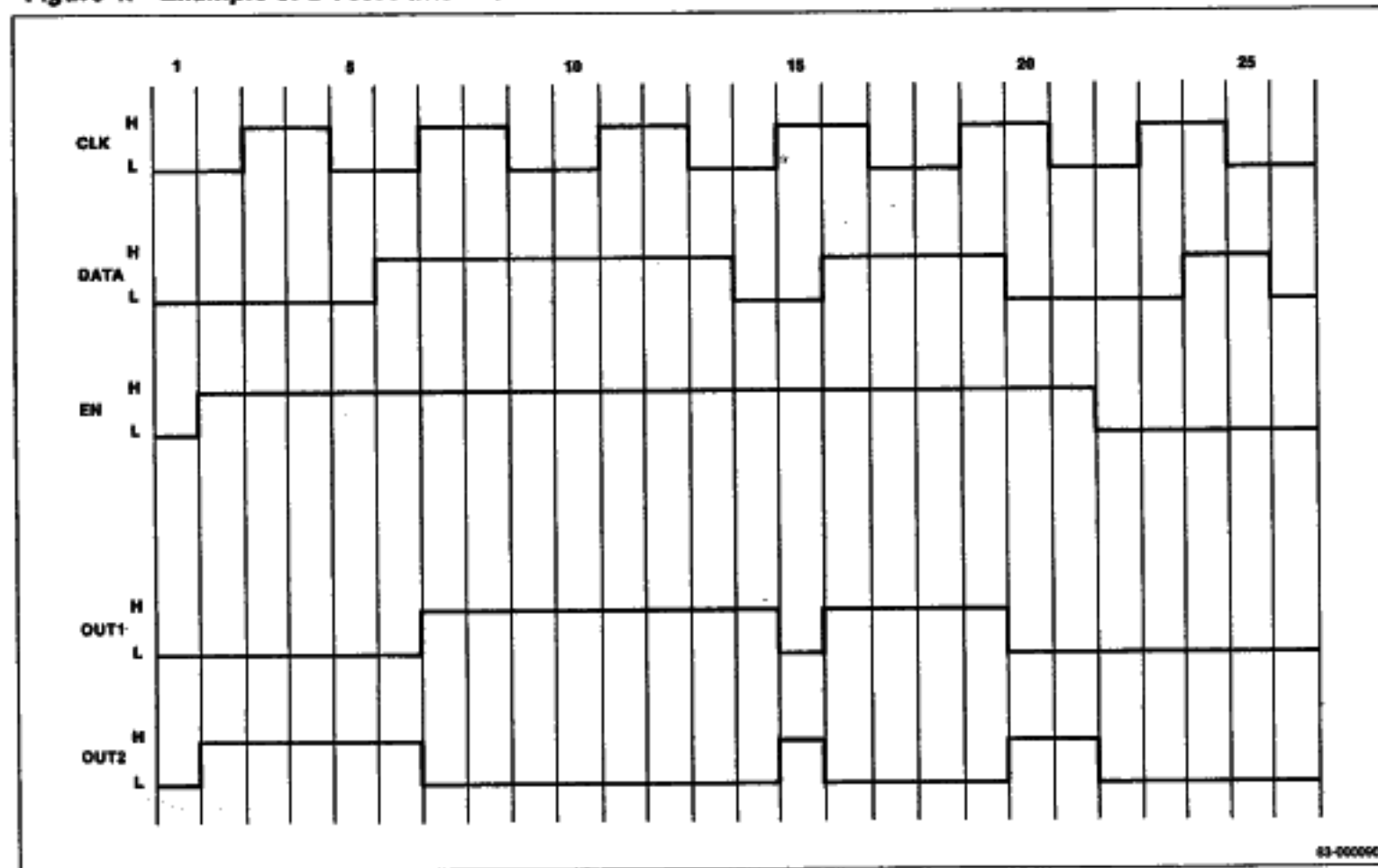


Figure 4. Example of a Test Pattern Chart



Gate Array Development Process

Figure 5 is a flowchart showing supporting data, development steps, and customer/NEC interface options.

Customer/NEC Interface Options

NEC's computer and communications environment allows gate array designers to select the interface most suitable to their needs.

Standard Data. For the simplest interface, the customer provides a circuit diagram and test patterns. The remainder of the development process is NEC's responsibility.

Macro Converted Data. The customer provides a circuit diagram based on the macros in the Block Library plus test pattern data.

File Generated Data. The customer provides a netlist and test pattern file in NEC compatible format. The netlist is a text file describing circuit interconnections. Data may be sent to NEC on magnetic tape or a floppy disk or transmitted via telephone. The formats and procedures for handling these files will be fully specified by the appropriate NEC Design Center.

Graphic PC Generated Data. Using the PC9800 workstation, a customer can easily generate the necessary netlist and test pattern file. The PC9800 workstation supports schematic capture and limited design rule checking.

Workstation Generated Data. For this interface, the customer performs logic simulation using either workstations by Valid Systems, Mentor Graphics, Daisy Systems and others, or the TEGAS-5™ software on a main frame computer. NEC does the final compatibility check. (Separate manuals describe the various workstation interfaces.)

PG Mask Tape Interface. A separate manual will be issued when this interface becomes available.

TEGAS-5 is the trademark of Calma Company.

Development Steps

Design Rule Checking. Once the circuit interconnect data is complete, the first step of the logic validation process is the design rule check. Parameters such as cell usage, power dissipation and fan-out loading are determined and checked.

Unit Simulation [Static Logic Simulation]. Here, any coding errors and data conversion errors are eliminated.

Delay Time Simulation. Before automatic placement and routing, delay time simulation gives an accurate estimate of the expected circuit delays.

Automatic Placement and Routing. NEC's advanced software allows up to 95-percent cell utilization without resorting to manual routing.

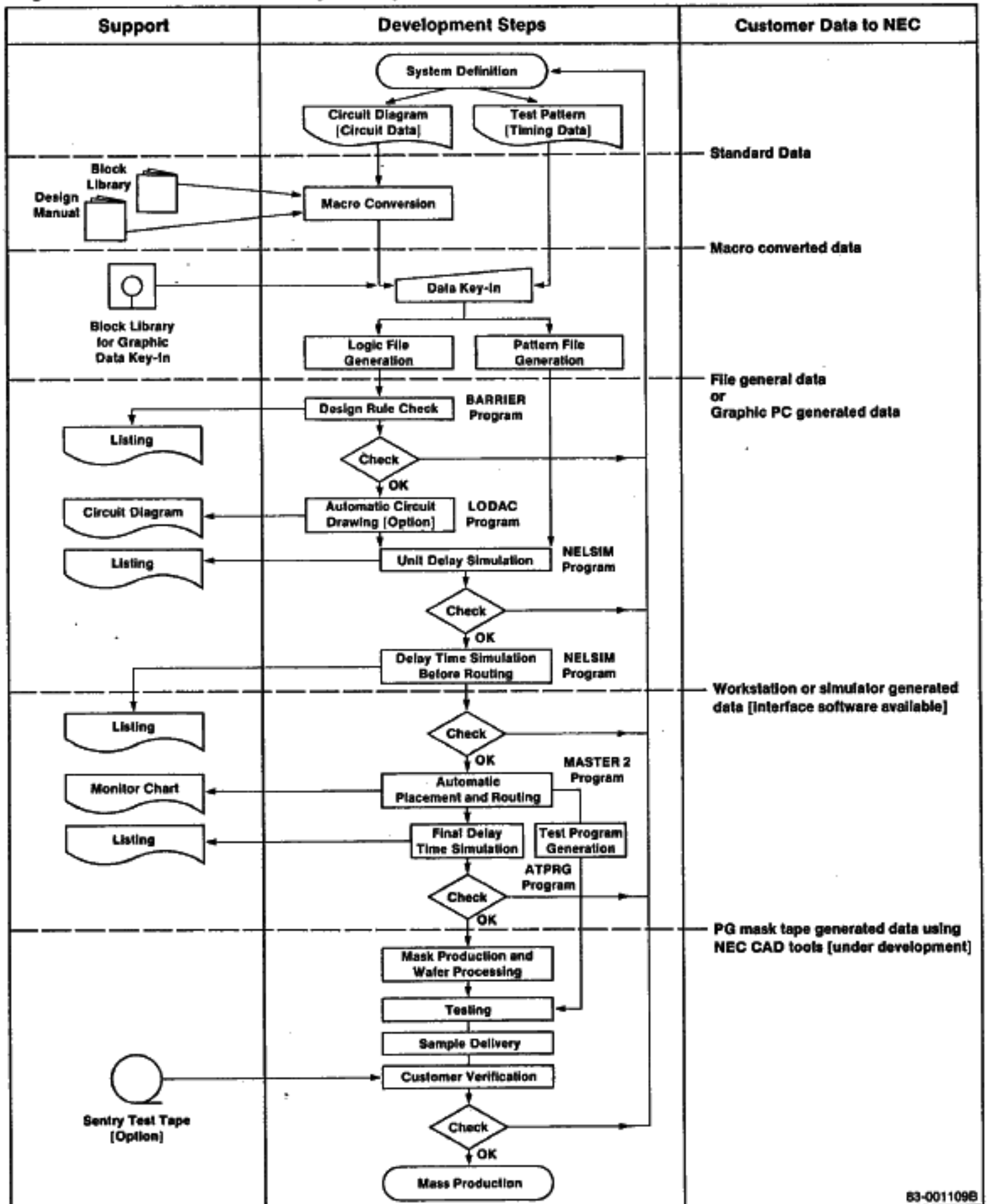
Final Delay Time Simulation. Here, wire lengths are taken into account. Results of this step provide the customer with an accurate circuit analysis.

Production. If the above steps are completed successfully, design enters actual production followed by 100-percent wafer testing.

Packaging. Successfully tested wafers are divided into individual chips, which are then die-bonded onto the customer-specified package. Chips are then wire-bonded and sealed. The dc parameters and logic functions of each chip are checked in the final test.

Prototype Evaluation. Ten engineering samples are delivered to the customer for the system function test. If customer evaluation is satisfactory, the development process is finished. NEC is ready to begin mass production.

Figure 5. Flowchart for Gate Array Development



μ PD65000 (CMOS-2) SERIES 3-MICRON

NEC

Development Procedure

The semicustom approach of gate arrays offers a unique and effective method of manufacturing ICs at reduced cost and development time. NEC makes this possible by stocking wafers that are completely fabricated except for the final step of interconnection. This provides a designer the freedom of interconnecting the uncommitted components to achieve a unique circuit configuration.

CMOS-2 Block Library List

Interface Blocks

| Block Type | Function |
|------------|--|
| FI01 | Input Buffer (CMOS Level) |
| FI02 | Input Buffer (TTL Level) |
| FI03, FI04 | Oscillator block |
| F001 | Output Buffer (Normal) |
| EXT1 | Output Buffer (Nch Open Drain) |
| EXT2 | Output Buffer (Pch Open Drain) |
| B003 | I/O Buffer (Three-State CMOS Level In) |
| B004 | I/O Buffer (Three-State TTL Level In) |
| B008 | Output Buffer (Three-State) |

Functional Blocks

| | Block Type | Function | Cells |
|-----------------|------------|----------------------|-------|
| Level Generator | F091 | H.L. Level Generator | 1 |
| Inverter | F101 | 1-Input (F.O. = 8) | 1 |
| | F102 | 1-Input (F.O. = 16) | 1 |
| | F103 | 1-Input (F.O. = 24) | 2 |
| | F104 | 1-Input (F.O. = 32) | 2 |
| Buffer | F111 | 1-Input (F.O. = 8) | 1 |
| | F112 | 1-Input (F.O. = 16) | 2 |
| | F113 | 1-Input (F.O. = 24) | 2 |
| | F114 | 1-Input (F.O. = 32) | 3 |
| NOR | F202 | 2-Input NOR Gate | 1 |
| | F203 | 3-Input NOR Gate | 2 |
| | F204 | 4-Input NOR Gate | 2 |
| | F208 | 8-Input NOR Gate | 7 |
| OR | F212 | 2-Input OR Gate | 2 |
| | F213 | 3-Input OR Gate | 2 |
| | F214 | 4-Input OR Gate | 3 |

Essential Documents

- Contract and nondisclosure agreement
- Circuit diagram based on the NEC Block Library
- Interconnection data file (LOGINC)
- Test pattern file (NELPAT)
- Pin assignment (if required)
- Critical path identification (if required)

Functional Blocks [cont]

| | Block Type | Function | Cells | |
|---------|------------|-------------------------------------|------------------|---|
| NAND | F302 | 2-Input NAND Gate | 1 | |
| | F303 | 3-Input NAND Gate | 2 | |
| | F304 | 4-Input NAND Gate | 2 | |
| | F305 | 5-Input NAND Gate | 3 | |
| | F306 | 6-Input NAND Gate | 3 | |
| | F308 | 8-Input NAND Gate | 7 | |
| | AND | F312 | 2-Input AND Gate | 2 |
| | | F313 | 3-Input AND Gate | 2 |
| F314 | | 4-Input AND Gate | 3 | |
| AND-NOR | F421 | 2-Wide, 1-2-Input AND-OR-Inverter | 2 | |
| | F422 | 3-Wide, 1-1-2-Input AND-OR-Inverter | 2 | |
| | F423 | 2-Wide, 1-3-Input AND-OR-Inverter | 2 | |
| | F424 | 2-Wide, 2-2-Input AND-OR-Inverter | 2 | |
| | F425 | 3-Wide, 2-2-2-Input AND-OR-Inverter | 3 | |
| | F426 | 2-Wide, 3-3-Input AND-OR-Inverter | 3 | |
| | F429 | 4-Wide, 2-2-2-Input AND-OR-Inverter | 4 | |
| | F442 | 2-Wide, 4-4-Input AND-OR-Inverter | 4 | |
| OR-NAND | F431 | 2-Wide, 1-2-Input OR-AND-Inverter | 2 | |
| | F432 | 2-Wide, 2-2-Input OR-AND-Inverter | 2 | |
| | F433 | 2-Wide, 1-3-Input OR-AND-Inverter | 2 | |
| | F434 | 2-Wide, 2-2-Input OR-AND-Inverter | 2 | |
| | F435 | 2-Wide, 2-3-Input OR-AND-Inverter | 3 | |
| | F436 | 2-Wide, 3-3-Input OR-AND-Inverter | 3 | |
| | F454 | 4-Wide, 2-2-2-Input OR-AND-Inverter | 4 | |
| | Driver | F501 | Clock Driver | 1 |
| F502 | | Clock Driver (Dual) | 2 | |
| F503 | | Clock Driver (With Buffer) | 2 | |
| F504 | | Clock Driver (Dual with Buffer) | 4 | |
| F505 | | 2-Wide, 1-2-Input NAND-AND-Inverter | 2 | |
| EX-OR | F511 | 2-Input Exclusive-OR Gate | 3 | |
| EX-NOR | F512 | 2-Input Exclusive-NOR Gate | 3 | |



**μPD65000 (CMOS-2) SERIES
3-MICRON**

Functional Blocks [cont]

| | Block Type | Function | Cells |
|--------------------|------------|--|--------|
| Full Adder | F521 | 1 Bit Full Adder | 7 |
| | F523 | 4-Bit Full Adder | 34 |
| Three-State Buffer | F531 | Three-State Buffer (EN) (F.O. = 8) | 3 |
| | F532 | Three-State Buffer ($\overline{\text{EN}}$) (F.O. = 8) | 3 |
| | F533 | Three-State Buffer (EN) (F.O. = 24) | 4 |
| Multiplexer | F569 | 8-1 Multiplexer | 17 |
| | F570 | 4-1 Multiplexer | 8 |
| | F571 | 2-1 Multiplexer | 4 |
| Parity Generator | F581 | 8 Bit Odd Parity Generator | 18 |
| | F582 | 8 Bit Even Parity Generator | 18 |
| Latch | F595 | R-S Latch | 4 |
| | F601 | D-Latch | 3 |
| | F602 | D-Latch (with $\overline{\text{Reset}}$) | 4 |
| | F603 | D-Latch (with $\overline{\text{Reset}}$) | 4 |
| | F604 | D-Latch $\overline{\text{C}}$ | 3 |
| | F605 | D-Latch $\overline{\text{C}}$ with $\overline{\text{Reset}}$ | 4 |
| | F901 | 4 Bit D-Latch | 10 |
| | F902 | 8 Bit D-Latch | 18 |
| | Flip-Flop | F611 | D-Type |
| F612 | | D-Type with $\overline{\text{Reset}}$ | 7 |
| F613 | | D-Type with $\overline{\text{Set}}$ | 7 |
| F614 | | D-Type with $\overline{\text{Set-Reset}}$ | 7 |
| F615 | | D-Type with $\overline{\text{Reset}}$ | 7 |
| F616 | | D-Type with $\overline{\text{Set}}$ | 7 |
| F617 | | D-Type with $\overline{\text{Set-Reset}}$ | 7 |
| F631 | | D-Type $\overline{\text{C}}$ | 5 |
| F635 | | D-Type $\overline{\text{C}}$ with $\overline{\text{Reset}}$ | 7 |
| F636 | | D-Type $\overline{\text{C}}$ with $\overline{\text{Set}}$ | 7 |
| F637 | | D-Type $\overline{\text{C}}$ with $\overline{\text{Set-Reset}}$ | 7 |
| F641 | | D-Type (Buffered Out) | 6 |
| F642 | | D-Type (Buffered Out) with $\overline{\text{Reset}}$ | 8 |
| F643 | | D-Type (Buffered Out) with $\overline{\text{Set}}$ | 8 |
| F644 | | D-Type (Buffered Out) with $\overline{\text{Set-Reset}}$ | 8 |
| F645 | | D-Type (Buffered Out) with $\overline{\text{Reset}}$ | 8 |
| F646 | | D-Type (Buffered Out) with $\overline{\text{Set}}$ | 8 |
| F647 | | D-Type (Buffered Out) with $\overline{\text{Set-Reset}}$ | 8 |
| F661 | | D-Type (Buffered Out) $\overline{\text{C}}$ | 6 |
| F665 | | D-Type (Buffered Out) $\overline{\text{C}}$ with $\overline{\text{Reset}}$ | 8 |
| F666 | | D-Type (Buffered Out) $\overline{\text{C}}$ with $\overline{\text{Set}}$ | 8 |
| F667 | | D-Type (Buffered Out) $\overline{\text{C}}$ with $\overline{\text{Set-Reset}}$ | 8 |
| F922 | | 4 Bit D-Type with $\overline{\text{Reset}}$ | 26 |

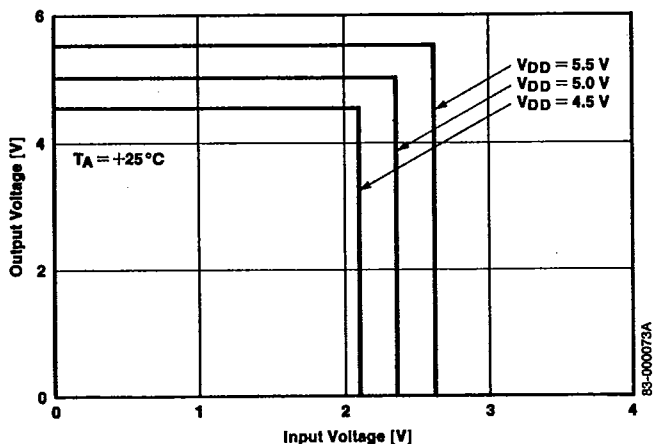
| | Block Type | Function | Cells |
|------------|--|--|-------|
| Flip-Flop | F691 | Serial/Parallel Shift Register | 5 |
| | F911 | 4 Bit Shift Register with $\overline{\text{Reset}}$ | 26 |
| | F912 | 4 Bit Serial/Parallel Shift Register | 24 |
| | F913 | 4 Bit Parallel Shift Register with $\overline{\text{Reset}}$ | 35 |
| | F712 | Toggle with $\overline{\text{Reset}}$ | 7 |
| | F713 | Toggle with $\overline{\text{Set}}$ | 7 |
| | F714 | Toggle with $\overline{\text{Set-Reset}}$ | 7 |
| | F715 | Toggle with $\overline{\text{Reset}}$ | 7 |
| | F716 | Toggle with $\overline{\text{Set}}$ | 7 |
| | F717 | Toggle with $\overline{\text{Set-Reset}}$ | 7 |
| | F735 | Toggle ($\overline{\text{T}}$) with $\overline{\text{Reset}}$ | 7 |
| | F736 | Toggle ($\overline{\text{T}}$) with $\overline{\text{Set}}$ | 7 |
| | F737 | Toggle ($\overline{\text{T}}$) with $\overline{\text{Set-Reset}}$ | 7 |
| | F742 | Toggle (Buffered Out) with $\overline{\text{Reset}}$ | 8 |
| | F743 | Toggle (Buffered Out) with $\overline{\text{Set}}$ | 8 |
| | F744 | Toggle (Buffered Out) with $\overline{\text{Set-Reset}}$ | 8 |
| | F745 | Toggle (Buffered Out) with $\overline{\text{Reset}}$ | 8 |
| | F746 | Toggle (Buffered Out) with $\overline{\text{Set}}$ | 8 |
| | F747 | Toggle (Buffered Out) with $\overline{\text{Set-Reset}}$ | 8 |
| | F765 | Toggle (Buffered Out) ($\overline{\text{T}}$) with $\overline{\text{Reset}}$ | 8 |
| | F766 | Toggle (Buffered Out) ($\overline{\text{T}}$) with $\overline{\text{Set}}$ | 8 |
| | F767 | Toggle (Buffered Out) ($\overline{\text{T}}$) with $\overline{\text{Set-Reset}}$ | 8 |
| | F791 | Toggle with $\overline{\text{Set-Reset}}$ and $\overline{\text{Tog-EN}}$ | 9 |
| F792 | Toggle ($\overline{\text{T}}$) with $\overline{\text{Set-Reset}}$ and $\overline{\text{Tog-EN}}$ | 9 | |
| F771 | JK F/F | 9 | |
| F772 | JK F/F with $\overline{\text{Reset}}$ | 11 | |
| F773 | JK F/F with $\overline{\text{Set}}$ | 11 | |
| F774 | JK F/F with $\overline{\text{Set-Reset}}$ | 11 | |
| F775 | JK F/F with $\overline{\text{Reset}}$ | 11 | |
| F776 | JK F/F with $\overline{\text{Set}}$ | 11 | |
| F777 | JK F/F with $\overline{\text{Set-Reset}}$ | 11 | |
| F781 | JK F/F $\overline{\text{C}}$ | 9 | |
| F785 | JK F/F $\overline{\text{C}}$ with $\overline{\text{Reset}}$ | 11 | |
| F786 | JK F/F $\overline{\text{C}}$ with $\overline{\text{Set}}$ | 11 | |
| F787 | JK F/F $\overline{\text{C}}$ with $\overline{\text{Set-Reset}}$ | 11 | |
| Counter | F961 | 4-Bit Sync Binary Counter with $\overline{\text{Reset}}$ | 54 |
| | F962 | 4-Bit Sync Binary Counter with $\overline{\text{Reset}}$ | 34 |
| Decoder | F981 | 2-to-4 Decoder with $\overline{\text{EN}}$ | 9 |
| | F982 | 3-to-8 Decoder with $\overline{\text{EN}}$ | 20 |
| Comparator | F985 | 4-Bit Magnitude Comparator | 46 |
| Misc | BUSA | Bus Array | |

**μPD65000 (CMOS-2) SERIES
3-MICRON**

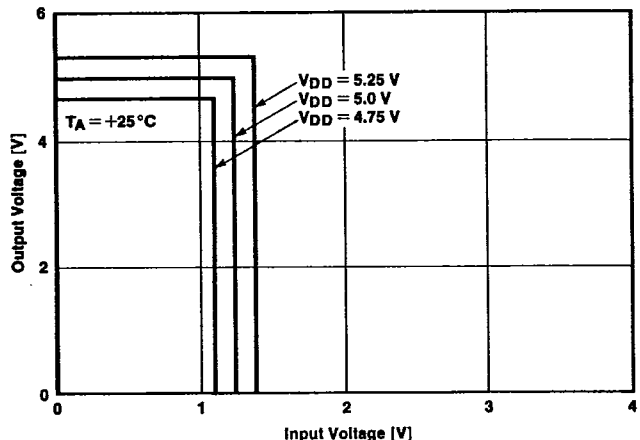


Operating Characteristics

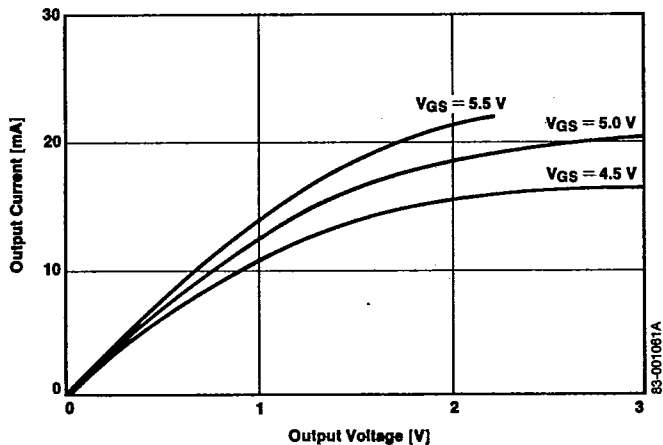
Output Voltage vs Input Voltage [CMOS Input]



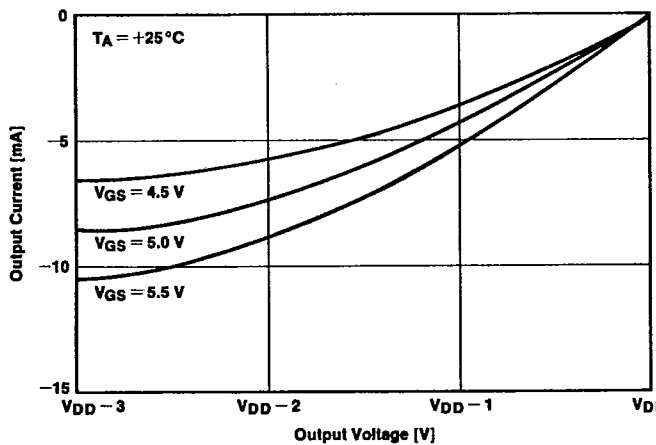
Output Voltage vs Input Voltage [TTL Input]



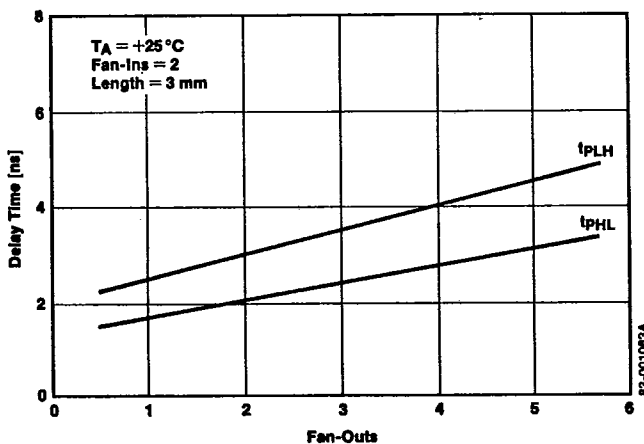
Output Current vs Output Voltage [N-Channel]



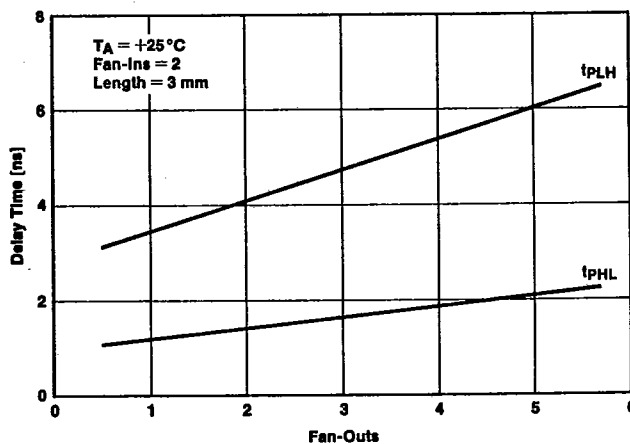
Output Current vs Output Voltage [P-Channel]



Delay Time vs Fan-Outs [NAND]

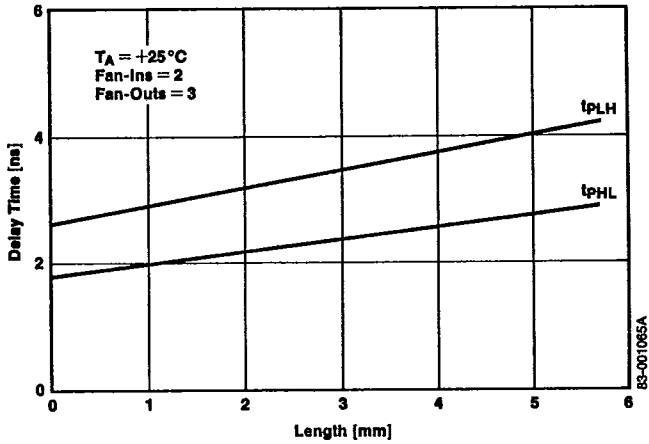


Delay Time vs Fan-Outs [NOR]

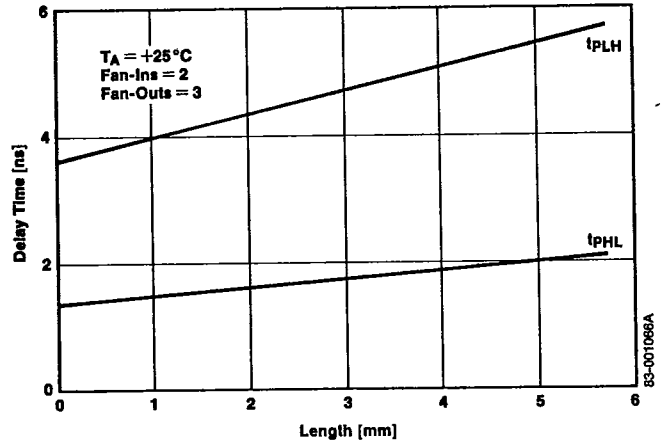


Operating Characteristics (cont)

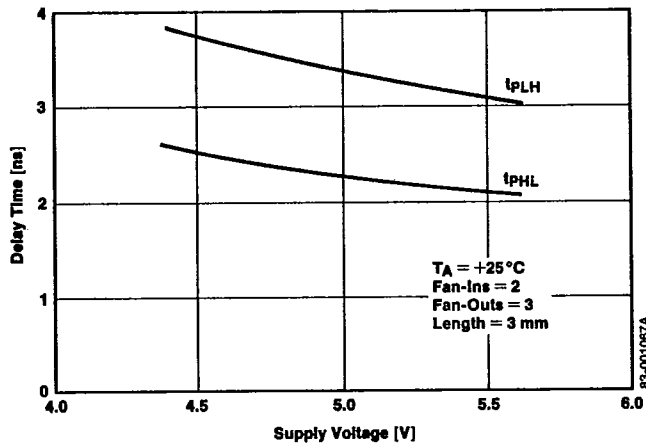
Delay Time vs Length [NAND]



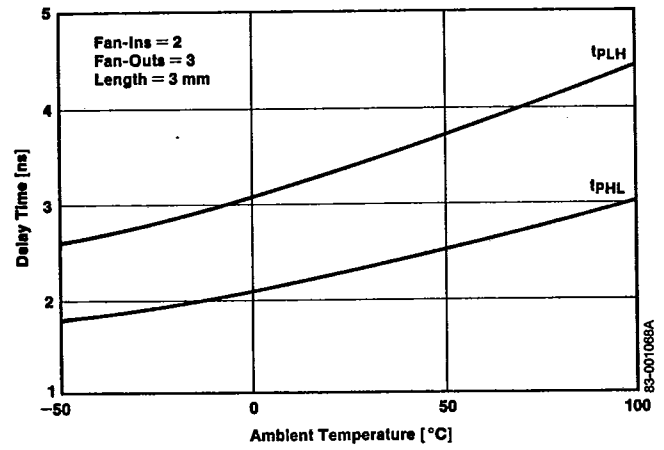
Delay Time vs Length [NOR]



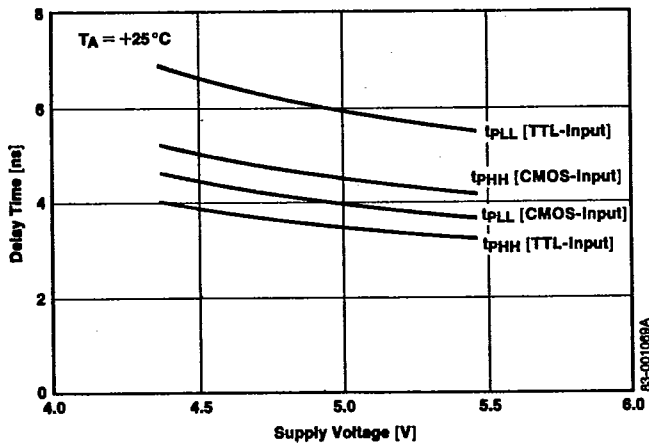
Delay Time vs Supply Voltage [NAND]



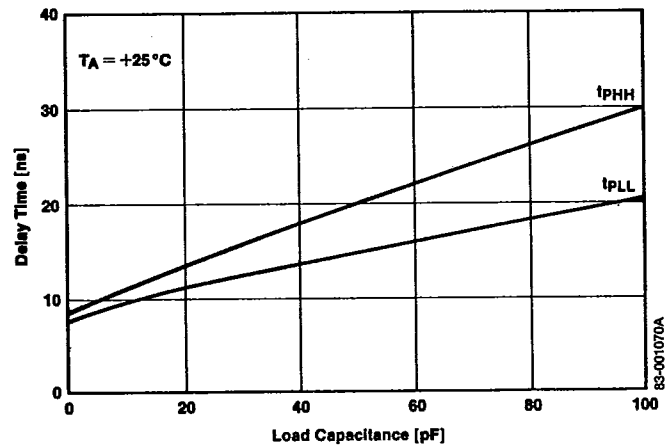
Delay Time vs Ambient Temperature [NAND]



Delay Time vs Supply Voltage [Input Buffer]



Delay Time vs Load Capacitance [Output Buffer]

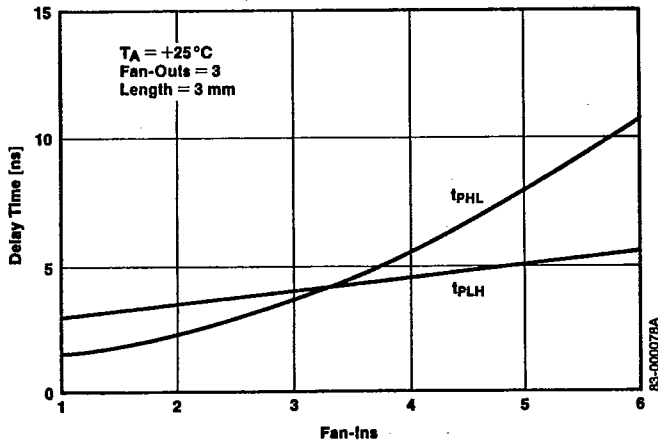


**μPD65000 (CMOS-2) SERIES
3-MICRON**

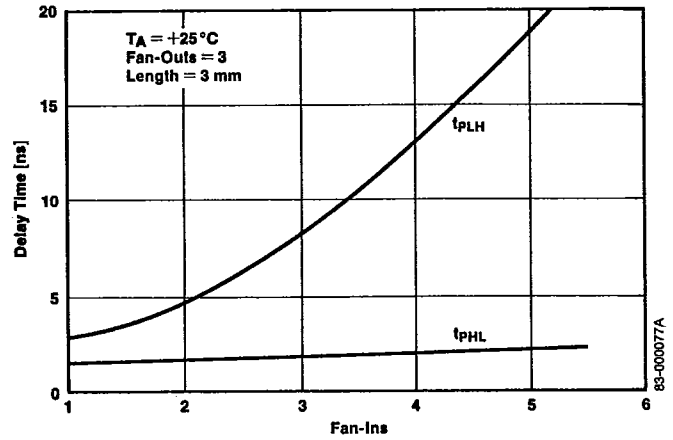


Operating Characteristics (cont)

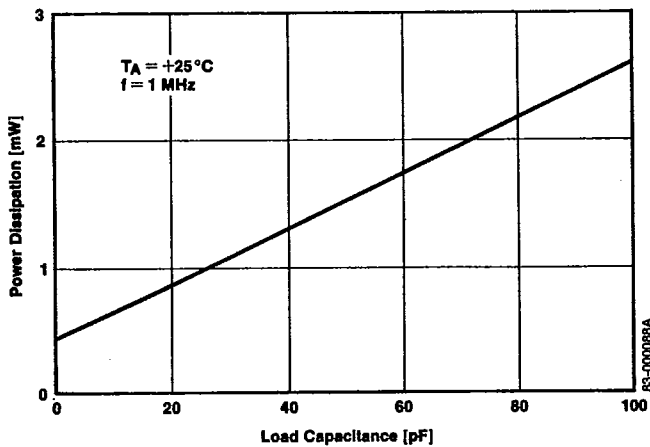
Delay Time vs Fan-Ins [NAND]



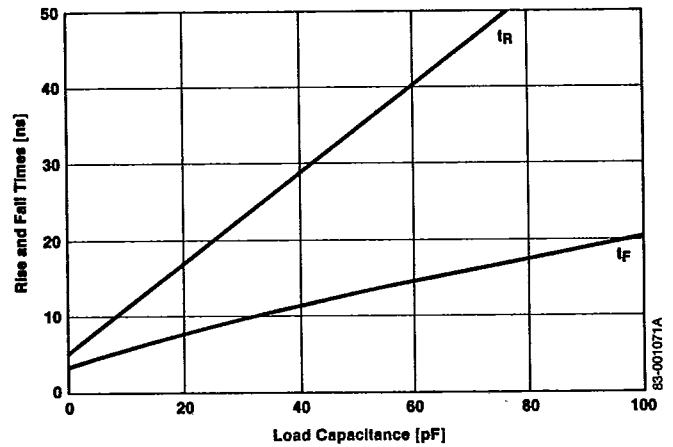
Delay Time vs Fan-Ins [NOR]



Power Dissipation vs Load Capacitance [Output Buffer]



Rise and Fall Times vs Load Capacitance [Output Buffer]





**μPD65000 (CMOS-2) SERIES
3-MICRON**

Packaging Information

The 3-micron gate arrays are available in a wide variety of packages to accommodate unique applications. The following table shows the package types in the μPD65000 (CMOS-2) series. (DIP = Dual in-line package; QIP = Quad in-line package; PGA = Pin grid array.)

Package Availability

| Package Type | μPD65003 | μPD65002 | μPD65010 | μPD65020 |
|-----------------|----------|----------|----------|----------|
| DIP | | | | |
| 16-Pin | • | | | |
| 18-Pin | • | | | |
| 20-Pin | • | | | |
| 24-Pin | • | • | • | |
| 28-Pin | • | • | • | • |
| 40-Pin | • | • | • | • |
| 48-Pin | | • | • | • |
| 64-Pin (shrink) | | | • | • |
| QIP | | | | |
| 64-Pin | | | • | • |
| Flat | | | | |
| 44-Pin | • | • | • | • |
| 52-Pin | | • | • | • |
| 64-Pin | | | • | • |
| 80-Pin | | | • | • |
| 100-Pin | | | | • |
| PGA | | | | |
| 72-Pin | | | | • |

Package Marking

Example of Plastic Package

