

# CD4070B, CD4077B

## CMOS Quad Exclusive-OR and Exclusive-NOR Gate

### Features

- High-Voltage Types (20V Rating)
- CD4070B - Quad Exclusive-OR Gate
- CD4077B - Quad Exclusive-NOR Gate
- Medium Speed Operation
  - $t_{PHL}, t_{PLH} = 65\text{ns}$  (Typ) at  $V_{DD} = 10\text{V}$ ,  $C_L = 50\text{pF}$
- 100% Tested for Quiescent Current at 20V
- Standardized Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of  $1\mu\text{A}$  at 18V Over Full Package Temperature Range
  - $100\text{nA}$  at 18V and  $25^\circ\text{C}$
- Noise Margin (Over Full Package Temperature Range)
  - 1V at  $V_{DD} = 5\text{V}$ , 2V at  $V_{DD} = 10\text{V}$ , 2.5V at  $V_{DD} = 15\text{V}$
- Meets All Requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications

- Logical Comparators
- Adders/Subtractors
- Parity Generators and Checkers

### Description

The Harris CD4070B contains four independent Exclusive-OR gates. The Harris CD4077B contains four independent Exclusive-NOR gates.

The CD4070B and CD4077B provide the system designer with a means for direct implementation of the Exclusive-OR and Exclusive-NOR functions, respectively.

### Ordering Information

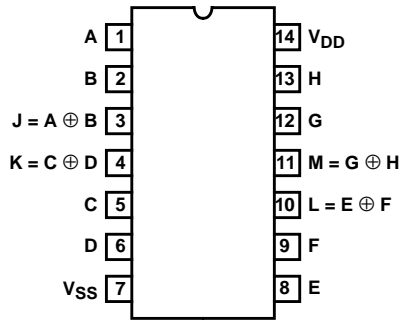
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD4070BE	-55 to 125	14 Ld PDIP
CD4070BF3A	-55 to 125	14 Ld CERDIP
CD4070BM	-55 to 125	14 Ld SOIC
CD4070BMT	-55 to 125	14 Ld SOIC
CD4070BM96	-55 to 125	14 Ld SOIC
CD4070BNSR	-55 to 125	14 Ld SOP
CD4070BPW	-55 to 125	14 Ld TSSOP
CD4070BPWR	-55 to 125	14 Ld TSSOP
CD4077BE	-55 to 125	14 Ld PDIP
CD4077BF3A	-55 to 125	14 Ld CERDIP
CD4077BM	-55 to 125	14 Ld SOIC
CD4077BMT	-55 to 125	14 Ld SOIC
CD4077BM96	-55 to 125	14 Ld SOIC
CD4077BNSR	-55 to 125	14 Ld SOP
CD4077BPW	-55 to 125	14 Ld TSSOP
CD4077BPWR	-55 to 125	14 Ld TSSOP

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

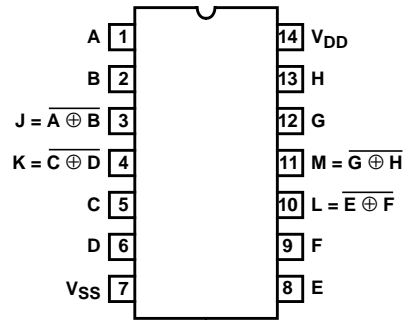
# CD4070B, CD4077B

## Pinouts

**CD4070B**  
(PDIP, Cerdip, SOIC, SOP, TSSOP)  
TOP VIEW

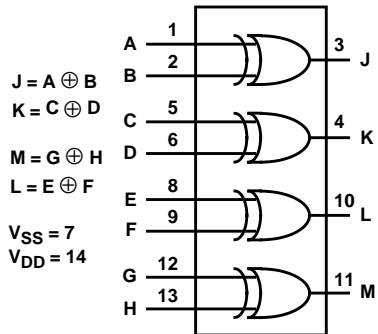


**CD4077B**  
(PDIP, Cerdip, SOIC, SOP, TSSOP)  
TOP VIEW

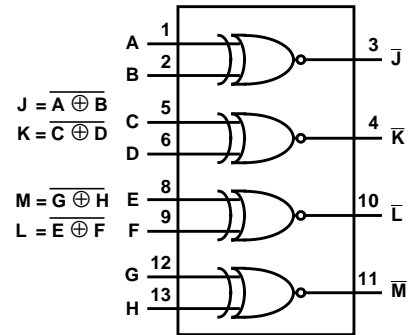


## Functional Diagrams

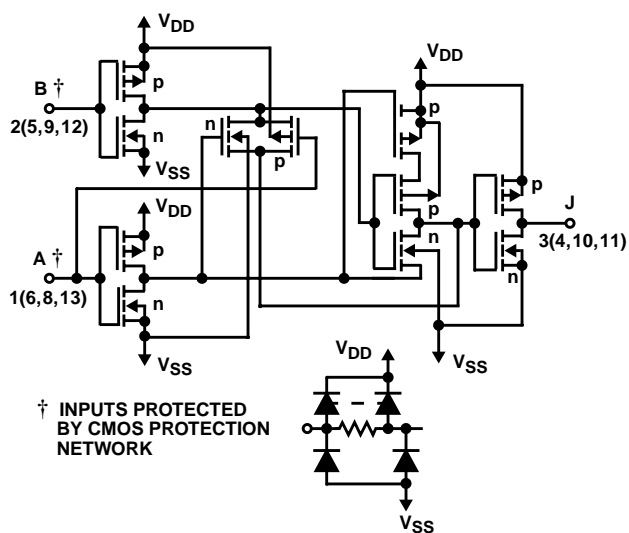
**CD4070B**



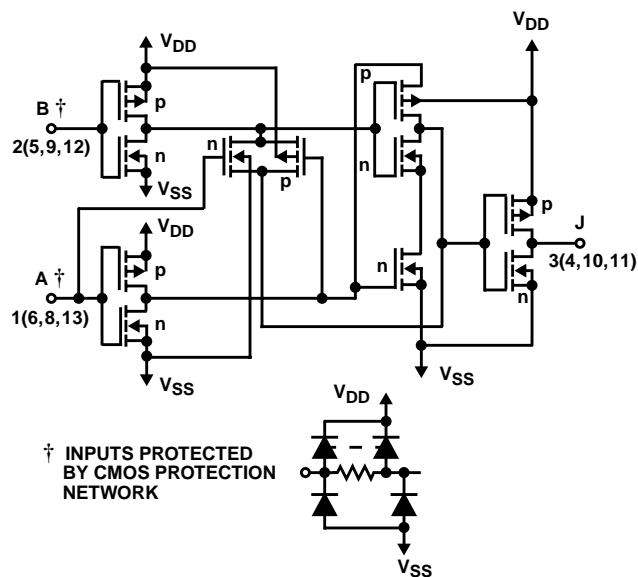
**CD4077B**



## CD4070B, CD4077B



**FIGURE 1. SCHEMATIC DIAGRAM FOR CD4070B  
(1 OF 4 IDENTICAL GATES)**



**FIGURE 2. SCHEMATIC DIAGRAM FOR CD4077B  
(1 OF 4 IDENTICAL GATES)**

**CD4070B TRUTH TABLE (1 OF 4 GATES)**

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

NOTE:  
 1 = High Level  
 0 = Low Level  
 J = A ⊕ B

**CD4077B TRUTH TABLE (1 OF 4 GATES)**

A	B	J
0	0	1
1	0	0
0	1	0
1	1	1

NOTE:  
 1 = High Level  
 0 = Low Level  
 J = A ⊕ B

## CD4070B, CD4077B

### Absolute Maximum Ratings

DC Supply Voltage Range ( $V_{DD}$ ) ..... -0.5V to 20V  
 Input Voltage Range, All Inputs ..... -0.5V to  $V_{DD}$  0.5V  
 DC Input Current .....  $\pm 10\text{mA}$

### Operating Conditions

Temperature Range ( $T_A$ ) ..... -55°C to 125°C  
 Supply Voltage Range (Typical) ..... 3V to 18V

### Thermal Information

Package Thermal Impedance,  $\theta_{JA}$  (see Note 1):  
 E (PDIP) Package ..... 80°C/W  
 M (SOIC) Package ..... 86°C/W  
 NS (SOP) Package ..... 76°C/W  
 PW (TSSOP) Package ..... 113°C/W  
 Maximum Junction Temperature (Hermetic Package or Die) . 175°C  
 Maximum Junction Temperature (Plastic Package) ..... 150°C  
 Maximum Storage Temperature Range ..... -65°C to 150°C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

#### NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

### DC Electrical Specifications

PARAMETER	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
				-55	-40	85	125	25			
	$V_O$ (V)	$V_{IN}$ (V)	$V_{DD}$ (V)					MIN	TYP	MAX	
Quiescent Device Current $I_{DD}$ Max	-	0, 5	5	0.25	0.25	7.5	7.5	-	0.01	0.25	$\mu\text{A}$
	-	0, 10	10	0.5	0.5	15	15	-	0.01	0.5	$\mu\text{A}$
	-	0, 15	15	1	1	30	30	-	0.01	1	$\mu\text{A}$
	-	0, 20	20	5	5	150	150	-	0.02	5	$\mu\text{A}$
Output Low (Sink) Current $I_{OL}$ Min	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	mA
	1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8	-	mA
Output High (Source) Current $I_{OH}$ Min	4.6	0, 5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0, 5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	mA
	9.5	0, 10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	mA
	13.5	0, 15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	mA
Output Voltage: Low Level, $V_{OL}$ Max	-	0, 5	5	0.05	0.05	0.05	0.05	-	0	0.05	V
	-	0, 10	10	0.05	0.05	0.05	0.05	-	0	0.05	V
	-	0, 15	15	0.05	0.05	0.05	0.05	-	0	0.05	V
Output Voltage: High Level, $V_{OH}$ Min	-	0, 5	5	4.95	4.95	4.95	4.95	4.95	5	-	V
	-	0, 10	10	9.95	9.95	9.95	9.95	9.95	10	-	V
	-	0, 15	15	14.95	14.95	14.95	14.95	14.95	15	-	V
Input Low Voltage, $V_{IL}$ Max	0.5, 4.5	-	5	1.5	1.5	1.5	1.5	-	-	1.5	V
	1, 9	-	10	3	3	3	3	-	-	3	V
	1.5, 13.5	-	15	4	4	4	4	-	-	4	V
Input High Voltage, $V_{IH}$ Min	0.5, 4.5	-	5	3.5	3.5	3.5	3.5	3.5	-	-	V
	1, 9	-	10	7	7	7	7	7	-	-	V
	1.5, 13.5	-	15	11	11	11	11	11	-	-	V
Input Current, $I_{IN}$ Max	-	0, 18	18	$\pm 0.1$	$\pm 0.1$	$\pm 1$	$\pm 1$	-	$\pm 10^{-5}$	$\pm 0.1$	$\mu\text{A}$

# CD4070B, CD4077B

## AC Electrical Specifications

$T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 200\text{k}\Omega$

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS ON ALL TYPES		UNITS
		$V_{DD}$ (V)	TYP	MAX	
Propagation Delay Time	$t_{PHL}, t_{PLH}$	5	140	280	ns
		10	65	130	ns
		15	50	100	ns
Transition Time	$t_{THL}, t_{TLH}$	5	100	200	ns
		10	50	100	ns
		15	40	80	ns
Input Capacitance	$C_{IN}$	Any Input	5	7.5	pF

## Typical Performance Curves



FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS



FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS



FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

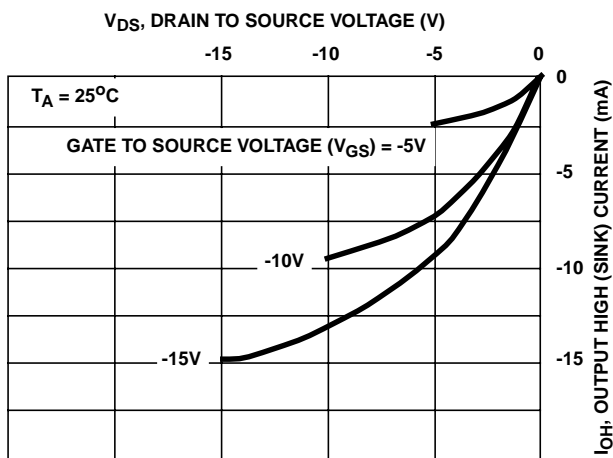


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

**Typical Performance Curves** (Continued)

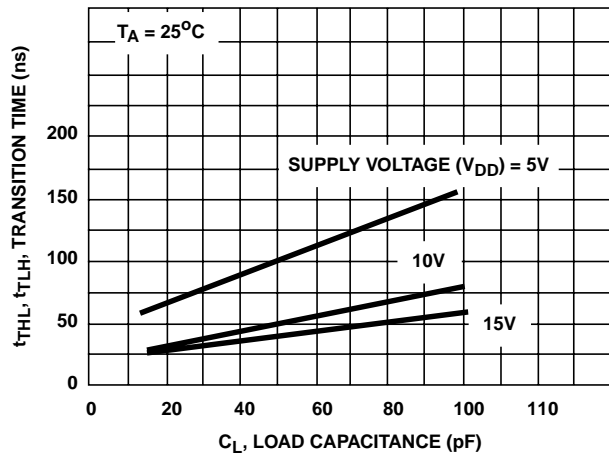


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

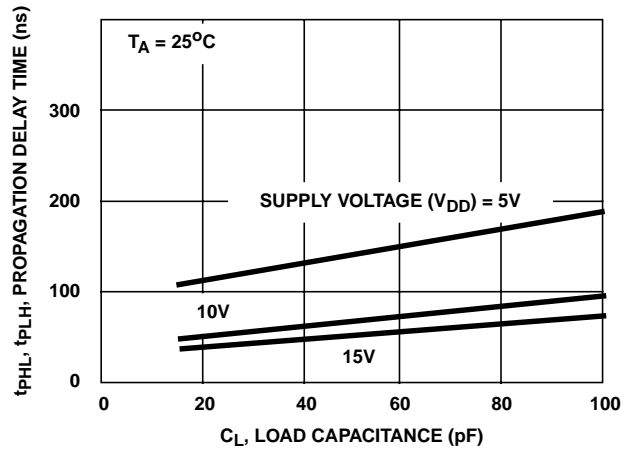


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

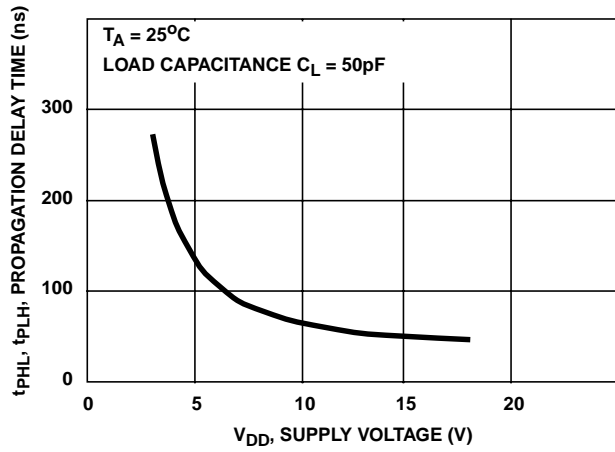


FIGURE 9. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF SUPPLY VOLTAGE

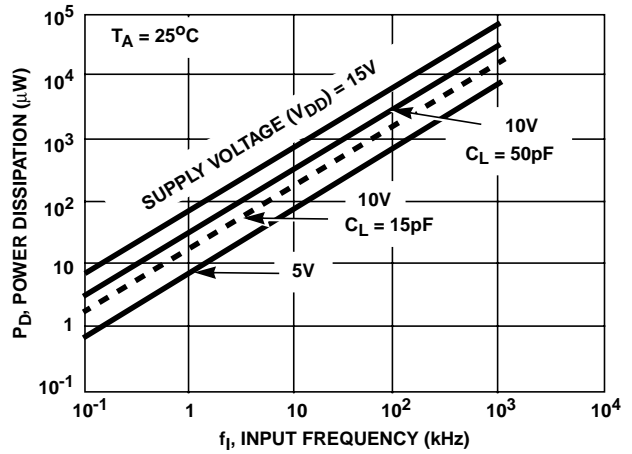


FIGURE 10. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



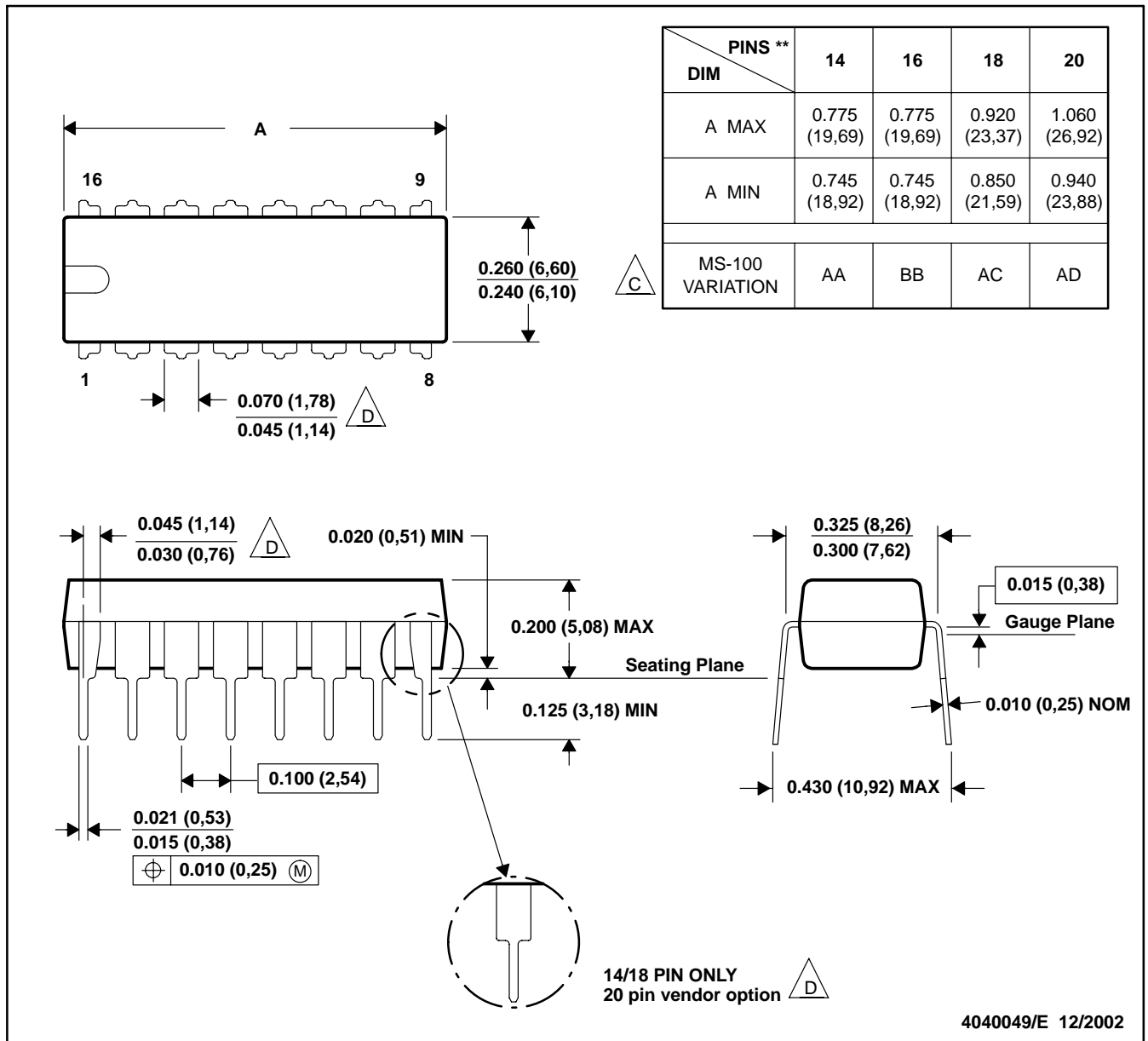
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 D The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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