

# MC14046B

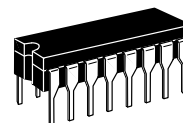
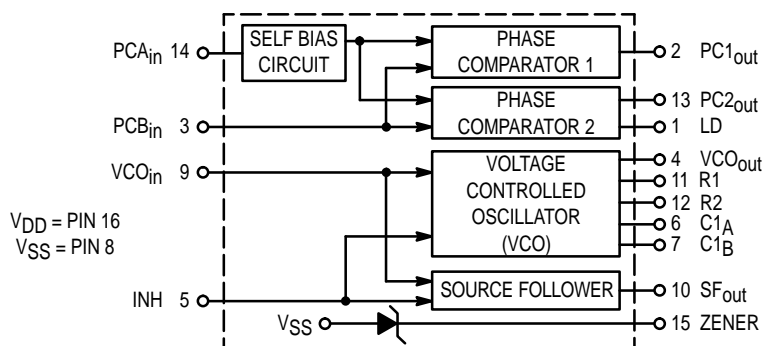
## Phase Locked Loop

The MC14046B phase locked loop contains two phase comparators, a voltage-controlled oscillator (VCO), source follower, and zener diode. The comparators have two common signal inputs,  $PCA_{in}$  and  $PCB_{in}$ . Input  $PCA_{in}$  can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal  $PC1_{out}$ , and maintains  $90^\circ$  phase shift at the center frequency between  $PCA_{in}$  and  $PCB_{in}$  signals (both at 50% duty cycle). Phase comparator 2 (with leading edge sensing logic) provides digital error signals,  $PC2_{out}$  and LD, and maintains a  $0^\circ$  phase shift between  $PCA_{in}$  and  $PCB_{in}$  signals (duty cycle is immaterial). The linear VCO produces an output signal  $VCO_{out}$  whose frequency is determined by the voltage of input  $VCO_{in}$  and the capacitor and resistors connected to pins  $C1_A$ ,  $C1_B$ , R1, and R2. The source-follower output  $SF_{out}$  with an external resistor is used where the  $VCO_{in}$  signal is needed but no loading can be tolerated. The inhibit input  $Inh$ , when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation.

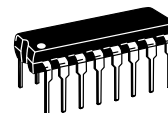
Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

- Buffered Outputs Compatible with MHTL and Low-Power TTL
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 to 18 V
- Pin-for-Pin Replacement for CD4046B
- Phase Comparator 1 is an Exclusive Or Gate and is Duty Cycle Limited
- Phase Comparator 2 switches on Rising Edges and is not Duty Cycle Limited

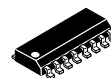
### BLOCK DIAGRAM



**L SUFFIX**  
CERAMIC  
CASE 620



**P SUFFIX**  
PLASTIC  
CASE 648



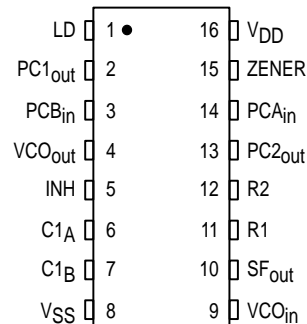
**DW SUFFIX**  
SOIC  
CASE 751G

### ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBDW	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.

### PIN ASSIGNMENT



**MAXIMUM RATINGS\*** (Voltages Referenced to V<sub>SS</sub>)

Rating	Symbol	Value	Unit
DC Supply Voltage	V <sub>DD</sub>	- 0.5 to + 18	Vdc
Input Voltage, All Inputs	V <sub>in</sub>	- 0.5 to V <sub>DD</sub> + 0.5	Vdc
DC Input Current, per Pin	I <sub>in</sub>	± 10	mAdc
Power Dissipation, per Package†	P <sub>D</sub>	500	mW
Operating Temperature Range	T <sub>A</sub>	- 55 to + 125	°C
Storage Temperature Range	T <sub>stg</sub>	- 65 to + 150	°C

\* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level V <sub>in</sub> = V <sub>DD</sub> or 0  "1" Level V <sub>in</sub> = 0 or V <sub>DD</sub>	V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage # (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  "1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  Sink (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	I <sub>OH</sub>	5.0	- 1.2	—	- 1.0	- 1.7	—	- 0.7	—	mAdc
		5.0	- 0.25	—	- 0.2	- 0.36	—	- 0.14	—	
		10	- 0.62	—	- 0.5	- 0.9	—	- 0.35	—	
	I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc
Input Capacitance	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) I <sub>nh</sub> = PCA <sub>in</sub> = V <sub>DD</sub> , Zener = VCO <sub>in</sub> = 0 V, PCB <sub>in</sub> = V <sub>DD</sub> or 0 V, I <sub>out</sub> = 0 μA	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current† (I <sub>nh</sub> = "0", f <sub>0</sub> = 10 kHz, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 1.0 MΩ, R <sub>2</sub> = ∞, R <sub>SF</sub> = ∞, and 50% Duty Cycle)	I <sub>T</sub>	5.0	I <sub>T</sub> = (1.46 μA/kHz) f + I <sub>DD</sub>							mAdc
		10	I <sub>T</sub> = (2.91 μA/kHz) f + I <sub>DD</sub>							
		15	I <sub>T</sub> = (4.37 μA/kHz) f + I <sub>DD</sub>							

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V<sub>DD</sub> = 5.0 Vdc

2.0 Vdc min @ V<sub>DD</sub> = 10 Vdc

2.5 Vdc min @ V<sub>DD</sub> = 15 Vdc

†To Calculate Total Current in General:

$$I_T \approx 2.2 \times V_{DD} \left( \frac{V_{COin} - 1.65}{R_1} + \frac{V_{DD} - 1.35}{R_2} \right)^{3/4} + 1.6 \times \left( \frac{V_{COin} - 1.65}{R_{SF}} \right)^{3/4} + 1 \times 10^{-3} (C_L + 9) V_{DD} f +$$

$$1 \times 10^{-1} V_{DD}^2 \left( \frac{100\% \text{ Duty Cycle of PCA}_{in}}{100} \right) + I_Q \quad \text{where: } I_T \text{ in } \mu\text{A}, C_L \text{ in pF, } V_{COin}, V_{DD} \text{ in Vdc, } f \text{ in kHz, and } R_1, R_2, R_{SF} \text{ in M}\Omega, C_L \text{ on } V_{COout}.$$

**ELECTRICAL CHARACTERISTICS\*** ( $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	V <sub>DD</sub> Vdc	Minimum	Typical	Maximum	Units
			Device		Device	
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	$t_{TLH}$	5.0 10 15	— — —	180 90 65	350 150 110	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	100 50 37	175 75 55	ns

**PHASE COMPARATORS 1 and 2**

Input Resistance — $PCA_{in}$	$R_{in}$	5.0 10 15	1.0 0.2 0.1	2.0 0.4 0.2	— — —	$M\Omega$
— $PCB_{in}$	$R_{in}$	15	150	1500	—	$M\Omega$
Minimum Input Sensitivity AC Coupled — $PCA_{in}$ C series = 1000 pF, $f = 50 \text{ kHz}$	$V_{in}$	5.0 10 15	— — —	200 400 700	300 600 1050	mV p-p
DC Coupled — $PCA_{in}$ , $PCB_{in}$	—	5 to 15	See Noise Immunity			

**VOLTAGE CONTROLLED OSCILLATOR (VCO)**

Maximum Frequency $(VCO_{in} = V_{DD}$ , $C1 = 50 \text{ pF}$ $R1 = 5.0 \text{ k}\Omega$ , and $R2 = \infty$ )	$f_{max}$	5.0 10 15	0.5 1.0 1.4	0.7 1.4 1.9	— — —	MHz
Temperature — Frequency Stability $(R2 = \infty)$	—	5.0 10 15	— — —	0.12 0.04 0.015	— — —	%/°C
Linearity ( $R2 = \infty$ ) $(VCO_{in} = 2.5 \text{ V} \pm 0.3 \text{ V}$ , $R1 > 10 \text{ k}\Omega$ ) $(VCO_{in} = 5.0 \text{ V} \pm 2.5 \text{ V}$ , $R1 > 400 \text{ k}\Omega$ ) $(VCO_{in} = 7.5 \text{ V} \pm 5.0 \text{ V}$ , $R1 \geq 1000 \text{ k}\Omega$ )	—	5.0 10 15	— — —	1.0 1.0 1.0	— — —	%
Output Duty Cycle	—	5 to 15	—	50	—	%
Input Resistance — $VCO_{in}$	$R_{in}$	15	150	1500	—	$M\Omega$

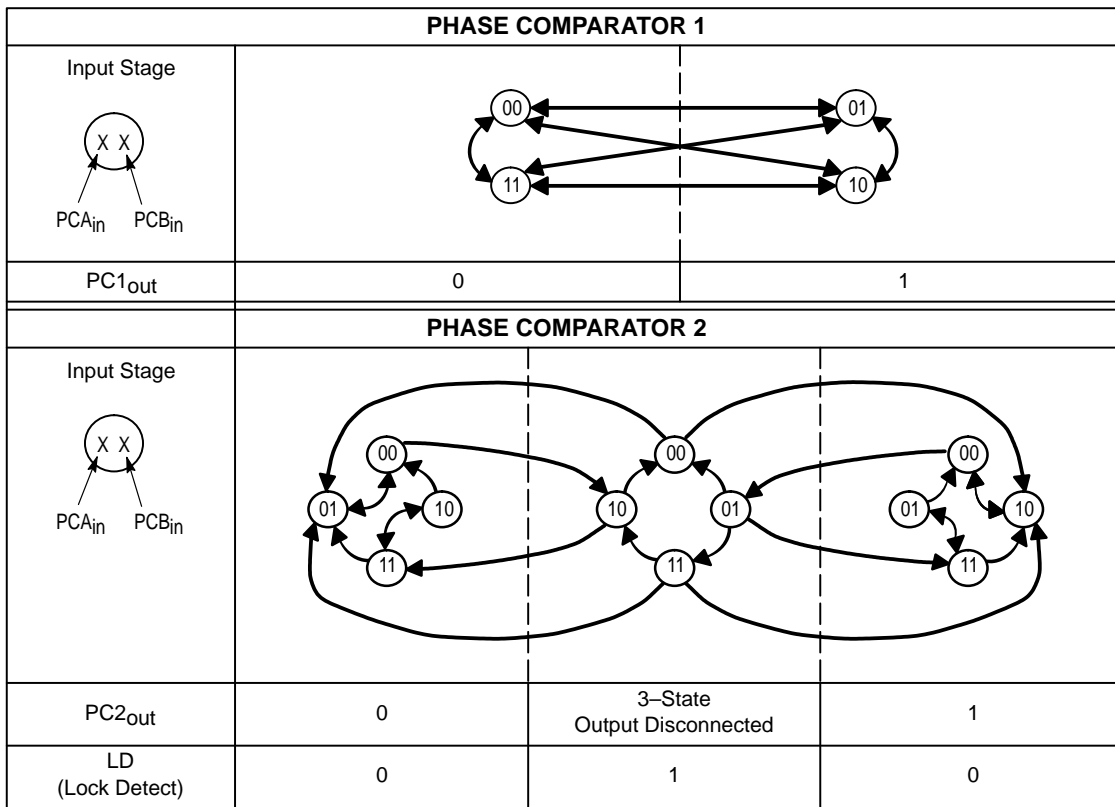
**SOURCE-FOLLOWER**

Offset Voltage $(VCO_{in}$ minus $SF_{out}$ , $RSF > 500 \text{ k}\Omega$ )	—	5.0 10 15	— — —	1.65 1.65 1.65	2.2 2.2 2.2	V
Linearity $(VCO_{in} = 2.5 \text{ V} \pm 0.3 \text{ V}$ , $RSF > 50 \text{ k}\Omega$ ) $(VCO_{in} = 5.0 \text{ V} \pm 2.5 \text{ V}$ , $RSF > 50 \text{ k}\Omega$ ) $(VCO_{in} = 7.5 \text{ V} \pm 5.0 \text{ V}$ , $RSF > 50 \text{ k}\Omega$ )	—	5.0 10 15	— — —	0.1 0.6 0.8	— — —	%

**ZENER DIODE**

Zener Voltage ( $I_Z = 50 \mu\text{A}$ )	$V_Z$	—	6.7	7.0	7.3	V
Dynamic Resistance ( $I_Z = 1.0 \text{ mA}$ )	$R_Z$	—	—	100	—	$\Omega$

\* The formula given is for the typical characteristics only.

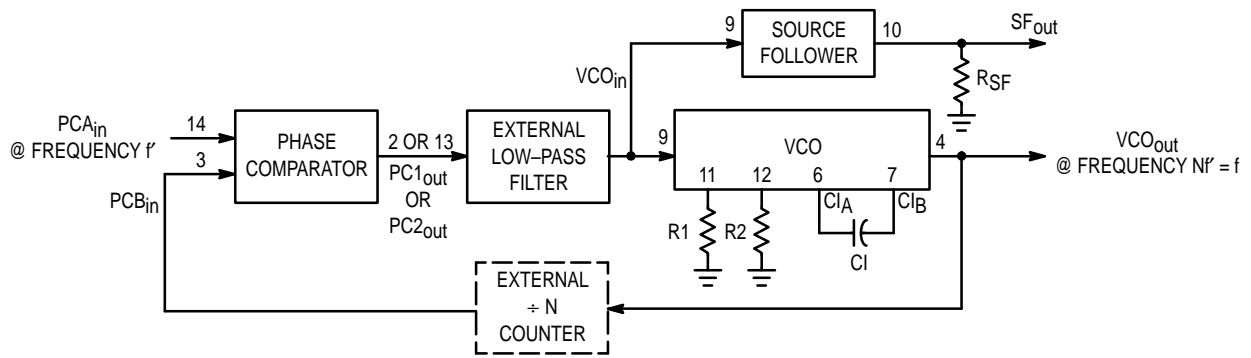


Refer to Waveforms in Figure 3.

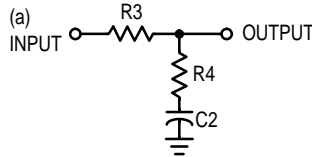
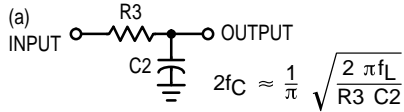
Figure 1. Phase Comparators State Diagrams

Characteristic	Using Phase Comparator 1	Using Phase Comparator 2
No signal on input PCA <sub>in</sub> .	VCO in PLL system adjusts to center frequency (f <sub>0</sub> ).	VCO in PLL system adjusts to minimum frequency (f <sub>min</sub> ).
Phase angle between PCA <sub>in</sub> and PCB <sub>in</sub> .	90° at center frequency (f <sub>0</sub> ), approaching 0° and 180° at ends of lock range (2f <sub>L</sub> )	Always 0° in lock (positive rising edges).
Locks on harmonics of center frequency.	Yes	No
Signal input noise rejection.	High	Low
Lock frequency range (2f <sub>L</sub> ).	The frequency range of the input signal on which the loop will stay locked if it was initially in lock; 2f <sub>L</sub> = full VCO frequency range = f <sub>max</sub> - f <sub>min</sub> .	
Capture frequency range (2f <sub>C</sub> ).	The frequency range of the input signal on which the loop will lock if it was initially out of lock.	
	Depends on low-pass filter characteristics (see Figure 3). f <sub>C</sub> ≤ f <sub>L</sub>	f <sub>C</sub> = f <sub>L</sub>
Center frequency (f <sub>0</sub> ).	The frequency of VCO <sub>out</sub> , when VCO <sub>in</sub> = 1/2 V <sub>DD</sub>	
VCO output frequency (f).	$f_{min} = \frac{1}{R_2(C_1 + 32 \text{ pF})} \quad (\text{VCO input} = V_{SS})$ $f_{max} = \frac{1}{R_1(C_1 + 32 \text{ pF})} + f_{min} \quad (\text{VCO input} = V_{DD})$ <p>Where: 10K ≤ R<sub>1</sub> ≤ 1 M  10K ≤ R<sub>2</sub> ≤ 1 M  100pF ≤ C<sub>1</sub> ≤ .01 μF</p>	
Note: These equations are intended to be a design guide. Since calculated component values may be in error by as much as a factor of 4, laboratory experimentation may be required for fixed designs. Part to part frequency variation with identical passive components is typically less than ± 20%.		

Figure 2. Design Information



### Typical Low-Pass Filters



Typically:

$$R_4 C_2 = \frac{6N}{f_{\max}} - \frac{N}{2\pi\Delta f}$$

$$(R_3 + 3,000\Omega) C_2 = \frac{100N\Delta f}{f_{\max}^2} - R_4 C_2$$

$$\Delta f = f_{\max} - f_{\min}$$

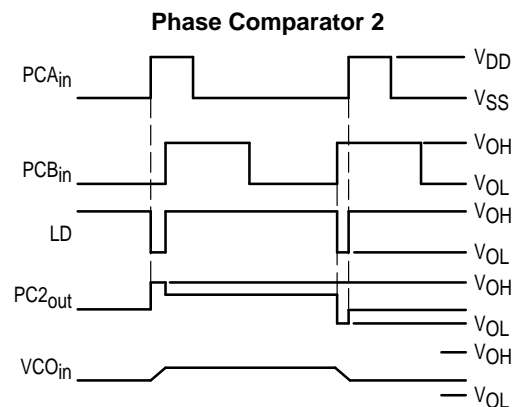
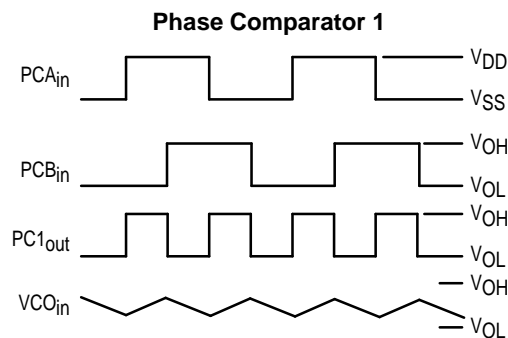
NOTE: Sometimes R3 is split into two series resistors each R3 ÷ 2. A capacitor C<sub>C</sub> is then placed from the midpoint to ground. The value for C<sub>C</sub> should be such that the corner frequency of this network does not significantly affect ω<sub>n</sub>. In Figure B, the ratio of R3 to R4 sets the damping, R4 ≅ (0.1)(R3) for optimum results.

### LOW-PASS FILTER

Definitions: N = Total division ratio in feedback loop  
 $K\phi = V_{DD}/\pi$  for Phase Comparator 1  
 $K\phi = V_{DD}/4\pi$  for Phase Comparator 2  
 $KVCO = \frac{2\pi\Delta fVCO}{V_{DD} - 2V}$   
 for a typical design  $\omega_n \cong \frac{2\pi f_r}{10}$  (at phase detector input)  
 $\zeta \cong 0.707$

Filter A	Filter B
$\omega_n = \sqrt{\frac{K\phi KVCO}{NR_3 C_2}}$	$\omega_n = \sqrt{\frac{K\phi KVCO}{NC_2(R_3 + R_4)}}$
$\zeta = \frac{N\omega_n}{2K\phi KVCO}$	$\zeta = 0.5 \omega_n (R_3 C_2 + \frac{N}{K\phi KVCO})$
$F(s) = \frac{1}{R_3 C_2 S + 1}$	$F(s) = \frac{R_3 C_2 S + 1}{S(R_3 C_2 + R_4 C_2) + 1}$

### Waveforms



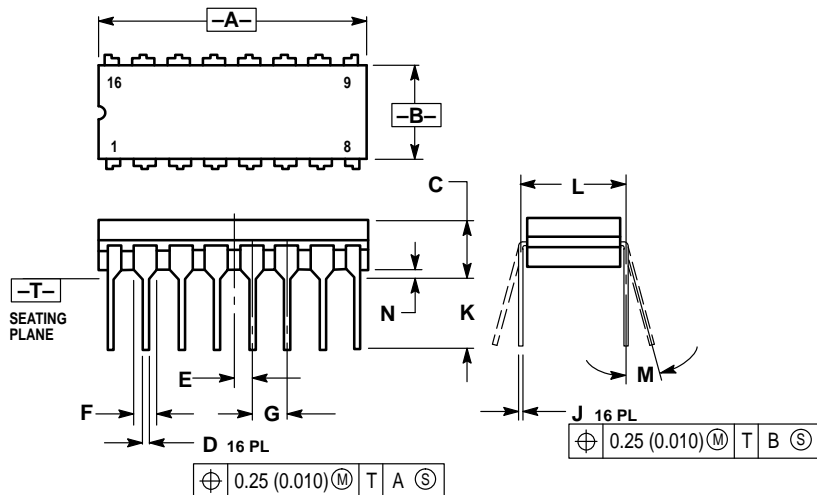
Note: for further information, see:

- (1) F. Gardner, "Phase-Lock Techniques", John Wiley and Son, New York, 1966.
- (2) G. S. Moschytz, "Miniature RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.
- (3) Garth Nash, "Phase-Lock Loop Design Fundamentals", AN-535, Motorola Inc.
- (4) A. B. Przedpelski, "Phase-Locked Loop Design Articles", AR254, reprinted by Motorola Inc.

Figure 3. General Phase-Locked Loop Connections and Waveforms

## OUTLINE DIMENSIONS

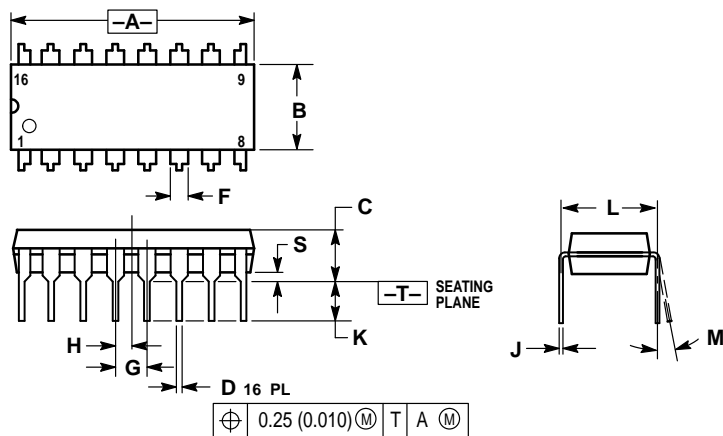
### L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

### P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R

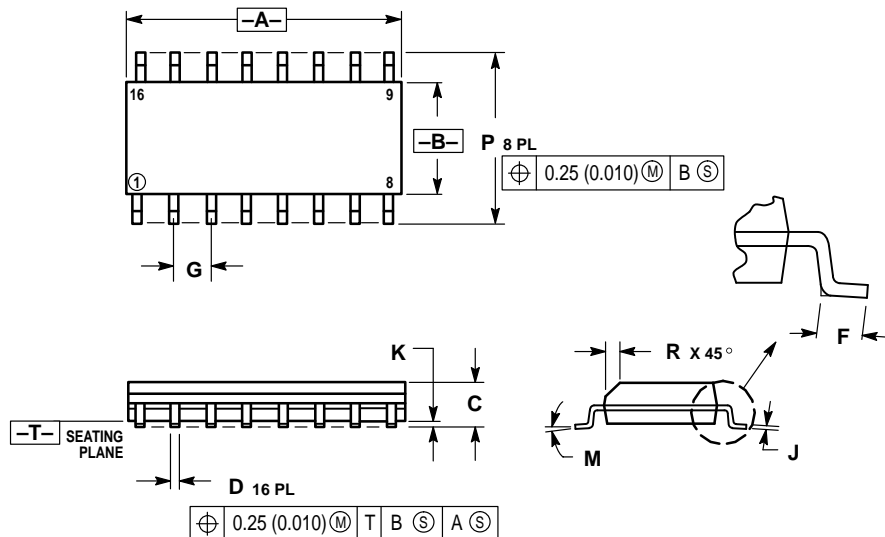


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

## OUTLINE DIMENSIONS

### D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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MC14046B/D

