

CD4067B, CD4097B Types

CMOS Analog Multiplexers/Demultiplexers

High-Voltage Types (20-Volt Rating)

CD4067B - Single 16-Channel Multiplexer/Demultiplexer

CD4097B - Differential 8-Channel Multiplexer/Demultiplexer

CD4067B and CD4097B CMOS

analog multiplexers/demultiplexers* are digitally controlled analog switches having low ON impedance, low OFF leakage current, and internal address decoding. In addition, the ON resistance is relatively constant over the full input-signal range.

The CD4067B is a 16-channel multiplexer with four binary control inputs, A, B, C, D, and an inhibit input, arranged so that any combination of the inputs selects one switch.

The CD4097B is a differential 8-channel multiplexer having three binary control inputs A, B, C, and an inhibit input. The inputs permit selection of one of eight pairs of switches.

A logic "1" present at the inhibit input turns all channels off.

The CD4067B and CD4097B types are supplied in 24-lead hermetic dual-in-line ceramic packages (F3A suffix), 24-lead dual-in-line plastic packages (E suffix), 24-lead small-outline packages (M, M96, and NSR suffixes), and 24-lead thin shrink small-outline packages (P and PWR suffixes).

*When these devices are used as demultiplexers, the channel in/out terminals are the outputs and the common out/in terminals are the inputs.

Recommended Operating Conditions at T_A = 25°C (Unless Otherwise Specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges. Values shown apply to all types except as noted.

Characteristic	Min.	Max.	Units
Supply-Voltage Range (T _A =Full Package-Temp. Range)	3	18	V
Multiplexer Switch Input Current Capability	-	25	mA
Output Load Resistance	100	-	Ω

NOTE:

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 1 on the CD4067; terminals 1 and 17 on the CD4097.

Features:

- Low ON resistance: 125 Ω (typ.) over 15 V_{pp} signal-input range for V_{DD}-V_{SS}=15 V
- High OFF resistance: channel leakage of ±10 pA (typ.) @ V_{DD}-V_{SS}=10 V
- Matched switch characteristics: R_{ON}=5 Ω (typ.) for V_{DD}-V_{SS}=15 V
- Very low quiescent power dissipation under all digital-control input and supply conditions: 0.2 μW (typ.) @ V_{DD}-V_{SS}=10 V
- Binary address decoding on chip
- 5-V, 10-V, and 15-V parametric ratings
- 100% tested for quiescent current at 20 V
- Standardized symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Analog and digital multiplexing and demultiplexing
- A/D and D/A conversion
- Signal gating

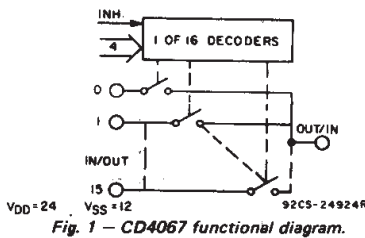
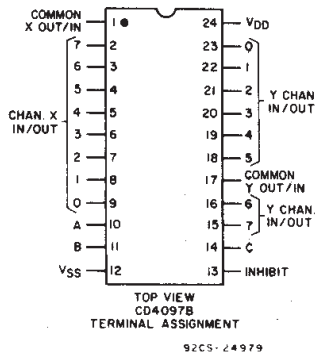
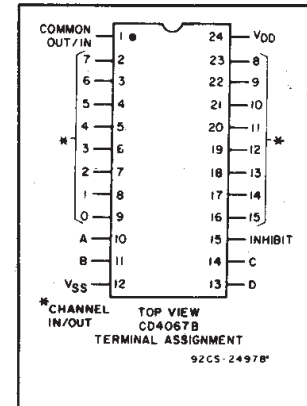


Fig. 1 - CD4067 functional diagram.

CD4067 TRUTH TABLE

A	B	C	D	Inh	Selected Channel
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

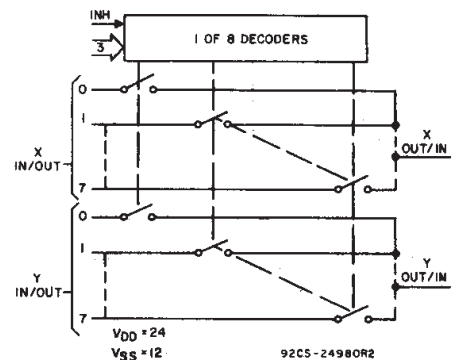


Fig. 2 - CD4097 functional diagram.

CD4097 TRUTH TABLE

A	B	C	Inh	Selected Channel
X	X	X	1	None
0	0	0	0	0X, 0Y
1	0	0	0	1X, 1Y
0	1	0	0	2X, 2Y
1	1	0	0	3X, 3Y
0	0	1	0	4X, 4Y
1	0	1	0	5X, 5Y
0	1	1	0	6X, 6Y
1	1	1	0	7X, 7Y

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ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						Units	
	V_{is} (V)	V_{SS} (V)	V_{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.		Max.
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{OS})											
Quiescent Device Current, I_{DD} Max.			5	5	5	150	150	—	0.04	5	μA
			10	10	10	300	300	—	0.04	10	
			15	20	20	600	600	—	0.04	20	
			20	100	100	3000	3000	—	0.08	100	
ON-state Resistance $V_{SS} \leq V_{is} \leq V_{DD}$ r_{on} Max.		0	5	800	850	1200	1300	—	470	1050	Ω
		0	10	310	330	520	550	—	180	400	
		0	15	200	210	300	320	—	125	240	
Change in on-state Resistance (Between Any Two Channels) Δr_{on}		0	5	—	—	—	—	—	15	—	Ω
		0	10	—	—	—	—	—	10	—	
		0	15	—	—	—	—	—	5	—	
OFF Channel Leakage Current: Any Channel OFF (Common OUT/IN) Max. or All Channels OFF		0	18	$\pm 100^*$		$\pm 1000^*$			± 0.1	$\pm 100^*$	nA
Capacitance: Input, C_{is}				—	—	—	—	—	5	—	pF
Output, C_{os}				—	—	—	—	—	55	—	
CD4067				—	—	—	—	—	35	—	
CD4097		-5	5	—	—	—	—	—	0.2	—	
Feed-through, C_{ios}				—	—	—	—	—	—	—	
				—	—	—	—	—	—	—	
				—	—	—	—	—	—	—	
Propagation Delay Time (Signal Input to Output)	V_{DD} 	$R_L = 200 K\Omega$ $C_L = 50 pF$ $t_r, t_f = 20 ns$	5	—	—	—	—	—	30	60	ns
			10	—	—	—	—	—	15	30	
			15	—	—	—	—	—	10	20	
CONTROL (ADDRESS or INHIBIT) V_C											
Input Low Voltage, V_{IL} Max.	$=V_{DD}$ thru $1 K\Omega$	$R_L = 1 K\Omega$ to V_{SS} $I_{IS} < 2 \mu A$ on all OFF Channels	5	1.5	—	—	—	—	—	1.5	V
			10	3	—	—	—	—	3		
			15	4	—	—	—	—	4		
Input High Voltage, V_{IH} Min.	$=V_{DD}$ thru $1 K\Omega$	$R_L = 1 K\Omega$ to V_{SS} $I_{IS} < 2 \mu A$ on all OFF Channels	5	3.5	3.5	—	—	—	—	—	
			10	7	7	—	—	—	—		
			15	11	11	—	—	—	—		

* Determined by minimum feasible leakage measurement for automatic testing.

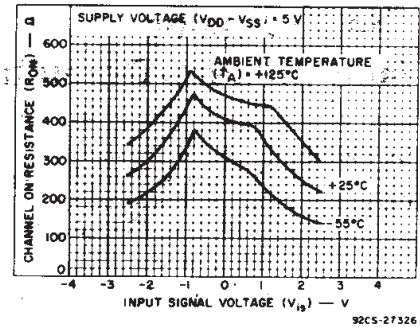


Fig. 3—Typical ON resistance vs. input signal voltage (all types).

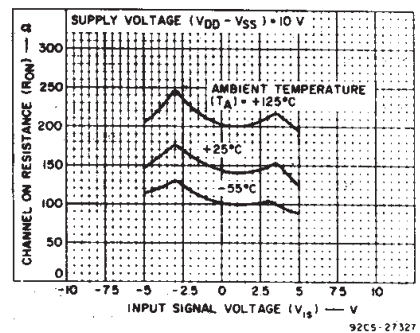


Fig. 4—Typical ON resistance vs. input signal voltage (all types).

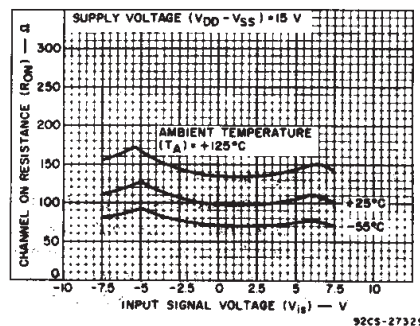


Fig. 5—Typical ON resistance vs. input signal voltage (all types).

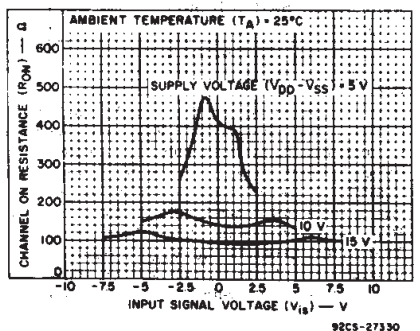


Fig. 6—Typical ON resistance vs. input signal voltage (all types).

CD4067B, CD4097B Types

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						Units	
	V _{is} (V)	V _{SS} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.		Max.
Input Current, I _{IN} Max.	V _{IN} = 0, 18 V			±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA
Propagation Delay Time: Address or Inhibit-to-Signal OUT (Channel turning ON)	R _L = 10 KΩ, C _L = 50 pF, t _r , t _f = 20 ns										ns
	0	5							325	650	
	0	10							135	270	
Address or Inhibit-to-Signal OUT (Channel turning OFF)	R _L = 300 Ω, C _L = 50 pF, t _r , t _f = 20 ns										ns
	0	5							220	440	
	0	10							90	180	
Input Capacitance, C _{IN}	Any Address or Inhibit Input										pF
	0	5							5	7.5	
	0	15									

TEST CIRCUITS

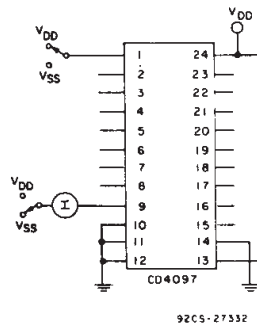
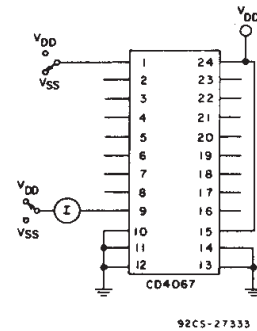


Fig. 7—OFF channel leakage current—any channel OFF.

MAXIMUM RATINGS, Absolute-Maximum Values:

- DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) -0.5V to +20V
- INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD} +0.5V
- DC INPUT CURRENT, ANY ONE INPUT ±10mA
- POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C Derate Linearly at 12mW/°C to 200mW
- DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
- OPERATING-TEMPERATURE RANGE (T_A) -55°C to +125°C
- STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to +150°C
- LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max +265°C

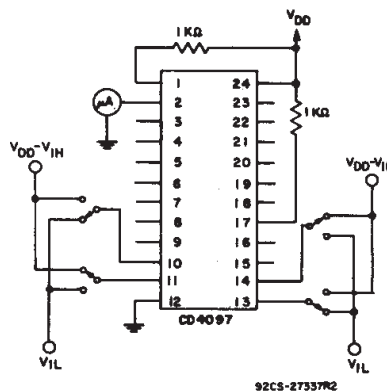
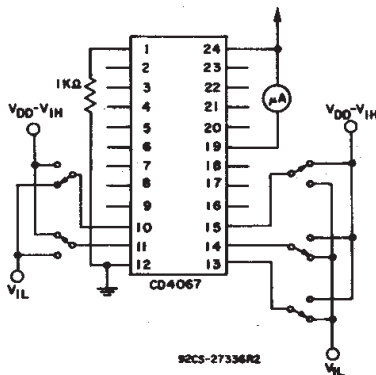


Fig. 8—Input voltage—measure < 2 μA on all OFF channels (e.g., channel 12).

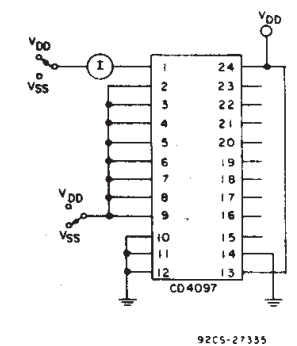
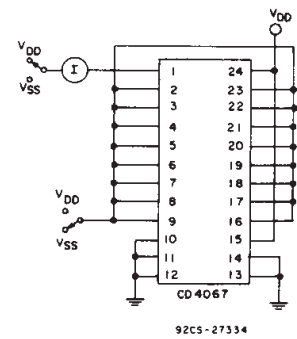


Fig. 9—OFF channel leakage current—all channels OFF.

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ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS			TYPICAL VALUES	UNITS			
	V _{is} (V)	V _{DD} (V)	R _L (KΩ)					
Cutoff (-3 dB) Frequency Channel ON (Sine Wave Input)	5 [●]	10	1	CD4067	14	MHz		
	20 log $\frac{V_{os}}{V_{is}} = -3$ dB			CD4097	20			
Total Harmonic Distortion, THD	f _{is} = 1 kHz sine wave			V _{os} at Common OUT/IN		%		
				V _{os} at Any Channel			60	
				2 [●]	5		10	0.3
				3 [●]	10			0.2
5 [●]	15	0.12						
-40 dB Feedthrough Frequency (All Channels OFF)	5 [●]	10	1	CD4067	20	MHz		
	20 log $\frac{V_{os}}{V_{is}} = -40$ dB			CD4097	12			
Signal Crosstalk (Frequency at -40 dB)	5 [●]	10	1	Between Any 2 Channels [▲]		1	MHz	
	20 log $\frac{V_{os}}{V_{is}} = -40$ dB			Between Sections CD4097 Only	Measured on Common	10		
					Measured on Any Channel	18		
Address-or-Inhibit-to-Signal Crosstalk	V _{SS} =0, t _r , t _f =20 ns, V _C =V _{DD} -V _{SS} (Square Wave)					75	mV (Peak)	

● Peak-to-peak voltage symmetrical about $\frac{V_{DD}-V_{SS}}{2}$.

▲ Worst case.

* Both ends of channel.

TEST CIRCUITS (Cont'd)

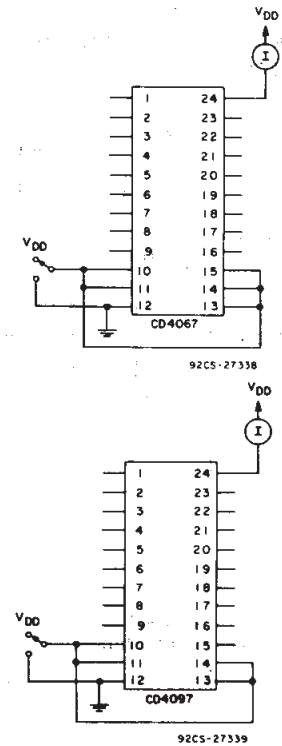


Fig. 10—Quiescent device current.

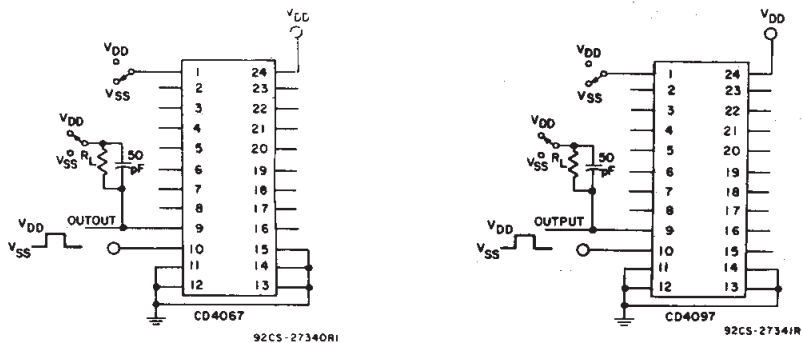


Fig. 11—Turn-on and turn-off propagation delay—address select input to signal output (e.g. measured on channel 0).

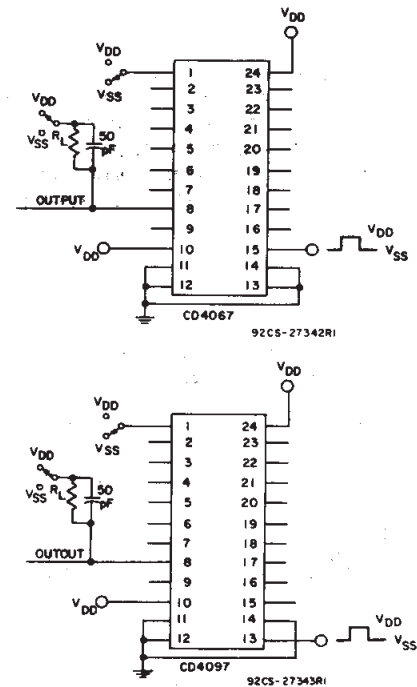


Fig. 12—Turn-on and turn-off propagation delay—
inhibit input to signal output (e.g. measured on channel 1).

CD4067B, CD4097B Types

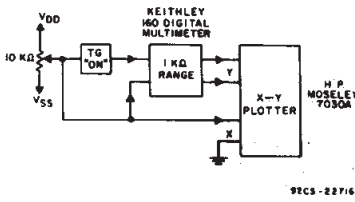


Fig. 13- Channel ON resistance measurement circuit.

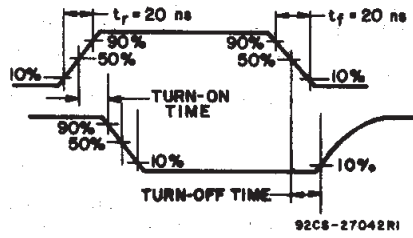


Fig. 14- Propagation delay waveform channel being turned ON ($R_L = 10\text{ K}\Omega$, $C_L = 50\text{ pF}$).

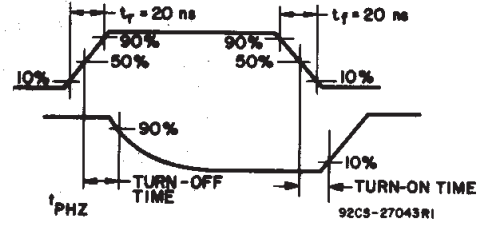


Fig. 15- Propagation delay waveform, channel being turned OFF ($R_L = 300\Omega$, $C_L = 50\text{ pF}$).

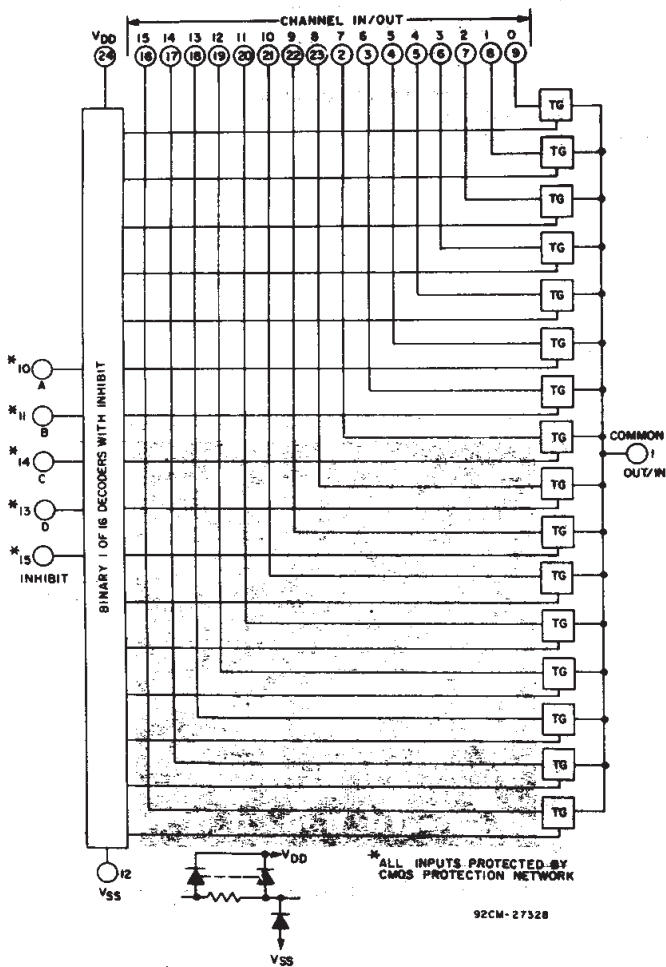


Fig. 16- CD4067 logic diagram.

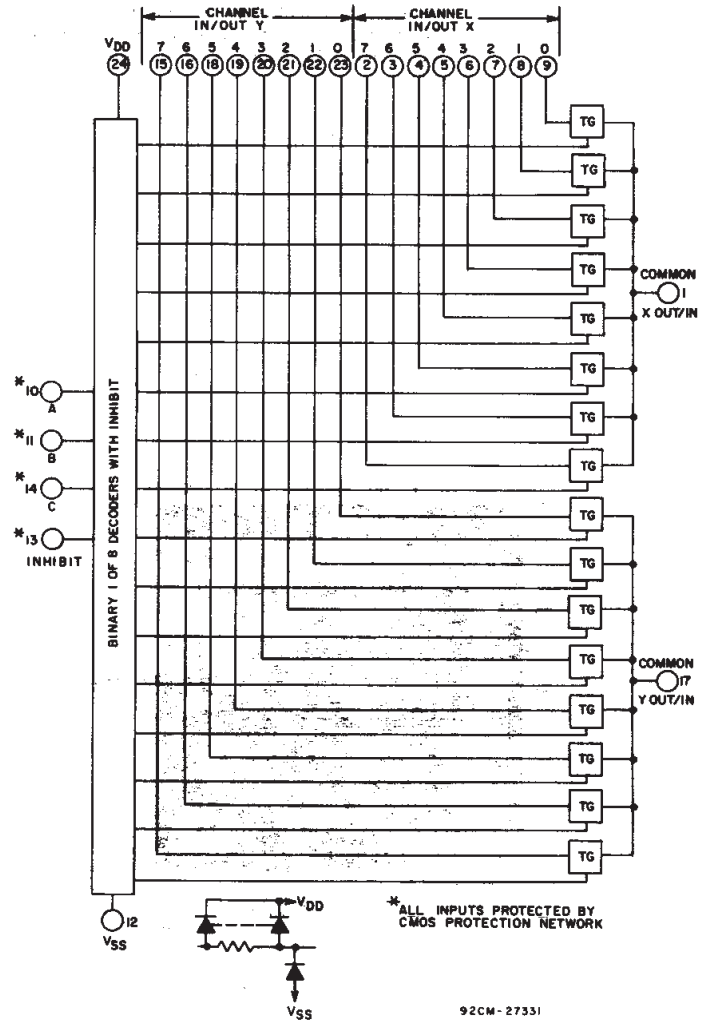


Fig. 17- CD4097 logic diagram.

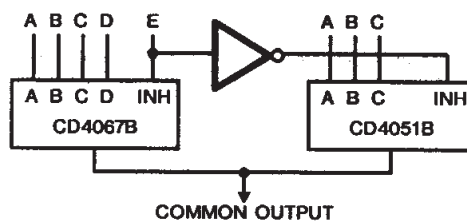


Fig. 18-24-to-1 MUX Addressing

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SPECIAL CONSIDERATIONS

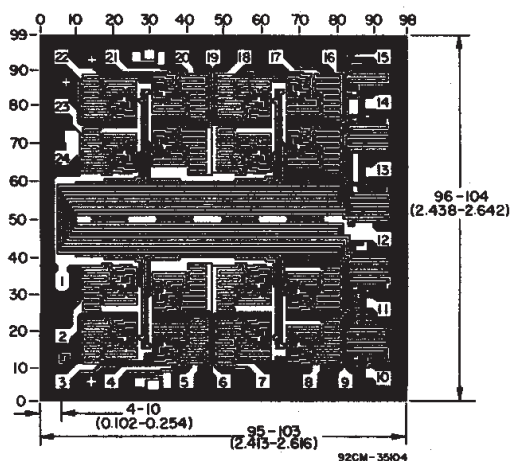
In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L =effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4067B or CD4097B.

When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned on or off by an address input, there is a momentary conductive path from the channel to V_{SS} , which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning on a channel will similarly dump some charge to V_{SS} .

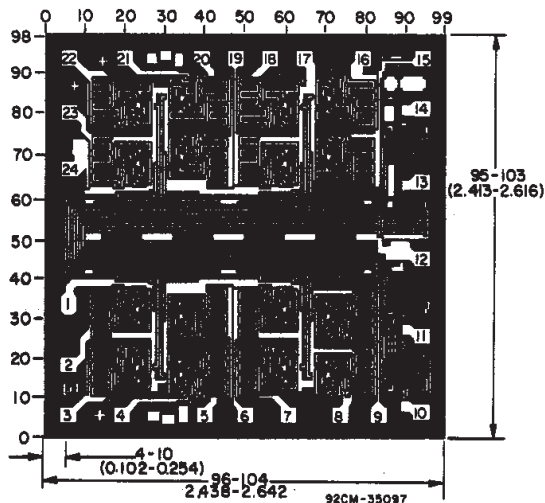
The amount of charge dumped is mostly a function of the signal level above V_{SS} . Typically, at $V_{DD}-V_{SS}=10$ V, a 100-pF

capacitor connected to the input or output of the channel will lose 3-4% of its voltage at the moment the channel turns on or off. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than 1-2 μ s. When the inhibit signal turns a channel off, there is no charge dumping to V_{SS} . Rather, there is a slight rise in the channel voltage level (65 mV typ.) due to capacitive coupling from inhibit input to channel input or output. Address inputs also couple some voltage steps onto the channel signal levels.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 1 on the CD4067B, terminals 1 and 17 on the CD4097B.



Dimensions and pad layout for CD4067BH.



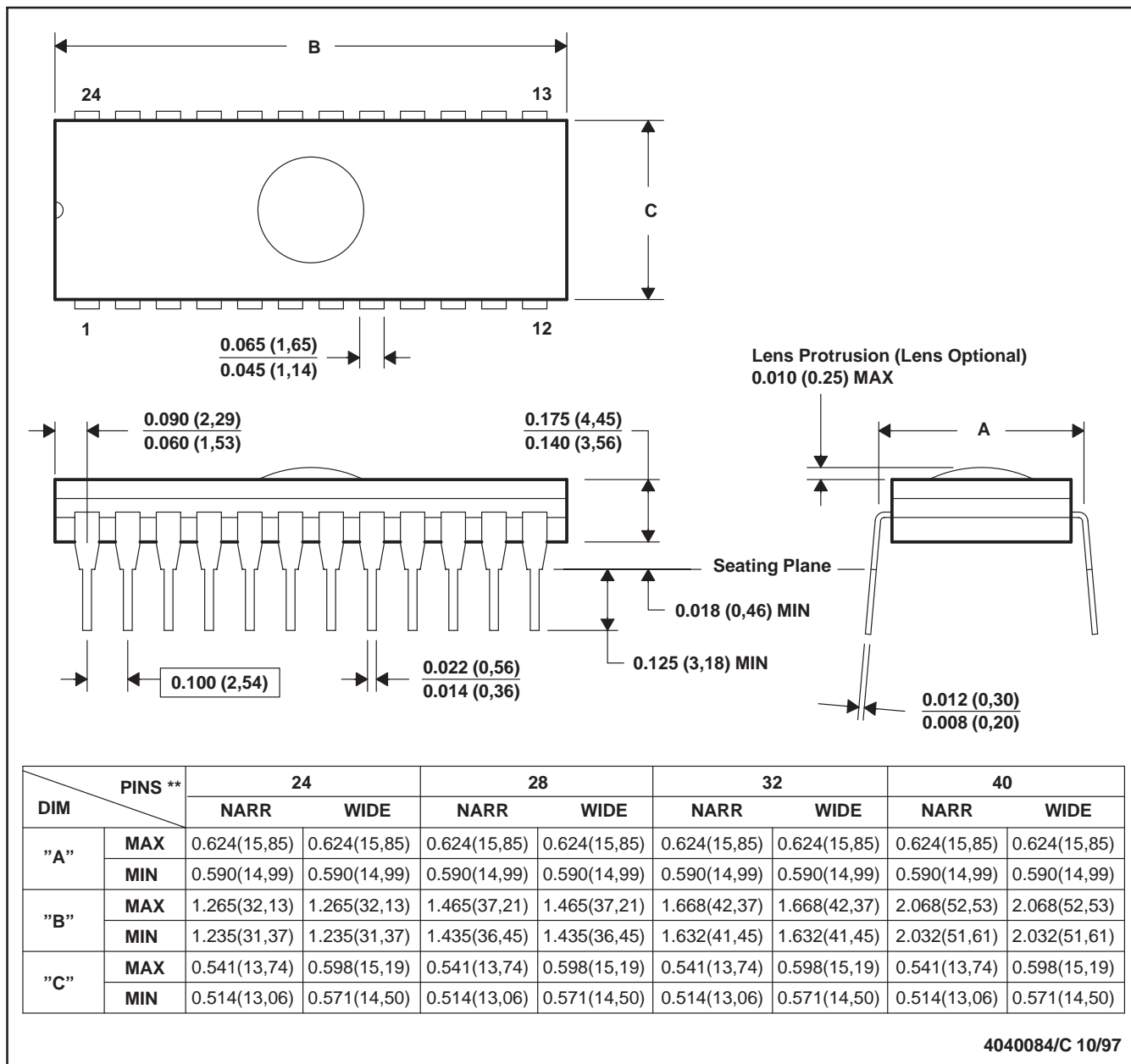
Dimensions and pad layout for CD4097BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE PACKAGE

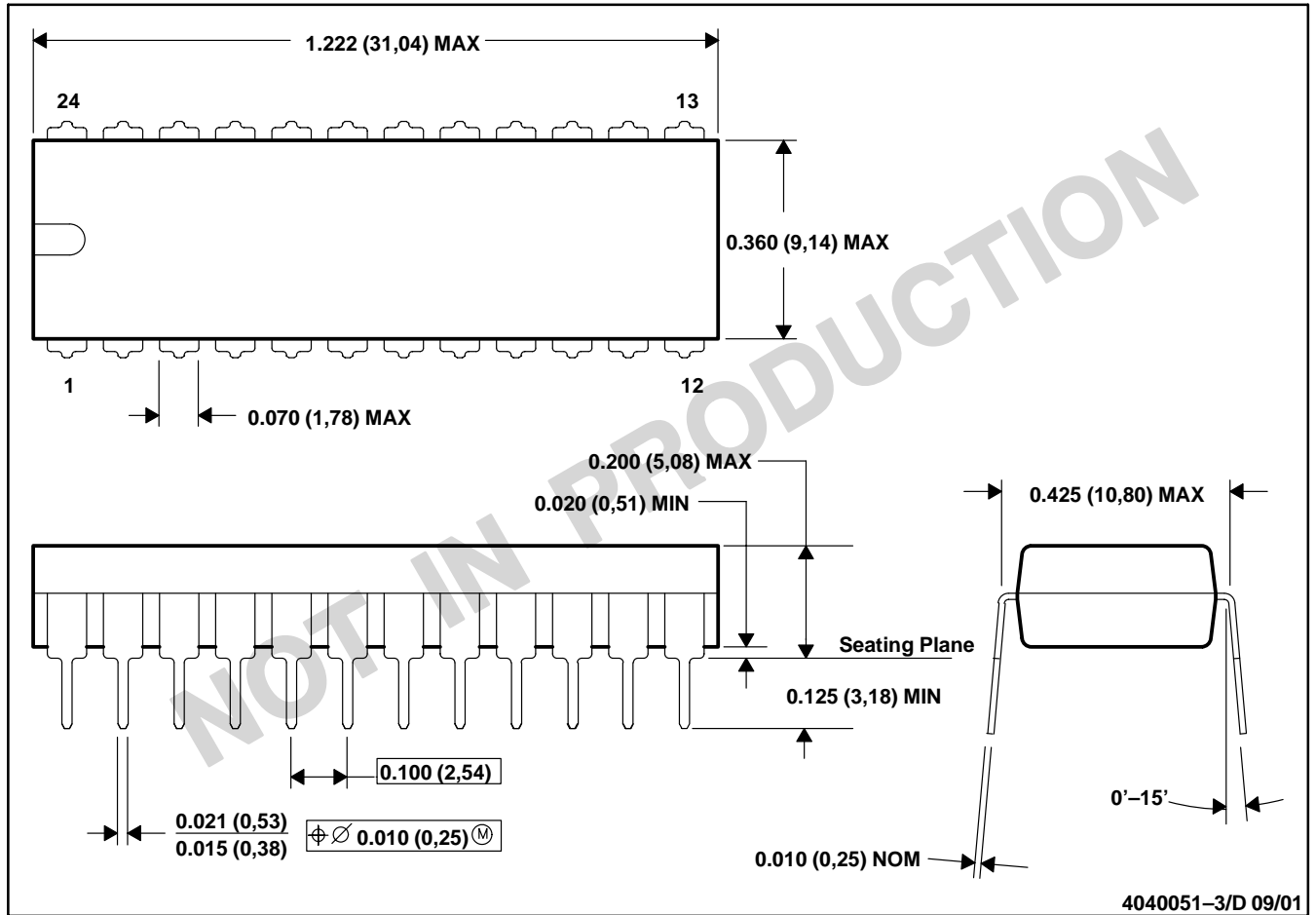
24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).
 D. This package can be hermetically sealed with a ceramic lid using glass frit.
 E. Index point is provided on cap for terminal identification.

N (R-PDIP-T24)

PLASTIC DUAL-IN-LINE

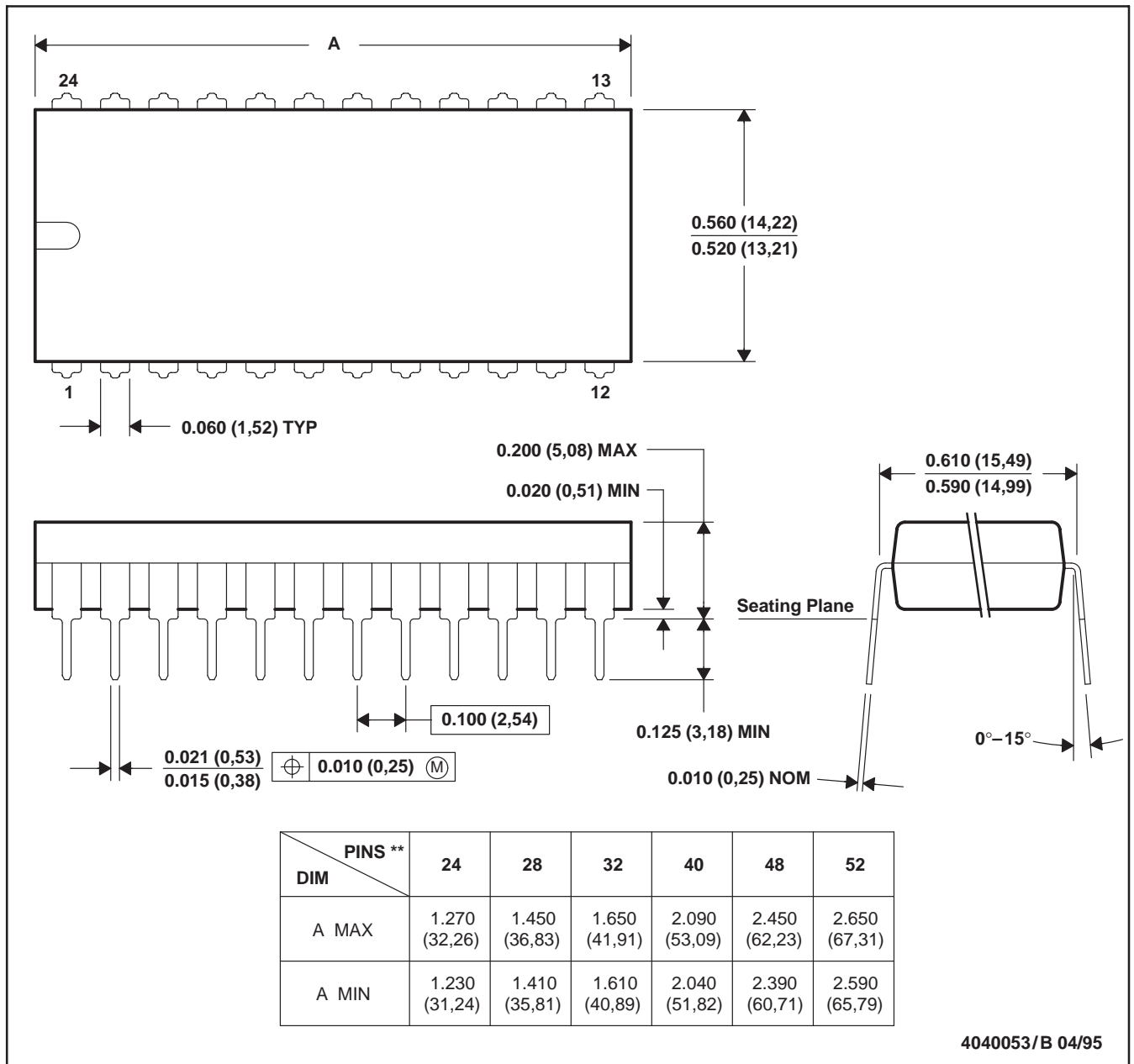


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-010

N (R-PDIP-T)**

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN

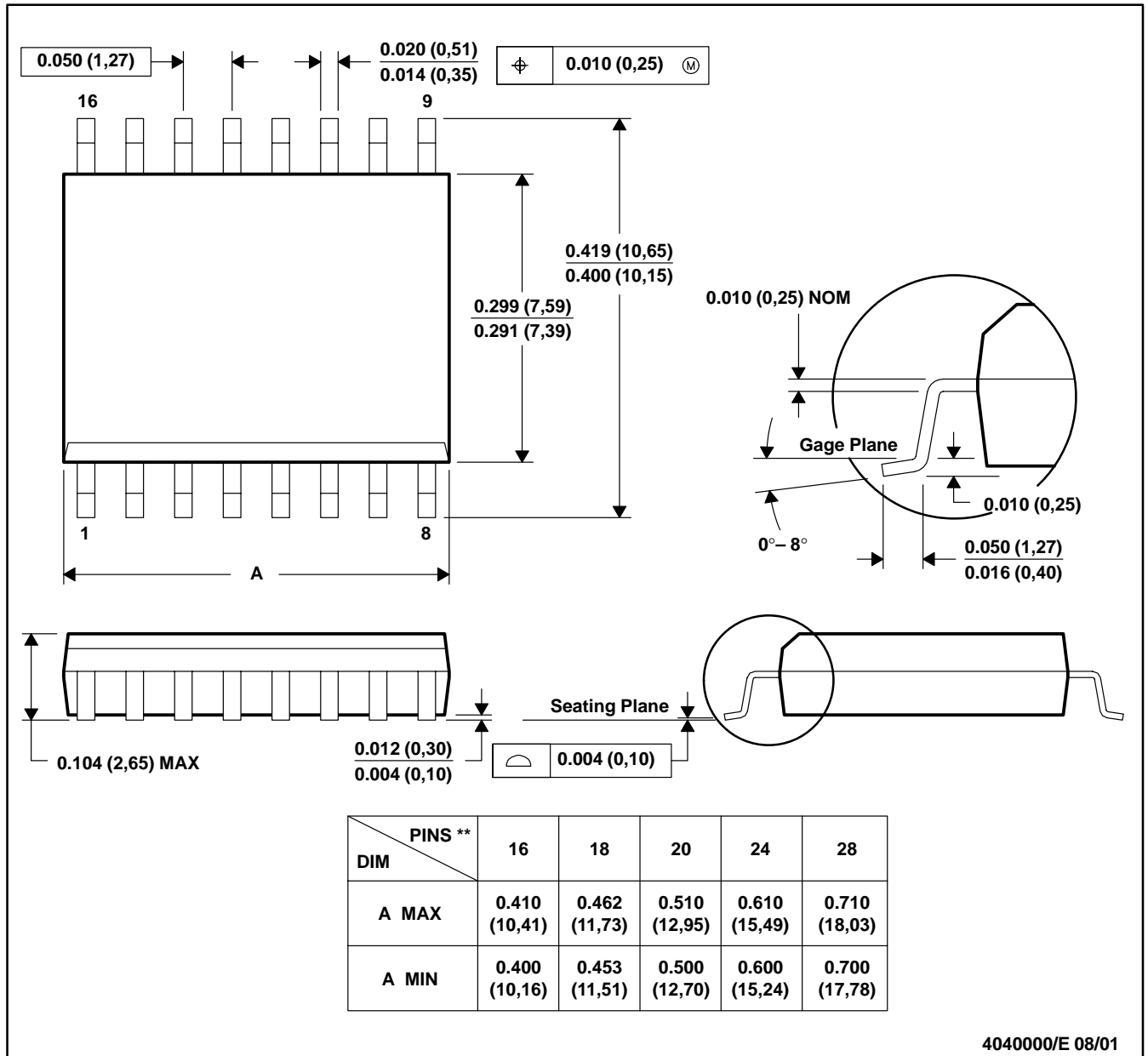


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-011
 D. Falls within JEDEC MS-015 (32 pin only)

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



4040000/E 08/01

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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