December 2003

ADC12L066
12-Bit, 66 MSPS, 450 MHz Bandwidth A/D Converter with Internal Sample-and-Hold

General Description

The ADC12L066 is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital words at 66 Megasamples per second (MSPS), minimum, with typical operation possible up to 80 MSPS. This converter uses a differential, pipeline architecture with digital error correction and an on-chip sample-and-hold circuit to minimize die size and power consumption while providing excellent dynamic performance. A unique sample-and-hold stage yields a full-power bandwidth of 450 MHz. Operating on a single 3.3V power supply, this device consumes just 357 mW at 66 MSPS, including the reference current. The Power Down feature reduces power consumption to just 50 mW.

The differential inputs provide a full scale input swing equal to $\pm V_{REF}$ with the possibility of a single-ended input. Full use of the differential input is recommended for optimum performance. For ease of use, the buffered, high impedance, single-ended reference input is converted on-chip to a differential reference for use by the processing circuitry. Output data format is 12-bit offset binary.

This device is available in the 32-lead LQFP package and will operate over the industrial temperature range of −40˚C to +85˚C. An evaluation board is available to facilitate the evaluation process.

Features

- Single supply operation
- Low power consumption
- Power down mode
- On-chip reference buffer

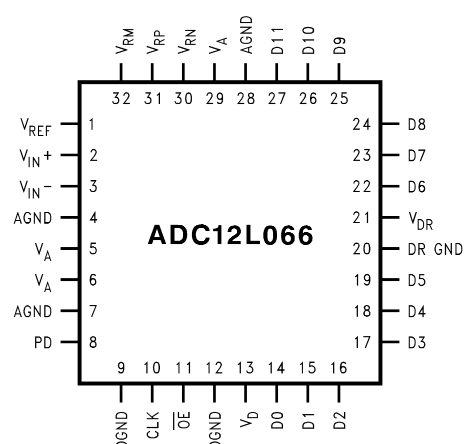
Key Specifications

Resolution	12 Bits
Conversion Rate	66 MSPS
Full Power Bandwidth	450 MHz
DNL	±0.4 LSB (typ)
SNR (f_{IN} = 10 MHz)	66 dB (typ)
SFDR (f_{IN} = 10 MHz)	80 dB (typ)
Data Latency	6 Clock Cycles
Supply Voltage	+3.3V ± 300 mV
Power Consumption, 66 MHz	357 mW (typ)

Applications

- Ultrasound and Imaging
- Instrumentation
- Cellular Base Stations/Communications Receivers
- Sonar/Radar
- xDSL
- Wireless Local Loops
- Data Acquisition Systems
- DSP Front Ends

Connection Diagram



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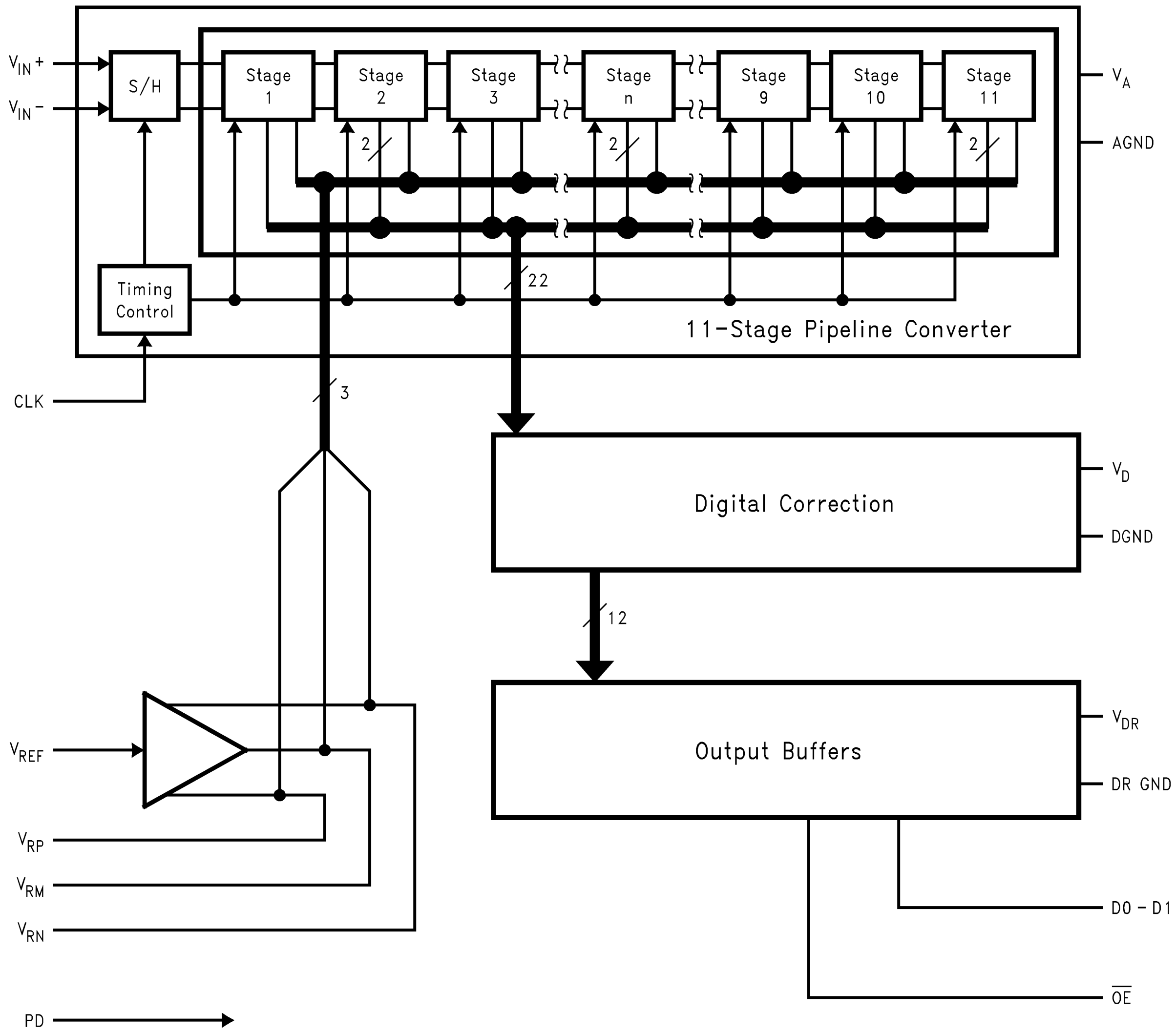
Ordering Information

Industrial (−40˚C ≤ T_A ≤ +85˚C)	Package
ADC12L066CIVY	32 Pin LQFP
ADC12L066CIVYX	32 Pin LQFP Tape and Reel
ADC12L066EVAL	Evaluation Board

Block Diagram



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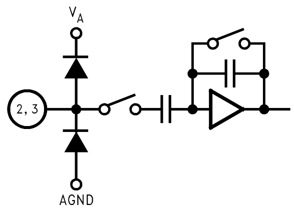
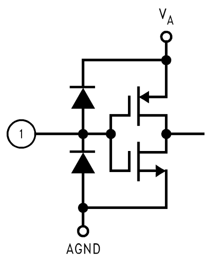
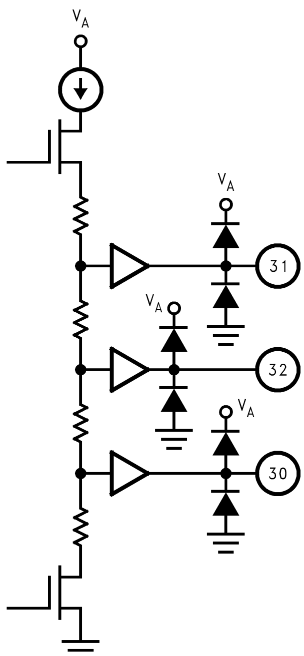
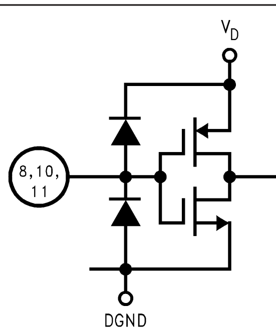
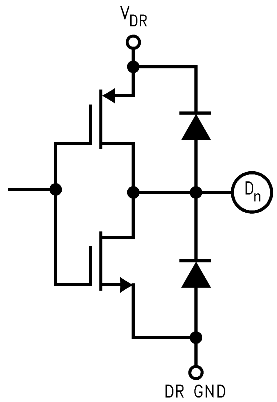
Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
2	V_{IN}^{+}		Analog signal Input pins. With a 1.0V reference voltage the differential input signal level is 2.0 V_{P-P}. The V_{IN^-} pin may be connected to V_{CM} for single-ended operation, but a differential input signal is required for best performance.
3	V_{IN}^{-}		
1	V_{REF}		Reference input. This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. V_{REF} is 1.0V nominal and should be between 0.8V and 1.5V.
31	V_{RP}		These pins are high impedance reference bypass pins. Connect a 0.1 µF capacitor from each of these pins to AGND. DO NOT LOAD these pins.
32	V_{RM}		
30	V_{RN}		
DIGITAL I/O			
10	CLK		Digital clock input. The range of frequencies for this input is 1 MHz to 80 MHz (typical) with guaranteed performance at 66 MHz. The input is sampled on the rising edge of this input.
11	$\overline{OE}$		$\overline{OE}$ is the output enable pin that, when low, enables the TRI-STATE® data output pins. When this pin is high, the outputs are in a high impedance state.
8	PD		PD is the Power Down input pin. When high, this input puts the converter into the power down mode. When this pin is low, the converter is in the active mode.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
14–19, 22–27	D0–D11		Digital data output pins that make up the 12-bit conversion results. D0 is the LSB, while D11 is the MSB of the offset binary output word.
ANALOG POWER			
5, 6, 29	V_A		Positive analog supply pins. These pins should be connected to a quiet +3.3V source and bypassed to AGND with 0.1 µF monolithic capacitors located within 1 cm of these power pins, and with a 10 µF capacitor.
4, 7, 28	AGND		The ground return for the analog supply.
DIGITAL POWER			
13	V_D		Positive digital supply pin. This pin should be connected to the same quiet +3.3V source as is V_A and bypassed to DGND with a 0.1 µF monolithic capacitor in parallel with a 10 µF capacitor, both located within 1 cm of the power pin.
9, 12	DGND		The ground return for the digital supply.
21	V_{DR}		Positive digital supply pin for the ADC12L066's output drivers. This pin should be connected to a voltage source of +1.8V to V_D and bypassed to DR GND with a 0.1 µF monolithic capacitor. If the supply for this pin is different from the supply used for V_A and V_D, it should also be bypassed with a 10 µF tantalum capacitor. The voltage at this pin should never exceed the voltage on V_D by more than 300 mV. All bypass capacitors should be located within 1 cm of the supply pin.
20	DR GND		The ground return for the digital supply for the ADC12L066's output drivers. This pin should be connected to the system digital ground, but not be connected in close proximity to the ADC12L066's DGND or AGND pins. See Section 5.0 (Layout and Grounding) for more details.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_A, V_D, V_{DR}	4.2V
$\|V_A–V_D\|$	≤ 100 mV
Voltage on Any Pin	−0.3V to (V_A or V_D +0.3V)
Input Current at Any Pin (Note 3)	±25 mA
Package Input Current (Note 3)	±50 mA
Package Dissipation at T_A = 25˚C	See (Note 4)
ESD Susceptibility	
Human Body Model (Note 5)	2500V
Machine Model (Note 5)	250V
Soldering Temperature, Infrared, 10 sec. (Note 6)	235˚C
Storage Temperature	−65˚C to +150˚C

Operating Ratings (Notes 1, 2)

Operating Temperature	−40˚C ≤ T_A ≤ +85˚C
Supply Voltage (V_A, V_D)	+3.0V to +3.60V
Output Driver Supply (V_{DR})	+1.8V to V_D
V_{REF} Input	0.8V to 1.5V
CLK, PD, $\overline{OE}$	−0.05V to (V_D + 0.05V)
V_{IN} Input	−0V to (V_A − 0.5V)
V_{CM}	0.5V to (V_A -1.5V)
|AGND−DGND|	≤100 mV

Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, V_{REF} = +1.0V, V_{CM} = 1.0V, f_{CLK} = 66 MHz, t_r = t_f = 2 ns, C_L = 15 pF/pin. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25˚C (Notes 7, 8, 9, 10)

Symbol	Parameter	Conditions		Typical (Note 10)	Limits (Note 10)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				**12**	Bits
INL	Integral Non Linearity (Note 11)			±1.2	**+2.7**	LSB (max)
					−3	LSB (min)
DNL	Differential Non Linearity			±0.4	**+1**	LSB (max)
					−0.95	LSB (min)
GE	Gain Error	Positive Error		−0.15	**±3**	%FS (max)
		Negative Error		+0.4	**+4**	%FS (max)
					−5	%FS (min)
	Offset Error (V_{IN}+ = V_{IN}−)			+0.2	**±1.3**	%FS (max)
	Under Range Output Code			0	**0**	
	Over Range Output Code			4095	**4095**	
REFERENCE AND ANALOG INPUT CHARACTERISTICS						
V_{CM}	Common Mode Input Voltage			1.0	**0.5**	V (min)
					1.5	V (max)
C_{IN}	V_{IN} Input Capacitance (each pin to GND)	V_{IN} + 1.0 Vdc + 1 V_{P-P}	(CLK LOW)	8		pF
			(CLK HIGH)	7		pF
V_{REF}	Reference Voltage (Note 13)			1.0	**0.8**	V (min)
					1.5	V (max)
	Reference Input Resistance			100		MΩ (min)

Converter Electrical Characteristics (Continued)

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, $V_A = V_D = +3.3V$, $V_{DR} = +2.5V$, PD = 0V, $V_{REF} = +1.0V$, $V_{CM} = 1.0V$, $f_{CLK} = 66$ MHz, $t_r = t_f = 2$ ns, $C_L = 15$ pF/pin. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}:** all other limits $T_J = 25°C$ (Notes 7, 8, 9, 10)

Symbol	Parameter	Conditions		Typical (Note 10)	Limits (Note 10)	Units (Limits)
DYNAMIC CONVERTER CHARACTERISTICS						
BW	Full Power Bandwidth	0 dBFS Input, Output at −3 dB		450		MHz
SNR	Signal-to-Noise Ratio	f_{IN} = 10 MHz, V_{IN} = −0.5 dBFS	85˚C	66	64.6	dB (min)
			25˚C		65	dB (min)
			−40˚C		64.6	dB (min)
		f_{IN} = 25 MHz, V_{IN} = −0.5 dBFS		65		dB
		f_{IN} = 150 MHz, V_{IN} = −6 dBFS	85˚C	55	52	dB (min)
			25˚C		54	dB (min)
			−40˚C		51	dB (min)
		f_{IN} = 240 Hz, V_{IN} = −6 dBFS		52		dB
SINAD	Signal-to-Noise & Distortion	f_{IN} = 10 MHz, V_{IN} = −0.5 dBFS	85˚C	66	64.3	dB (min)
			25˚C		64.8	dB (min)
			−40˚C		63	dB (min)
		f_{IN} = 25 MHz, V_{IN} = −0.5 dBFS		64		dB
		f_{IN} = 150 MHz, V_{IN} = −6 dBFS	85˚C	55	51.8	dB (min)
			25˚C		53.9	dB (min)
			−40˚C		50	dB (min)
		f_{IN} = 240 Hz, V_{IN} = −6 dBFS		51		dB
ENOB	Effective Number of Bits	f_{IN} = 10 MHz, V_{IN} = −0.5 dBFS	85˚C	10.7	10.3	
			25˚C		10.5	Bits (min)
			−40˚C		10.2	
		f_{IN} = 25 MHz, V_{IN} = −0.5 dBFS		10.3		Bits
		f_{IN} = 150 MHz, V_{IN} = −6 dBFS	85˚C	8.8	8.3	
			25˚C		8.6	Bits (min)
			−40˚C		8.0	
		f_{IN} = 240 Hz, V_{IN} = −6 dBFS		8.2		Bits

Converter Electrical Characteristics (Continued)

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, V_{REF} = +1.0V, V_{CM} = 1.0V, f_{CLK} = 66 MHz, t_r = t_f = 2 ns, C_L = 15 pF/pin. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25˚C (Notes 7, 8, 9, 10)

Symbol	Parameter	Conditions		Typical (Note 10)	Limits (Note 10)	Units (Limits)
2nd Harm	Second Harmonic Distortion	f_{IN} = 10 MHz, V_{IN} = −0.5 dBFS	85˚C	−80	−73	dB(max)
			25˚C		−73	dB (max)
			−40˚C		−68	dB (max)
		f_{IN} = 25 MHz, V_{IN} = −0.5 dBFS		−80		dB
		f_{IN} = 150 MHz, V_{IN} = −6 dBFS	85˚C	−81	−66	dB(max)
			25˚C		−66	dB (max)
			−40˚C		−56	dB (max)
		f_{IN} = 240 Hz, V_{IN} = −6 dBFS		−61		dB
3rd Harm	Third Harmonic Distortion	f_{IN} = 10 MHz, V_{IN} = −0.5 dBFS	85˚C	−84	−74	dB(max)
			25˚C		−74	dB (max)
			−40˚C		−71	dB (max)
		f_{IN} = 25 MHz, V_{IN} = −0.5 dBFS		−79		dB
		f_{IN} = 150 MHz, V_{IN} = −6 dBFS	85˚C	−78	−68	dB(max)
			25˚C		−68	dB (max)
			−40˚C		−64	dB (max)
		f_{IN} = 240 Hz, V_{IN} = −6 dBFS		−78		dB
THD	Total Harmonic Distortion	f_{IN} = 10 MHz, V_{IN} = −0.5 dBFS	85˚C	−77	−72	dB(max)
			25˚C		−72	dB (max)
			−40˚C		−66	dB (max)
		f_{IN} = 25 MHz, V_{IN} = −0.5 dBFS		−71		dB
		f_{IN} = 150 MHz, V_{IN} = −6 dBFS	85˚C	−69	−63	dB(max)
			25˚C		−63	dB (max)
			−40˚C		−53	dB (max)
		f_{IN} = 240 Hz, V_{IN} = −6 dBFS		−57		dB

Converter Electrical Characteristics (Continued)

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, $V_A = V_D = +3.3V$, $V_{DR} = +2.5V$, PD = 0V, $V_{REF} = +1.0V$, $V_{CM} = 1.0V$, $f_{CLK} = 66$ MHz, $t_r = t_f = 2$ ns, $C_L = 15$ pF/pin. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}:** all other limits $T_J = 25°C$ (Notes 7, 8, 9, 10)

Symbol	Parameter	Conditions		Typical (Note 10)	Limits (Note 10)	Units (Limits)
SFDR	Spurious Free Dynamic Range	$f_{IN} = 10$ MHz, $V_{IN} = -0.5$ dBFS	85˚C	80	73	
			25˚C		73	dB (min)
			−40˚C		68	
		$f_{IN} = 25$ MHz, $V_{IN} = -0.5$ dBFS		73		dB
		$f_{IN} = 150$ MHz, $V_{IN} = -6$ dBFS	85˚C	74	66	
			25˚C		66	dB (min)
			−40˚C		56	
		$f_{IN} = 240$ Hz, $V_{IN} = -6$ dBFS		61		dB

DC and Logic Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, $V_A = V_D = +3.3V$, $V_{DR} = +2.5V$, PD = 0V, $V_{REF} = +1.0V$, $V_{CM} = 1.0V$, $f_{CLK} = 66$ MHz, $t_r = t_f = 2$ ns, $C_L = 15$ pF/pin. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}:** all other limits $T_J = 25°C$ (Notes 7, 8, 9, 10)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 10)	Units (Limits)
CLK, PD, $\overline{OE}$ DIGITAL INPUT CHARACTERISTICS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_D = 3.3V$		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$V_D = 3.3V$		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN^+}, V_{IN^-} = 3.3V$	10		µA
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN^+}, V_{IN^-} = 0V$	−10		µA
C_{IN}	Digital Input Capacitance		5		pF
D0–D11 DIGITAL OUTPUT CHARACTERISTICS					
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_{OUT} = -0.5$ mA		**V_{DR} − 0.18**	V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_{OUT} = 1.6$ mA		**0.4**	V (max)
I_{OZ}	TRI-STATE Output Current	$V_{OUT} = 3.3V$	100		nA
		$V_{OUT} = 0V$	−100		nA
$+I_{SC}$	Output Short Circuit Source Current	$V_{OUT} = 0V$	−20		mA
$-I_{SC}$	Output Short Circuit Sink Current	$V_{OUT} = 2.5V$	20		mA
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	PD Pin = DGND, $V_{REF} = 1.0V$ PD Pin = V_{DR}	103 4	**139**	mA (max) mA
I_D	Digital Supply Current	PD Pin = DGND PD Pin = V_{DR}	5.3 2	**6.2**	mA (max) mA
I_{DR}	Digital Output Supply Current	PD Pin = DGND, (Note 14) PD Pin = V_{DR}	<1 0		mA mA
	Total Power Consumption	PD Pin = DGND, $C_L = 0$ pF (Note 15) PD Pin = V_{DR}	357 50	**479**	mW (max) mW
PSRR1	Power Supply Rejection	Rejection of Full-Scale Error with $V_A = 3.0V$ vs. 3.6V	58		dB

AC Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, V_{REF} = +1.0V, V_{CM} = 1.0V, f_{CLK} = 66 MHz, t_r = t_f = 2 ns, C_L = 15 pF/pin. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX}:** all other limits T_A = T_J = 25˚C (Notes 7, 8, 9, 10, 12)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 10)	Units (Limits)
$f_{CLK}1$	Maximum Clock Frequency		80	**66**	MHz (min)
$f_{CLK}2$	Minimum Clock Frequency		1		MHz
DC	Clock Duty Cycle		40 60		% (min) % (max)
t_{CH}	Clock High Time		6.5		ns (min)
t_{CL}	Clock Low Time		6.5		ns (min)
t_{CONV}	Conversion Latency			**6**	Clock Cycles
t_{OD}	Data Output Delay after Rising CLK Edge	V_{DR} = 2.5V	7.5	**11**	ns (max)
		V_{DR} = 3.3V	6.7	**10.5**	ns (max)
t_{AD}	Aperture Delay		2		ns
t_{AJ}	Aperture Jitter		1.2		ps rms
t_{DIS}	Data outputs into TRI-STATE Mode		10		ns
t_{EN}	Data Outputs Active after TRI-STATE		10		ns
t_{PD}	Power Down Mode Exit Cycle	0.1 µF on pins 30, 31, 32	300		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.

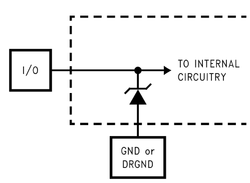
Note 3: When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or V_{IN} > V_A, V_D or V_{DR}), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

Note 4: The absolute maximum junction temperature ($T_J$max) for this device is 150˚C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature, (T_A), and can be calculated using the formula P_DMAX - ($T_J$max - T_A)/θ_{JA}. In the 32-pin LQFP, θ_{JA} is 79˚C/W, so P_DMAX = 1,582 mW at 25˚C and 823 mW at the maximum operating ambient temperature of 85˚C. Note that the power consumption of this device under normal operation will typically be about 612 mW (357 typical power consumption + 255 mW output loading with 250 MHz input). The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

Note 5: Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through 0Ω.

Note 6: The 235˚C reflow temperature refers to infrared reflow. For Vapor Phase Reflow (VPR), the following Conditions apply: Maintain the temperature at the top of the package body above 183˚C for a minimum 60 seconds. The temperature measured on the package body must not exceed 220˚C. Only one excursion above 183˚C is allowed per reflow cycle.

Note 7: The inputs are protected as shown below. Input voltages above V_A or below GND will not damage this device, provided current is limited per (Note 3). However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is 3.3V, the full-scale input voltage must be ≤3.4V to ensure accurate conversions.



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Note 8: To guarantee accuracy, it is required that $|V_A–V_D|$ ≤ 100 mV and separate bypass capacitors are used at each power supply pin.

Note 9: With the test condition for V_{REF} = +1.0V (2 V_{P-P} differential input), the 12-bit LSB is 488 µV.

Note 10: Typical figures are at T_A = T_J = 25˚C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 11: Integral Non Linearity is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive and negative full-scale.

Note 12: Timing specifications are tested at TTL logic levels, V_{IL} = 0.4V for a falling edge and V_{IH} = 2.4V for a rising edge.

Note 13: Optimum dynamic performance will be obtained by keeping the reference input in the 0.8V to 1.5V range. The LM4051CIM3-ADJ or the LM4051CIM3-1.2 bandgap voltage reference is recommended for this application.

Note 14: I_{DR} is the current consumed by the switching of the output drivers and is primarily determined by load capacitance on the output pins, the supply voltage, V_{DR}, and the rate at which the outputs are switching (which is signal dependent). $I_{DR}=V_{DR}(C_0 \times f_0 + C_1 \times f_1 + ...C_{11} \times f_{11})$ where V_{DR} is the output driver power supply voltage, C_n is total capacitance on the output pin, and f_n is the average frequency at which that pin is toggling.

Note 15: Power consumption excludes output driver power. See (Note 14).

Specification Definitions

APERTURE DELAY is the time after the rising edge of the clock to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

CLOCK DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

COMMON MODE VOLTAGE (V_{CM}) is the d.c. potential present at both signal inputs to the ADC.

CONVERSION LATENCY is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated as:

Gain Error = Positive Full Scale Error − Offset Error

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is $V_{REF}/2^n$, where “n” is the ADC resolution in bits, which is 12 in the case of the ADC12DL066.

INTEGRAL NON LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dBFS.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC12L066 is guaranteed not to have any missing codes.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL SCALE ERROR is the difference between the input voltage ($V_{IN^+} - V_{IN^-}$) just causing a transition from negative full scale to the first code and its ideal value of 0.5 LSB.

OFFSET ERROR is the input voltage that will cause a transition from a code of 01 1111 1111 to a code of 10 0000 0000.

OUTPUT DELAY is the time delay after the rising edge of the clock before the data update is presented at the output pins.

PIPELINE DELAY (LATENCY) See Conversion Latency

POSITIVE FULL SCALE ERROR is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well the ADC rejects a change in the power supply voltage. For the ADC12L066, PSRR1 is the ratio of the change in Full-Scale Error that results from a change in the d.c. power supply voltage, expressed in dB. PSRR2 is a measure of how well an a.c. signal riding upon the power supply is rejected at the output.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dBc, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

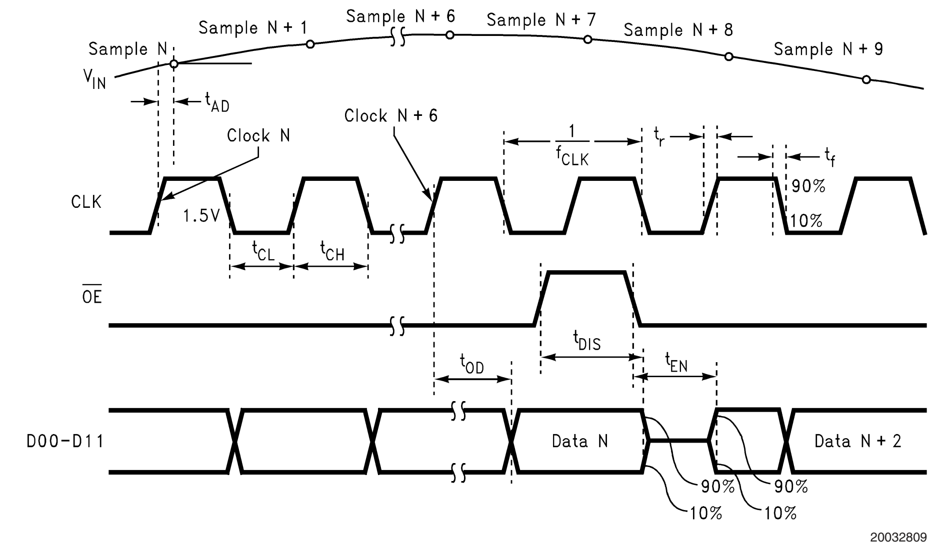
$$THD = 20 \times \log \sqrt{\frac{f_2^2 + \ldots + f_{10}^2}{f_1^2}}$$

where f_1 is the RMS power of the fundamental (output) frequency and f_2 through f_{10} are the RMS power in the first 9 harmonic frequencies.

SECOND HARMONIC DISTORTION (2ND HARM) is the difference expressed in dB, between the RMS power in the input frequency at the output and the power in its 2nd harmonic level at the output.

THIRD HARMONIC DISTORTION (3RD HARM) is the difference, expressed in dB, between the RMS power in the input frequency at the output and the power in its 3rd harmonic level at the output.

Timing Diagram



Output Timing

Transfer Characteristic

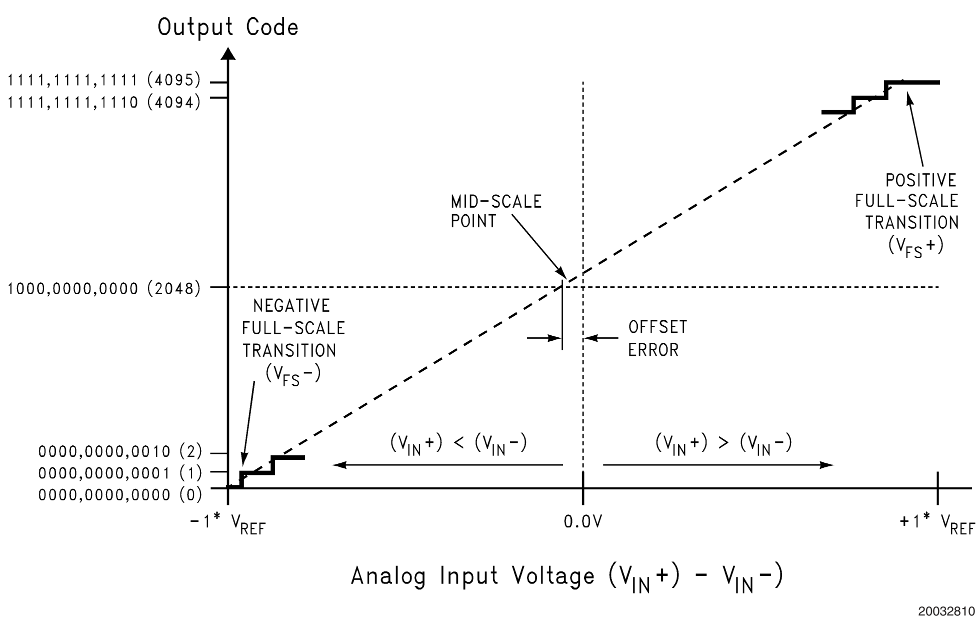
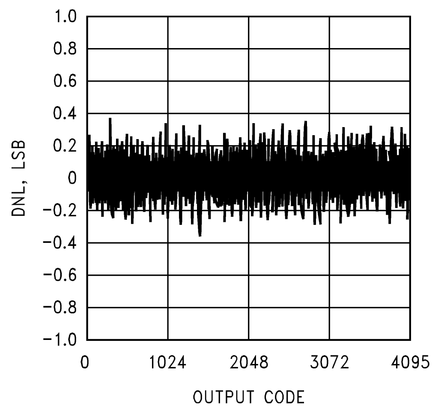


FIGURE 1. Transfer Characteristic

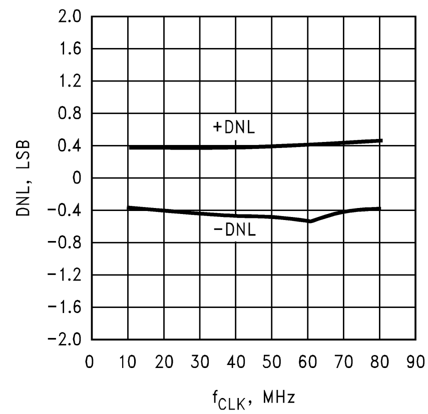
Typical Performance Characteristics $V_A = V_D = 3.3V$, $V_{DR} = 2.5V$, $f_{CLK} = 66$ MHz, $f_{IN} = 25$ MHz, $V_{REF} = 1.0V$, unless otherwise stated.

DNL



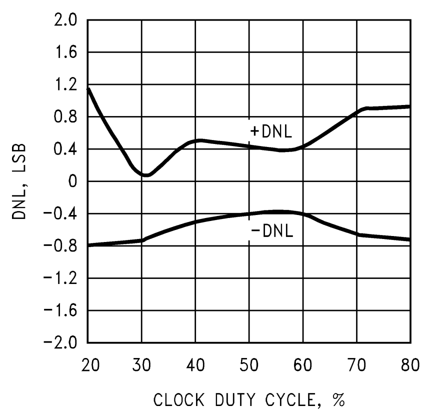
200328E6

DNL vs. f_{CLK}



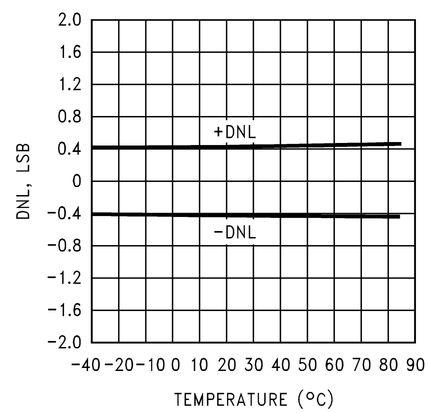
20032891

DNL vs. Clock Duty Cycle



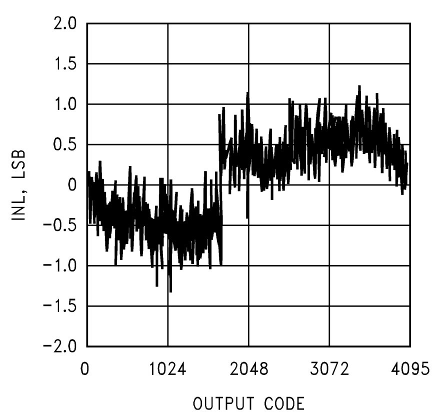
20032892

DNL vs. Temperature



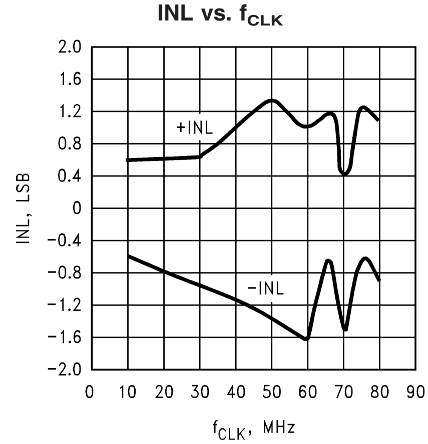
20032893

INL



200328E7

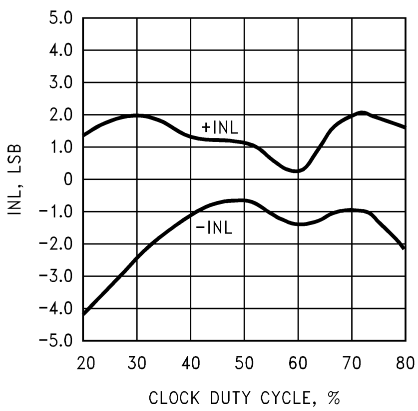
INL vs. f_{CLK}



20032894

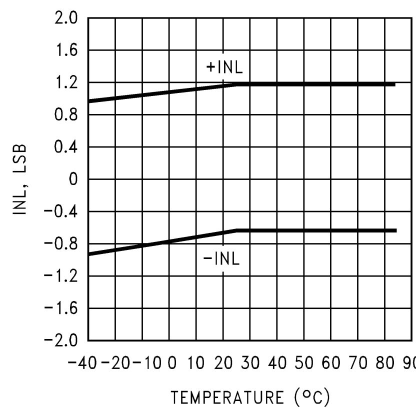
Typical Performance Characteristics $V_A = V_D = 3.3V$, $V_{DR} = 2.5V$, $f_{CLK} = 66$ MHz, $f_{IN} = 25$ MHz, $V_{REF} = 1.0V$, unless otherwise stated. (Continued)

INL vs. Clock Duty Cycle



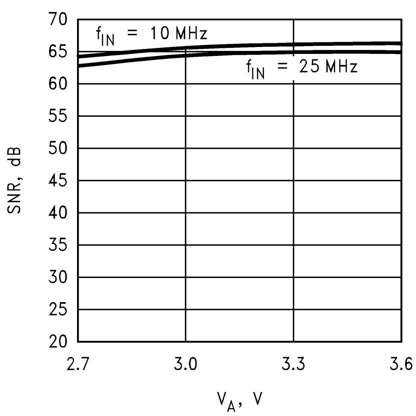
20032895

INL vs. Temperature



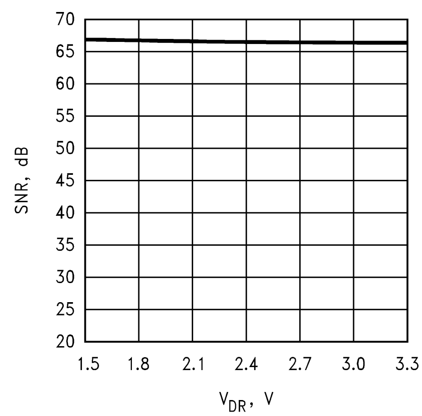
20032896

SNR vs. V_A



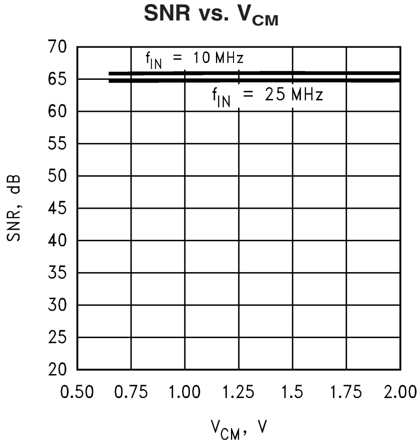
20032897

SNR vs. V_{DR}



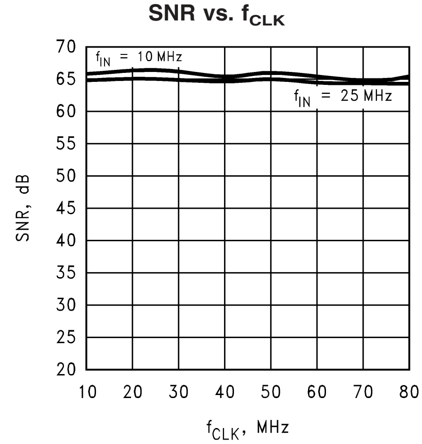
20032898

SNR vs. V_{CM}



200328B1

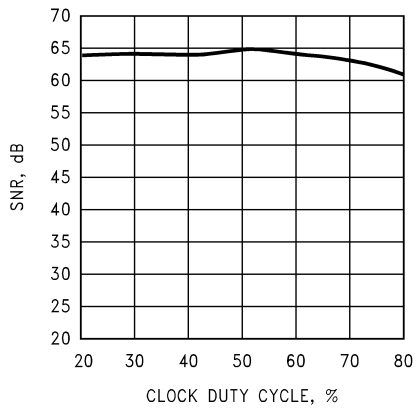
SNR vs. f_{CLK}



200328B2

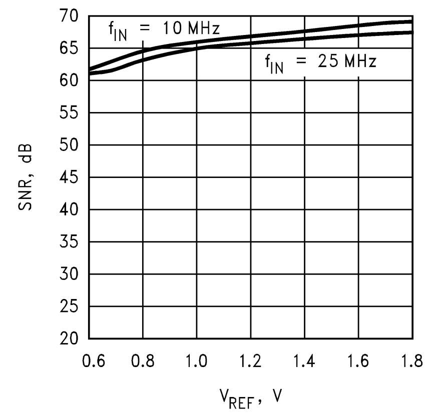
Typical Performance Characteristics $V_A = V_D = 3.3V$, $V_{DR} = 2.5V$, $f_{CLK} = 66$ MHz, $f_{IN} = 25$ MHz, $V_{REF} = 1.0V$, unless otherwise stated. (Continued)

SNR vs. Clock Duty Cycle



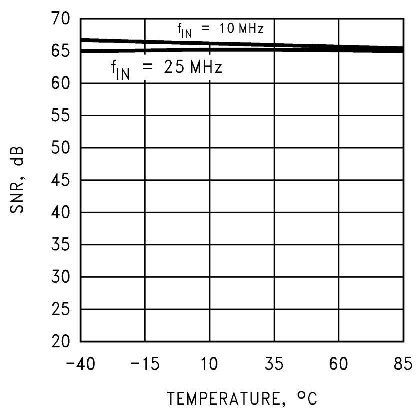
200328B3

SNR vs. V_{REF}



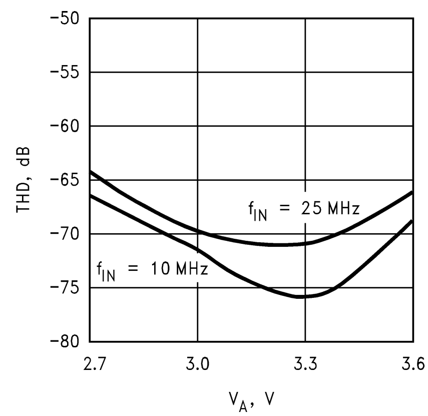
200328B4

SNR vs. Temperature



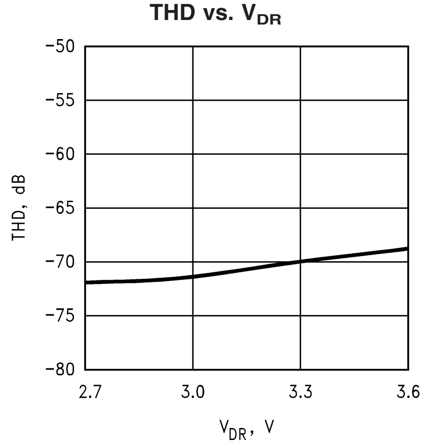
200328B5

THD vs. V_A



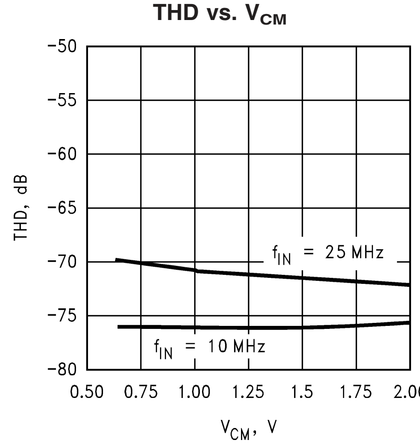
200328B6

THD vs. V_{DR}



200328B7

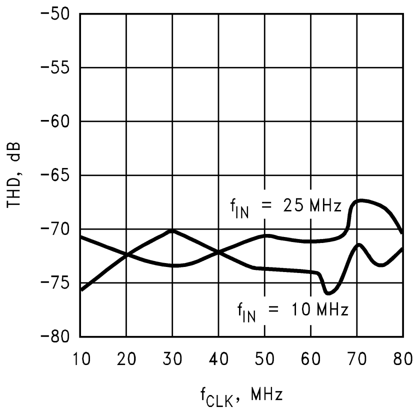
THD vs. V_{CM}



200328B8

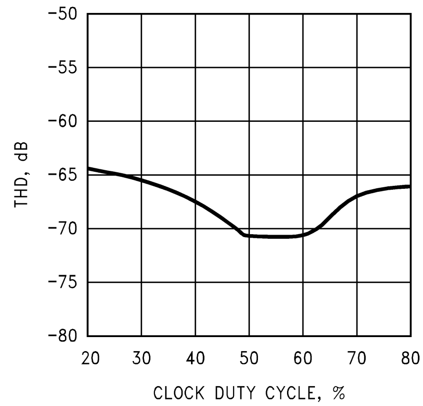
Typical Performance Characteristics $V_A = V_D = 3.3V$, $V_{DR} = 2.5V$, $f_{CLK} = 66$ MHz, $f_{IN} = 25$ MHz, $V_{REF} = 1.0V$, unless otherwise stated. (Continued)

THD vs. f_{CLK}



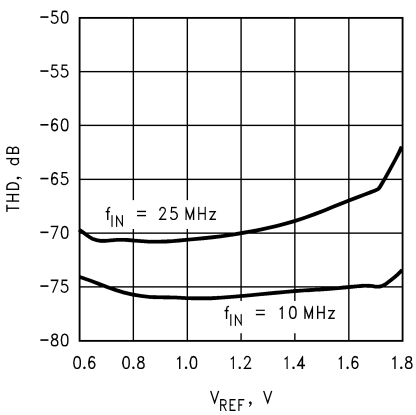
200328B9

THD vs. Clock Duty Cycle



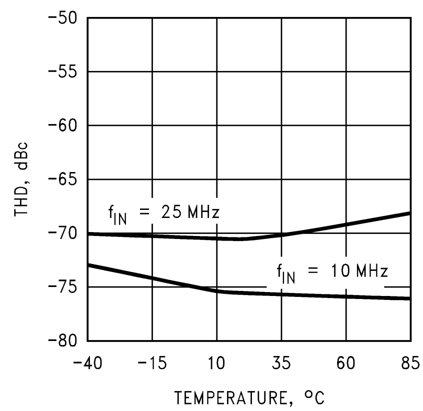
200328C1

THD vs. V_{REF}



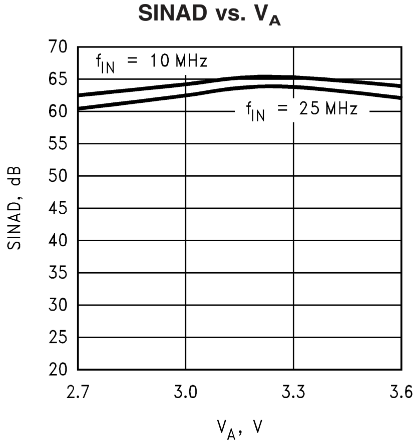
200328C2

THD vs. Temperature



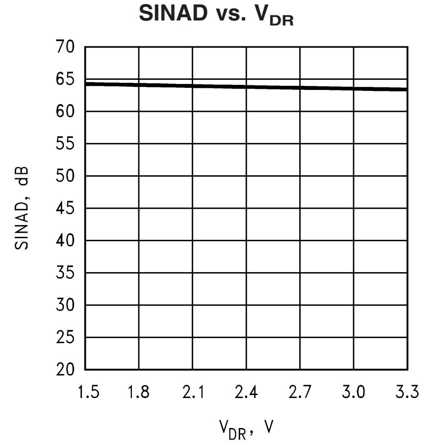
200328C3

SINAD vs. V_A



200328C4

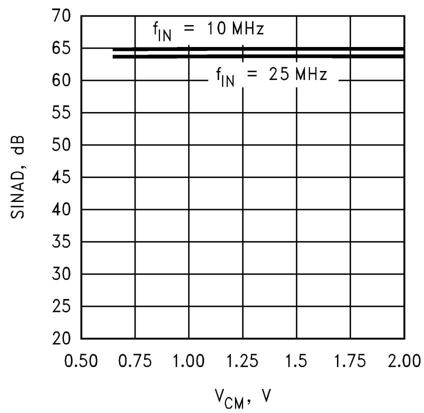
SINAD vs. V_{DR}



200328C5

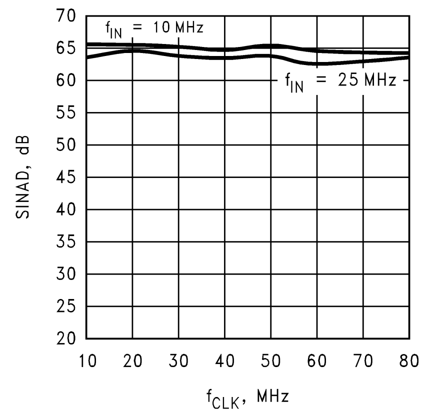
Typical Performance Characteristics $V_A = V_D = 3.3V$, $V_{DR} = 2.5V$, $f_{CLK} = 66$ MHz, $f_{IN} = 25$ MHz, $V_{REF} = 1.0V$, unless otherwise stated. (Continued)

SINAD vs. V_{CM}



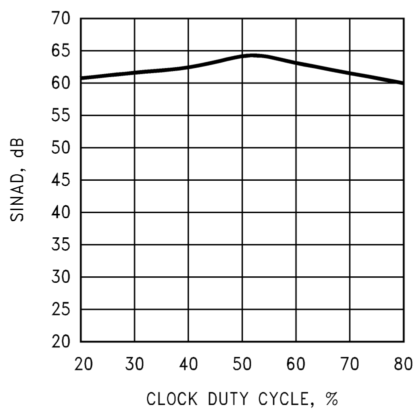
200328C6

SINAD vs. f_{CLK}



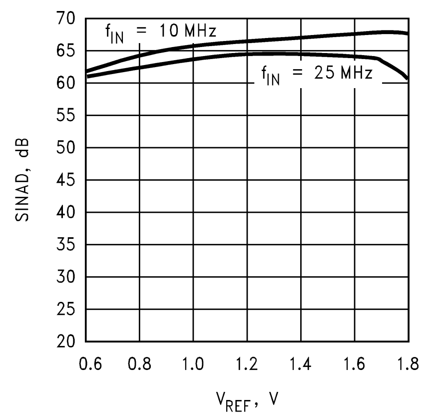
200328C7

SINAD vs. Clock Duty Cycle



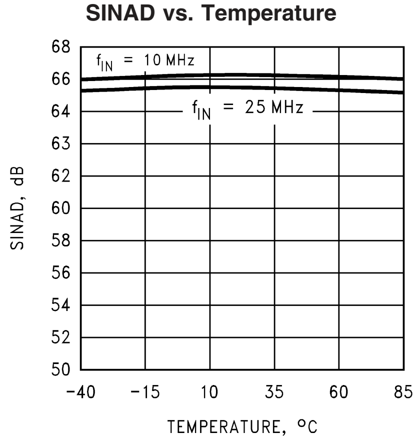
200328C8

SINAD vs. V_{REF}



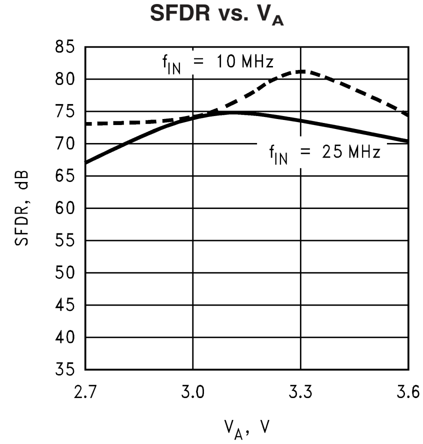
200328C9

SINAD vs. Temperature



200328D1

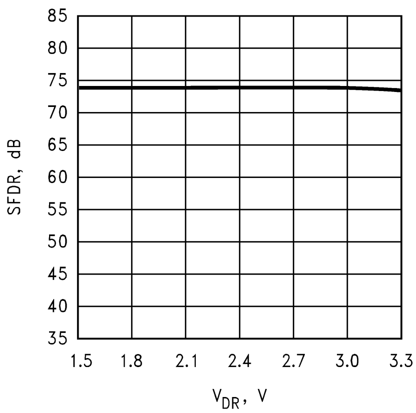
SFDR vs. V_A



200328D2

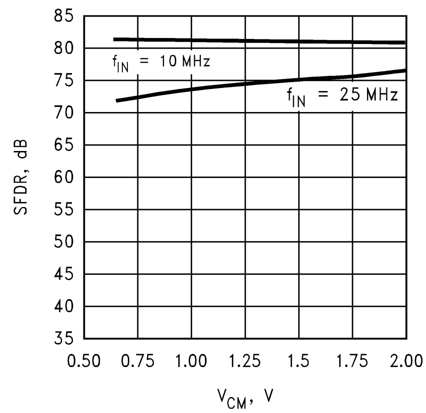
Typical Performance Characteristics $V_A = V_D = 3.3V$, $V_{DR} = 2.5V$, $f_{CLK} = 66$ MHz, $f_{IN} = 25$ MHz, $V_{REF} = 1.0V$, unless otherwise stated. (Continued)

SFDR vs. V_{DR}



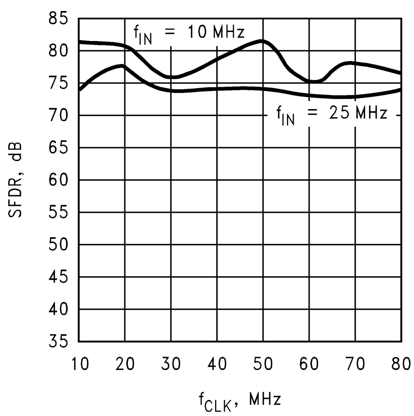
200328D3

SFDR vs. V_{CM}



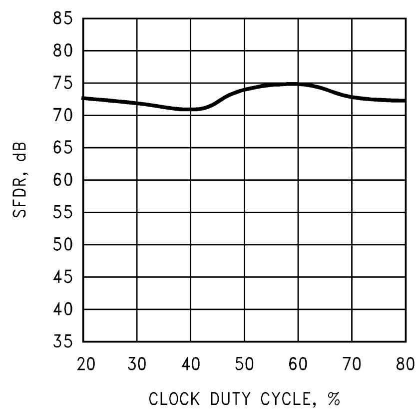
200328D4

SFDR vs. f_{CLK}



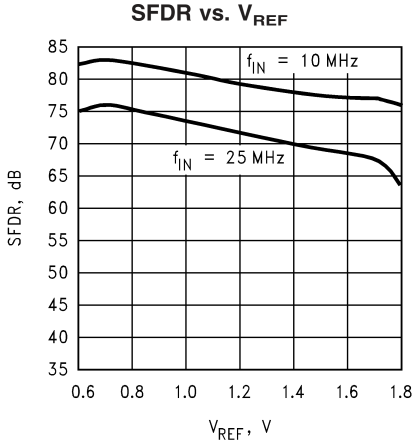
200328D5

SFDR vs. Clock Duty Cycle



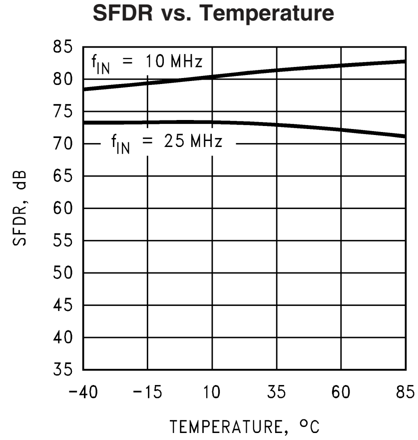
200328D6

SFDR vs. V_{REF}



200328D7

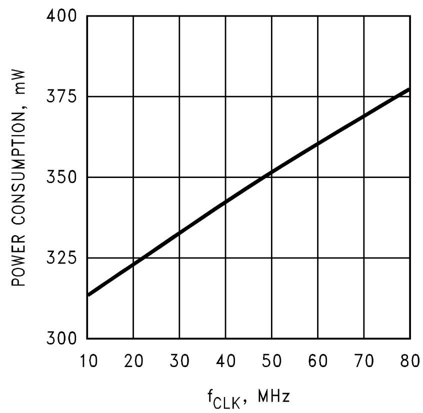
SFDR vs. Temperature



200328D8

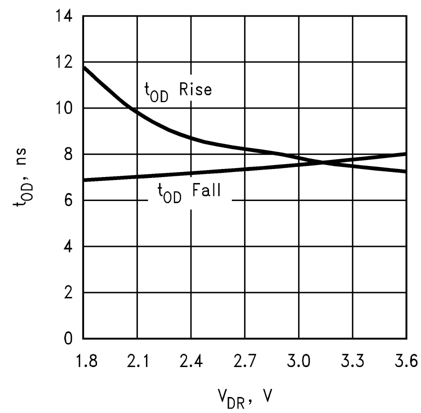
Typical Performance Characteristics $V_A = V_D = 3.3V$, $V_{DR} = 2.5V$, $f_{CLK} = 66$ MHz, $f_{IN} = 25$ MHz, $V_{REF} = 1.0V$, unless otherwise stated. (Continued)

Power Consumption vs. f_{CLK}



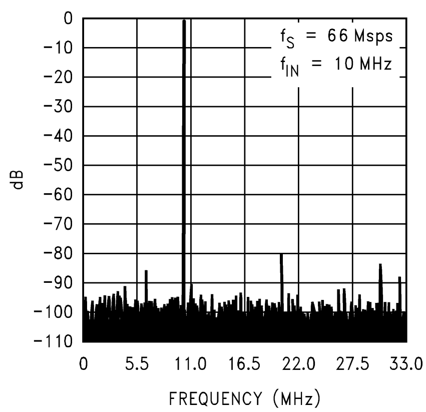
200328D9

t_{OD} vs. V_{DR}



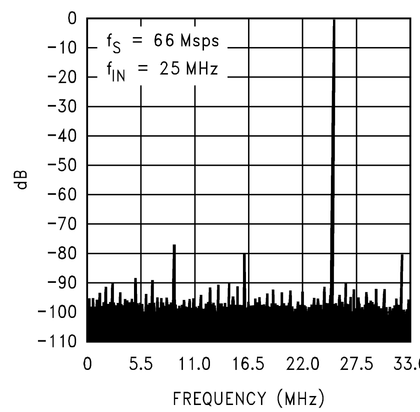
200328E1

Spectral Response @ 10 MHz Input



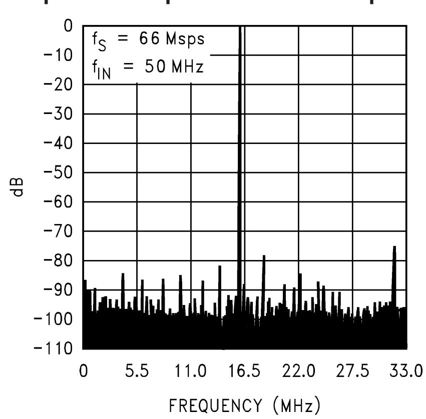
200328E4

Spectral Response @ 25 MHz Input



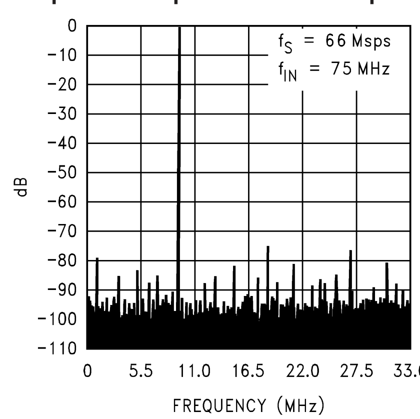
200328E8

Spectral Response @ 50 MHz Input



200328E9

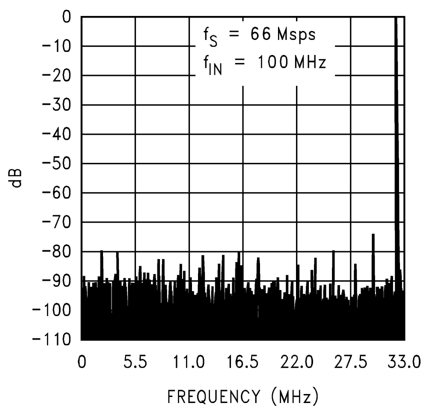
Spectral Response @ 75MHz Input



200328J0

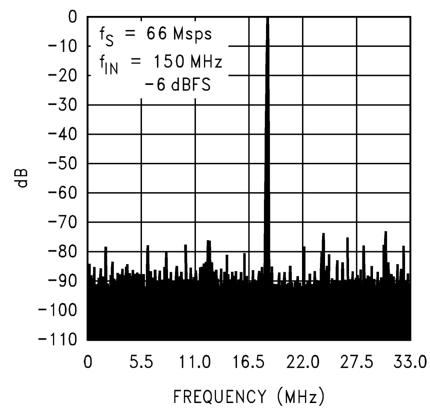
Typical Performance Characteristics $V_A = V_D = 3.3V$, $V_{DR} = 2.5V$, $f_{CLK} = 66$ MHz, $f_{IN} = 25$ MHz, $V_{REF} = 1.0V$, unless otherwise stated. (Continued)

Spectral Response @ 100 MHz Input



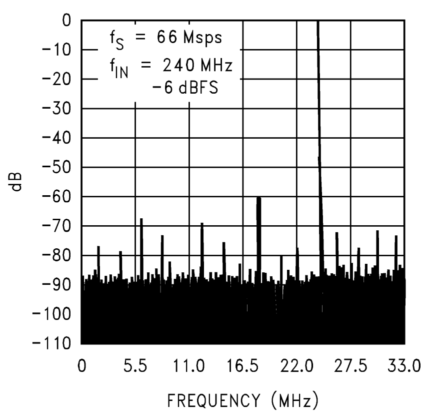
200328J1

Spectral Response @ 150 MHz Input



200328J2

Spectral Response @ 240 MHz Input



200328E5

Functional Description

Operating on a single +3.3V supply, the ADC12L066 uses a pipeline architecture and has error correction circuitry to help ensure maximum performance.

Differential analog input signals are digitized to 12 bits. Each analog input signal should have a peak-to-peak voltage equal to the input reference voltage, V_{REF}, be centered around a common mode voltage, V_{CM}, and be 180˚ out of phase with each other. *Table 1. Input to Output Relationship–Differential Input* and *Table 2. Input to Output Relationship–Single-Ended Input* indicate the input to output relationship of the ADC12L066. Biasing one input to V_{CM} and driving the other input with its full range signal results in a 6 dB reduction of the output range, limiting it to the range of ¼ to ¾ of the minimum output range obtainable if both inputs were driven with complimentary signals. Section 1.3 explains how to avoid this signal reduction.

TABLE 1. Input to Output Relationship–Differential Input

V_{IN^+}	V_{IN^-}	Output
$V_{CM} - V_{REF}/2$	$V_{CM} + V_{REF}/2$	0000 0000 0000
$V_{CM} - V_{REF}/4$	$V_{CM} + V_{REF}/4$	0100 0000 0000
V_{CM}	V_{CM}	1000 0000 0000
$V_{CM} + V_{REF}/4$	$V_{CM} - V_{REF}/4$	1100 0000 0000
$V_{CM} + V_{REF}/2$	$V_{CM} - V_{REF}/2$	1111 1111 1111

TABLE 2. Input to Output Relationship–Single-Ended Input

V_{IN^+}	V_{IN^-}	Output
$V_{CM} - V_{REF}$	V_{CM}	0000 0000 0000
$V_{CM} - V_{REF}/2$	V_{CM}	0100 0000 0000
V_{CM}	V_{CM}	1000 0000 0000
$V_{CM} + V_{REF}/2$	V_{CM}	1100 0000 0000
$V_{CM} + V_{REF}$	V_{CM}	1111 1111 1111

The output word rate is the same as the clock frequency, which can be between 1 MSPS and 80 MSPS (typical). The analog input voltage is acquired at the rising edge of the clock and the digital data for that sample is delayed by the pipeline for 6 clock cycles.

A logic high on the power down (PD) pin reduces the converter power consumption to 50 mW.

Applications Information

1.0 OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC12L066:

$3.0\text{ V} \leq V_A \leq 3.6\text{V}$

$V_D = V_A$

$1.8\text{V} \leq V_{DR} \leq V_D$

$1\text{ MHz} \leq f_{CLK} \leq 80\text{ MHz}$

$0.8\text{V} \leq V_{REF} \leq 1.5\text{V}$

$0.5\text{V} \leq V_{CM} \leq 1.5\text{V}$

1.1 ANALOG INPUTS

The ADC12L066 has two analog signal inputs, $V_{IN}+$ and V_{IN-}. These two pins form a differential input pair. There is one reference input pin, V_{REF}.

1.2 Reference Pins

The ADC12L066 is designed to operate with a 1.0V reference, but performs well with reference voltages in the range of 0.8V to 1.5V. Lower reference voltages will decrease the signal-to-noise ratio (SNR) of the ADC12L066. Increasing the reference voltage (and the input signal swing) beyond 1.5V may degrade THD for a full-scale input, especially at higher input frequencies. It is important that all grounds associated with the reference voltage and the input signal make connection to the analog ground plane at a single, quiet point in that plane to minimize the effects of noise currents in the ground path.

The ADC12L066 will perform well with reference voltages up to 1.5V for full-scale input frequencies up to 10 MHz. However, more headroom is needed as the input frequency increases, so the maximum reference voltage (and input swing) will decrease for higher full-scale input frequencies.

The three Reference Bypass Pins (V_{RP}, V_{RM} and V_{RN}) are made available for bypass purposes only. These pins should each be bypassed to ground with a 0.1 µF capacitor. Smaller capacitor values will allow faster recovery from the power down mode, but may result in degraded noise performance. DO NOT LOAD these pins. Loading any of these pins may result in performance degradation.

The nominal voltages for the reference bypass pins are as follows:

$V_{RM} = V_A / 2$

$V_{RP} = V_{RM} + V_{REF} / 2$

$V_{RN} = V_{RM} - V_{REF} / 2$

The V_{RM} pin may be used as a common mode voltage source (V_{CM}) for the analog input pins as long as no d.c. current is drawn from it. However, because the voltage at this pin is half that of the V_A supply pin, using these pins for a common mode source will result in reduced input headroom (the difference between the V_A supply voltage and the peak signal voltage at either analog input) and the possibility of reduced THD and SFDR performance. For this reason, it is recommended that V_A always exceed V_{REF} by at least 2 Volts. For high input frequencies it may be necessary to increase this headroom to maintain THD and SFDR performance. Alternatively, use V_{RN} for a V_{CM} source.

1.3 SIGNAL INPUTS

The signal inputs are $V_{IN}+$ and $V_{IN}-$. The input signal, V_{IN}, is defined as

$$V_{IN} = (V_{IN^+}) - (V_{IN}-)$$

Figure 2 shows the expected input signal range.

Note that the nominal input common mode voltage is V_{REF} and the nominal input signals each run between the limits of $V_{REF}/2$ and $3V_{REF}/2$. The Peaks of the input signals should never exceed the voltage described as

$$\text{Peak Input Voltage} = V_A - 0.8$$

to maintain dynamic performance.

The ADC12L066 performs best with a differential input with each input centered around a common mode voltage, V_{CM} (minimum of 0.5V). The peak-to-peak voltage swing at both $V_{IN}+$ and $V_{IN}-$ should each not exceed the value of the reference voltage or the output data will be clipped.

Applications Information (Continued)

The two input signals should be exactly 180˚ out of phase from each other and of the same amplitude. For single frequency (sine wave) inputs, angular errors result in a reduction of the effective full scale input. For a complex waveform, however, angular errors will result in distortion.

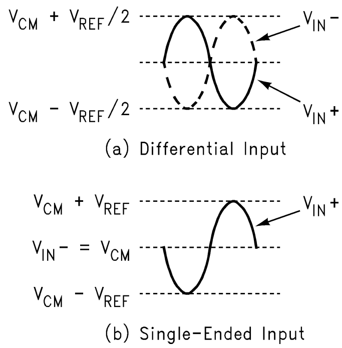


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FIGURE 2. Expected Input Signal Range

For angular deviations of up to 10 degrees from these two signals being 180 out of phase with each other, the full scale error in LSB can be described as approximately

$$E_{FS} = dev^{1.79}$$

Where dev is the angular difference between the two signals having a 180˚ relative phase relationship to each other (see *Figure 3*). Drive the analog inputs with a source impedance less than 100Ω.

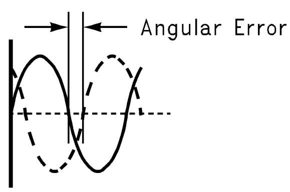

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FIGURE 3. Angular Errors Between the Two Input Signals Will Reduce the Output Level or Cause Distortion

For differential operation, each analog input pin of the differential pair should have a peak-to-peak voltage equal to the input reference voltage, V_{REF}, and be centered around V_{CM}.

1.3.1 Single-Ended Input Operation

Single-ended performance is inferior to that with differential input signals, so single-ended operation is not recommended, However, if single-ended operation is required and the resulting performance degradation is acceptable, one of the analog inputs should be connected to the d.c. mid point voltage of the driven input. The peak-to-peak differential input signal should be twice the reference voltage to maximize SNR and SINAD performance (*Figure 2*b).

For example, set V_{REF} to 0.5V, bias $V_{IN}-$ to 1.0V and drive $V_{IN}+$ with a signal range of 0.5V to 1.5V.

Because very large input signal swings can degrade distortion performance, better performance with a single-ended input can be obtained by reducing the reference voltage while maintaining a full-range output. *Table 1. Input to Output Relationship–Differential Input* and *Table 2. Input to Output Relationship–Single-Ended Input* indicate the input to output relationship of the ADC12L066.

1.3.2 Driving the Analog Inputs

The $V_{IN}+$ and the $V_{IN}-$ inputs of the ADC12L066 consist of an analog switch followed by a switched-capacitor amplifier. The capacitance seen at the analog input pins changes with the clock level, appearing as 8 pF when the clock is low, and 7 pF when the clock is high.

As the internal sampling switch opens and closes, current pulses occur at the analog input pins, resulting in voltage spikes at the signal input pins. As a driving amplifier attempts to counteract these voltage spikes, a damped oscillation may appear at the ADC analog input. The best amplifiers for driving the ADC12L066 input pins must be able to react to these spikes and settle before the switch opens and another sample is taken. The LMH6702 LMH6628, LMH6622 and the LMH6655 are good amplifiers for driving the ADC12L066.

To help isolate the pulses at the ADC input from the amplifier output, use RCs at the inputs, as can be seen in *Figure 5* and *Figure 6*. These components should be placed close to the ADC inputs because the input pins of the ADC is the most sensitive part of the system and this is the last opportunity to filter that input.

For Nyquist applications the RC pole should be at the ADC sample rate. The ADC input capacitance in the sample mode should be considered with setting the RC pole. Setting the pole in this manner will provide best SINAD performance.

To obtain best SNR performance, leave the RC values as calculated. To obtain best SINAD and ENOB performance, reduce the RC time constant until SNR and THD are numerically equal to each other. To obtain best distortion and SFDR performance, eliminate the RC altogether.

For undersampling applications, the RC pole should be set at about 1.5 to 2 times the maximum input frequency for narrow band applications. For wide band applications, the RC pole should be set at about 1.5 times the maximum input frequency to maintain a linear delay response.

A single-ended to differential conversion circuit is shown in *Figure 5* and *Table 3. Resistor values for Circuit of NS4771* gives resistor values for that circuit to provide input signals in a range of 1.0V ±0.5V at each of the differential input pins of the ADC12L066.

TABLE 3. Resistor values for Circuit of *Figure 5*

SIGNAL RANGE	R1	R2	R3	R4	R5, R6
0 - 0.25V	open	0Ω	124Ω	1500Ω	1000Ω
0 - 0.5V	0Ω	openΩ	499Ω	1500Ω	499Ω
±0.25V	100Ω	698Ω	100Ω	698Ω	499Ω

1.3.3 Input Common Mode Voltage

The input common mode voltage, V_{CM}, should be in the range of 0.5V to 1.5V and be of a value such that the peak excursions of the analog signal does not go more negative than ground or more positive than 0.8 Volts below the V_A supply voltage. The nominal V_{CM} should generally be about 1.0V, but V_{RM} or V_{RN} can be used as a V_{CM} source as long as no d.c. current is drawn from either of these pins.

Applications Information (Continued)

2.0 DIGITAL INPUTS

Digital inputs are TTL/CMOS compatible and consist of CLK, $\overline{OE}$ and PD.

2.1 CLK

The **CLK** signal controls the timing of the sampling process. Drive the clock input with a stable, low jitter clock signal in the range of 1 MHz to 80 MHz with rise and fall times of less than 2 ns. The trace carrying the clock signal should be as short as possible and should not cross any other signal line, analog or digital, not even at 90˚.

The **CLK** signal also drives an internal state machine. If the **CLK** is interrupted, or its frequency is too low, the charge on internal capacitors can dissipate to the point where the accuracy of the output data will degrade. This is what limits the lowest sample rate to 1 MSPS.

The duty cycle of the clock signal can affect the performance of any A/D Converter. Because achieving a precise duty cycle is difficult, the ADC12L066 is designed to maintain performance over a range of duty cycles. While it is specified and performance is guaranteed with a 50% clock duty cycle, performance is typically maintained over a clock duty cycle range of 40% to 60%.

The clock line should be series terminated at the clock source in the characteristic impedance of that line if the clock line is longer than

$$\frac{t_r}{6 \times t_{prop}}$$

where t_r is the clock rise time and t_{prop} is the propagation rate of the signal along the trace. For a typical board of FR-4 material, t_{PROP} is about 150 ps/in, or 60 ps/cm. The **CLOCK** pin may need to be a.c. terminated with a series RC such that the resistor value is equal to the characteristic impedance of the clock line and the capacitor value is

$$C \geq \frac{1.2 \times 10^{-9} \times l}{Z_o}$$

where "I" is the line length in inches and Z_o is the characteristic impedance of the clock line. This termination should be located as close as possible to, but within one centimeter of, the ADC12L066 clock pin as shown in *Figure 6*. It should also be located beyond the ADC clock pin as seen from the clock source.

Take care to maintain a constant clock line impedance throughout the length of the line and to properly terminate the source end of the line with its characteristic impedance. Refer to Application Note AN-905 for information on setting characteristic impedance.

2.2 $\overline{OE}$

The $\overline{OE}$ pin, when high, puts the output pins into a high impedance state. When this pin is low the outputs are in the active state. The ADC12L066 will continue to convert whether this pin is high or low, but the output can not be read while the $\overline{OE}$ pin is high.

Since ADC noise increases with increased output capacitance at the digital output pins, do use the TRI-STATE outputs of the ADC12L066 to drive a bus. Rather, each output pin should be located close to and drive a single digital input pin. To further reduce ADC noise, a 100 Ω resistor in series with each ADC digital output pin, located close to their respective pins, should be added to the circuit. See Section 3.0.

2.3 PD

The PD pin, when high, holds the ADC12L066 in a power-down mode to conserve power when the converter is not being used. The power consumption in this state is 50 mW with a 66 MHz clock and 30 mW if the clock is stopped. The output data pins are undefined in this mode. The data in the pipeline is corrupted while in the power down mode.

The Power Down Mode Exit Cycle time is determined by the value of the capacitors on pins 30, 31 and 32 and is about 300 ns with the recommended 0.1 µF on these pins. These capacitors loose their charge in the Power Down mode and must be recharged by on-chip circuitry before conversions can be accurate. Smaller capacitor values allow faster recovery from the power down mode, but can result in a reduction in SNR, SINAD and ENOB performance.

3.0 OUTPUTS

The ADC12L066 has 12 TTL/CMOS compatible Data Output pins. The offset binary data is present at these outputs while the $\overline{OE}$ and PD pins are low. While the t_{OD} time provides information about output timing, a simple way to capture a valid output is to latch the data on the *rising edge* of the conversion clock (pin 10).

Be very careful when driving a high capacitance bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through V_{DR} and DR GND. These large charging current spikes can cause on-chip ground noise and couple into the analog circuitry, degrading dynamic performance. Adequate bypassing, limiting output capacitance and careful attention to the ground plane will reduce this problem. Additionally, bus capacitance beyond the specified 15 pF/pin will cause t_{OD} to increase, making it difficult to properly latch the ADC output data. The result could be an apparent reduction in dynamic performance.

To minimize noise due to output switching, minimize the load currents at the digital outputs. This can be done by connecting buffers between the ADC outputs and any other circuitry (74ACQ541, for example). Only one driven input should be connected to each output pin. Additionally, inserting series resistors of 100Ω at the digital outputs, close to the ADC pins, will isolate the outputs from trace and other circuit capacitances and limit the output currents, which could otherwise result in performance degradation. See *Figure 4*.

While the ADC12L066 will operate with V_{DR} voltages down to 1.8V, t_{OD} increases with reduced V_{DR}. Be careful of external timing when using reduced V_{DR}.

Applications Information (Continued)

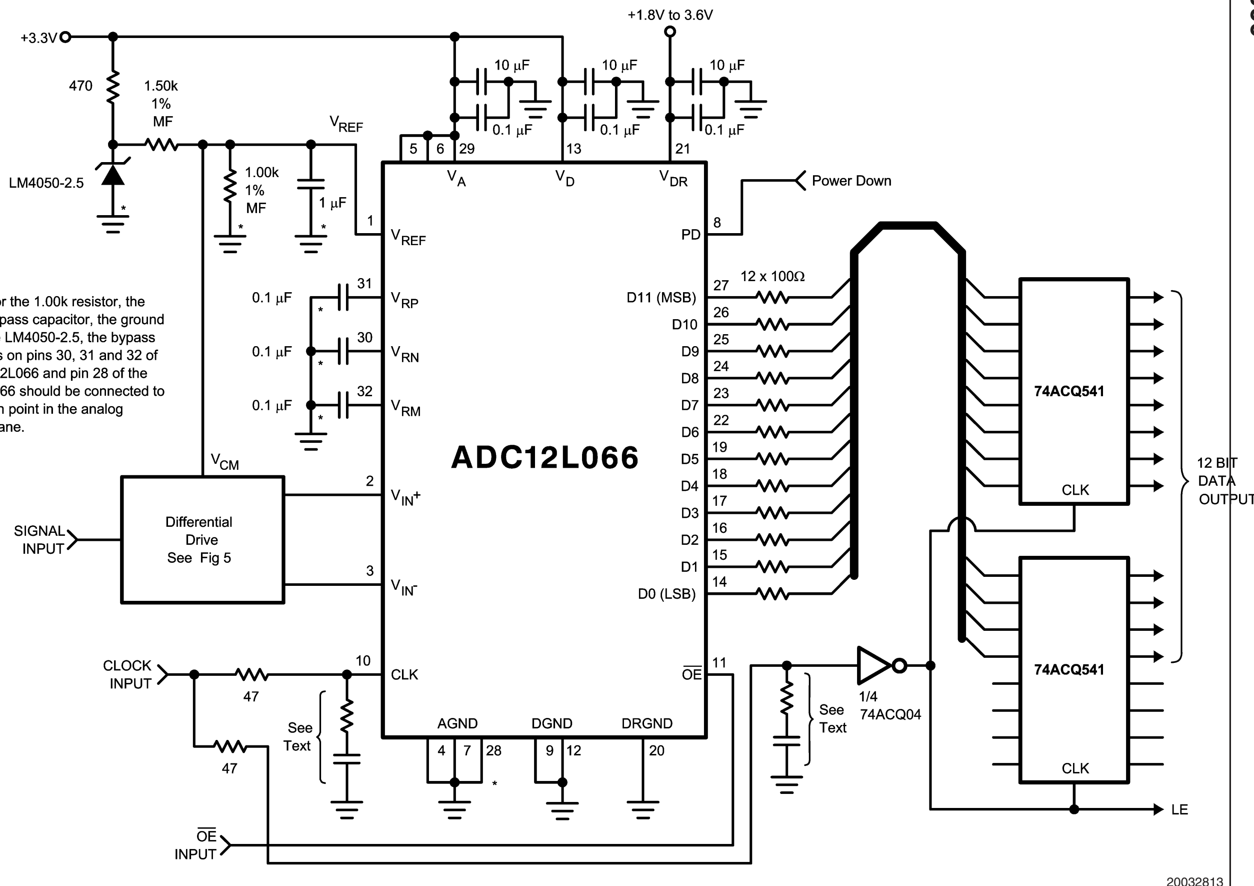


FIGURE 4. Simple Application Circuit with Single-Ended to Differential Buffer

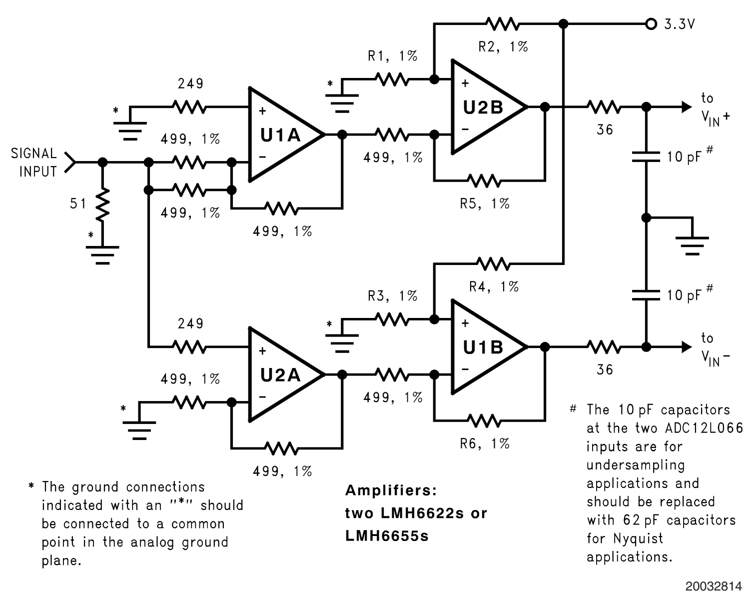


FIGURE 5. Differential Drive Circuit of *Figure 4*

Applications Information (Continued)

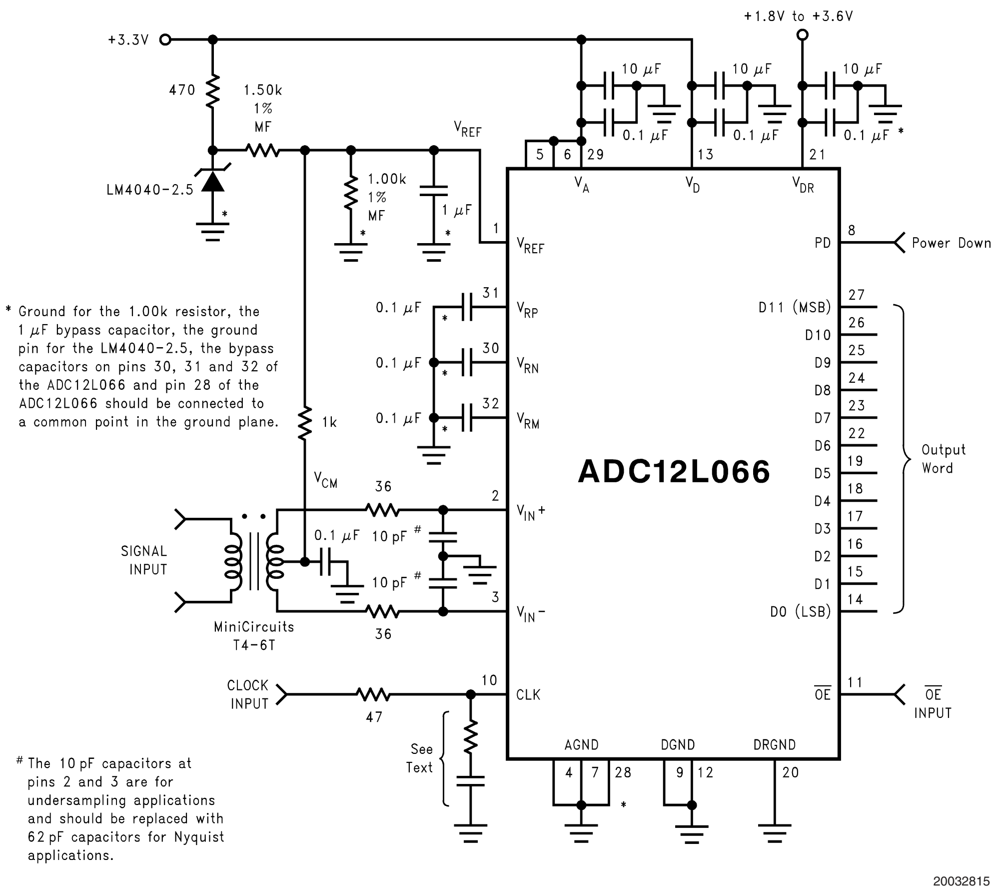


FIGURE 6. Driving the Signal Inputs with a Transformer

4.0 POWER SUPPLY CONSIDERATIONS

The power supply pins should be bypassed with a 10 µF capacitor and with a 0.1 µF ceramic chip capacitor within a centimeter of each power pin. Leadless chip capacitors are preferred because they have low series inductance.

As is the case with all high-speed converters, the ADC12L066 is sensitive to power supply noise. Accordingly, the noise on the analog supply pin should be kept below 100 mV_{P-P}.

No pin should ever have a voltage on it that is in excess of the supply voltages, not even on a transient basis. Be especially careful of this during turn on and turn off of power.

The V_{DR} pin provides power for the output drivers and may be operated from a supply in the range of 1.8V to V_D. This can simplify interfacing to devices and systems operating with supplies less than V_D. Note, however, that t_{OD} increases with reduced V_{DR}. **DO NOT operate the V_{DR} pin at a voltage higher than V_D.**

5.0 LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. Maintaining separate analog and digital areas of the board, with the ADC12L066 between these areas, is required to achieve specified performance.

The ground return for the data outputs (DR GND) carries the ground current for the output drivers. The output current can exhibit high transients that could add noise to the conversion process. To prevent this from happening, the DR GND pins should NOT be connected to system ground in close proximity to any of the ADC12L066's other ground pins.

Capacitive coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry, and to keep the clock line as short as possible.

Digital circuits create substantial supply and ground current transients. The logic noise thus generated could have significant impact upon system noise performance. The best logic family to use in systems with A/D converters is one which employs non-saturating transistor designs, or has low noise characteristics, such as the 74LS, 74HC(T) and 74AC(T)Q families. The worst noise generators are logic families that draw the largest supply current transients during clock or signal edges, like the 74F and the 74AC(T) families.

The effects of the noise generated from the ADC output switching can be minimized through the use of 100Ω resistors in series with each data output line. Locate these resistors as close to the ADC output pins as possible.

Since digital switching transients are composed largely of high frequency components, total ground plane copper

Applications Information (Continued)

weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane volume.

Generally, analog and digital lines should cross each other at 90˚ to avoid crosstalk. To maximize accuracy in high speed, high resolution systems, however, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. Even the generally accepted 90˚ crossing should be avoided with the clock line as even a little coupling can cause problems at high frequencies. This is because other lines can introduce jitter into the clock line, which can lead to degradation of SNR. Also, the high speed clock can introduce noise into the analog chain.

Best performance at high frequencies and at high resolution is obtained with a straight signal path. That is, the signal path through all components should form a straight line wherever possible.

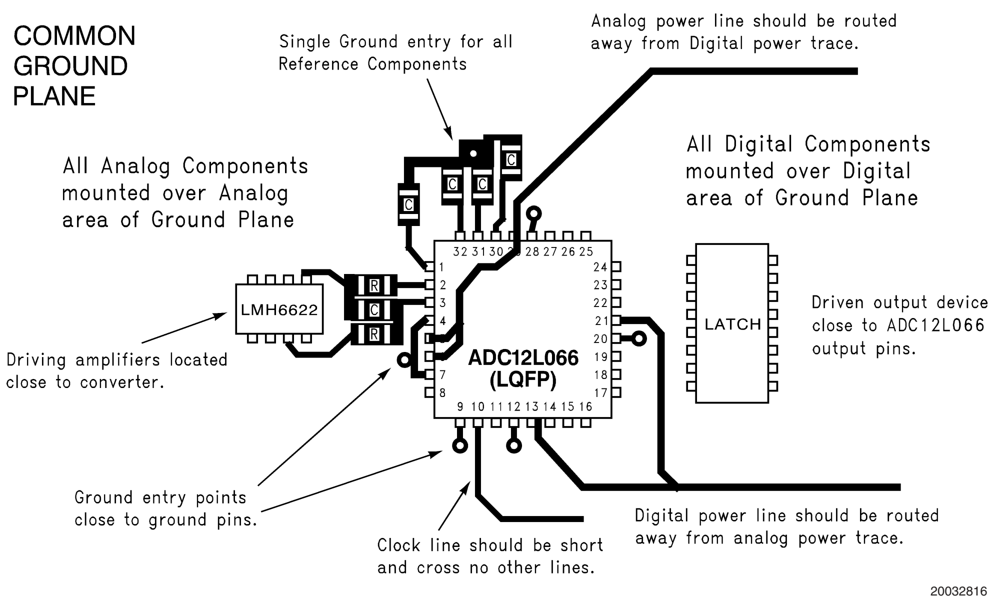


FIGURE 7. Example of a Suitable Layout

Be especially careful with the layout of inductors. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors should *not* be placed side by side, even with just a small part of their bodies beside each other.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane.

Figure 7 gives an example of a suitable layout. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed in the analog area of the board. All digital circuitry and I/O lines should be placed in the digital area of the board. The ADC12L066 should be between these two areas. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the ground plane at a single, quiet point. All ground connections should have a low inductance path to ground.

6.0 DYNAMIC PERFORMANCE

To achieve the best dynamic performance, the clock source driving the CLK input must be free of jitter. Isolate the ADC clock from any digital circuitry with buffers, as with the clock tree shown in *Figure 8*.

As mentioned in Section 5.0, it is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal, which can lead to reduced SNR performance, and the clock can introduce noise into other lines. Even lines with 90˚ crossings have capacitive coupling, so try to avoid even these 90˚ crossings of the clock line.

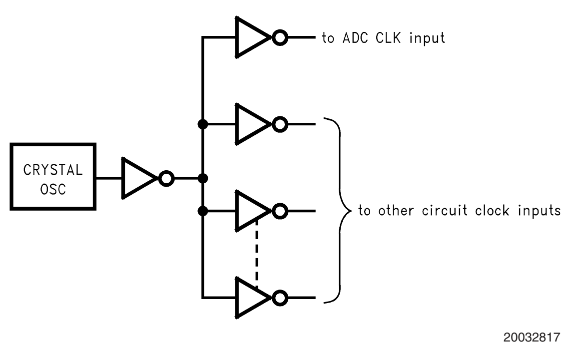


FIGURE 8. Isolating the ADC Clock from other Circuitry with a Clock Tree

7.0 COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 100 mV beyond the supply rails (more than 100 mV below the ground pins or 100 mV above the supply pins). Exceeding these limits on even a transient basis may

Applications Information (Continued)

cause faulty or erratic operation. It is not uncommon for high speed digital components (e.g., 74F and 74AC devices) to exhibit overshoot or undershoot that goes above the power supply or below ground. A resistor of about 50Ω to 100Ω in series with any offending digital input, close to the signal source, will eliminate the problem.

Do not allow input voltages to exceed the supply voltage, even on a transient basis. Not even during power up or power down.

Be careful not to overdrive the inputs of the ADC12L066 with a device that is powered from supplies outside the range of the ADC12L066 supply. Such practice may lead to conversion inaccuracies and even to device damage.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through V_{DR} and DR GND. These large charging current spikes can couple into the analog circuitry, degrading dynamic performance. Adequate bypassing and maintaining separate analog and digital areas on the pc board will reduce this problem.

Additionally, bus capacitance beyond the specified 15 pF/pin will cause t_{OD} to increase, making it difficult to properly latch the ADC output data. The result could, again, be a reduction in dynamic performance.

The digital data outputs should be buffered (with 74ACQ541, for example). Dynamic performance can also be improved by adding series resistors at each digital output, close to the ADC12L066, which reduces the energy coupled back into the converter output pins by limiting the output current. A reasonable value for these resistors is 100Ω.

Using an inadequate amplifier to drive the analog input. As explained in Section 1.3, the capacitance seen at the input alternates between 8 pF and 7 pF, depending upon the phase of the clock. This dynamic load is more difficult to drive than is a fixed capacitance.

If the amplifier exhibits overshoot, ringing, or any evidence of instability, even at a very low level, it will degrade performance. A small series resistor at each amplifier output and a capacitor across the analog inputs (as shown in *Figures 5, 6*) will improve performance. The LMH6702, LMH6628, LMH6622 and LMH6655 have been successfully used to drive the analog inputs of the ADC12L066.

Also, it is important that the signals at the two inputs have exactly the same amplitude and be exactly 180° out of phase with each other. Board layout, especially equality of the length of the two traces to the input pins, will affect the effective phase between these two signals. Remember that an operational amplifier operated in the non-inverting configuration will exhibit more time delay than will the same device operating in the inverting configuration.

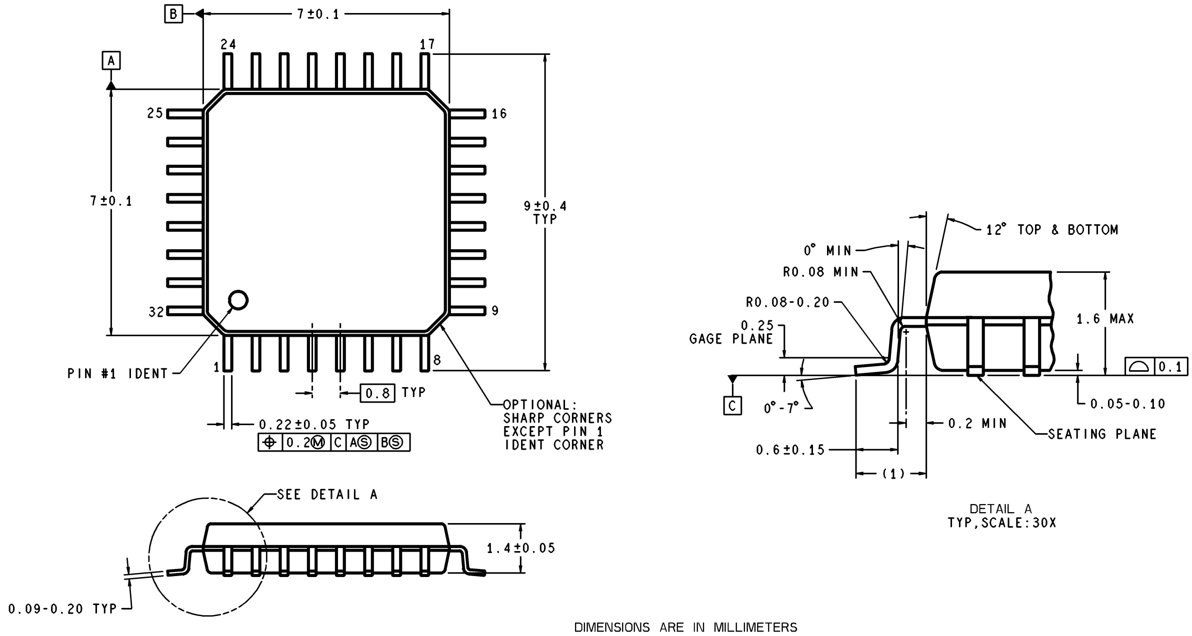
Operating with the reference pins outside of the specified range. As mentioned in Section 1.2, V_{REF} should be in the range of

$$0.8V \leq V_{REF} \leq 1.5V$$

Operating outside of these limits could lead to performance degradation.

Using a clock source with excessive jitter, using excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR and SINAD performance.

Physical Dimensions inches (millimeters) unless otherwise noted



VBE32A (Rev E)

32-Lead LQFP Package
Ordering Number ADC12L066CIVY
NS Package Number VBE32A

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