



# IRFBC30

## N - CHANNEL 600V - 1.8 $\Omega$ - 3.6A - TO-220 PowerMESH™ II MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
IRFBC30	600 V	< 2.2 $\Omega$	3.6 A

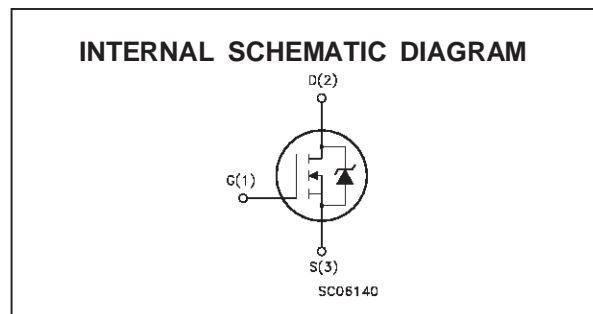
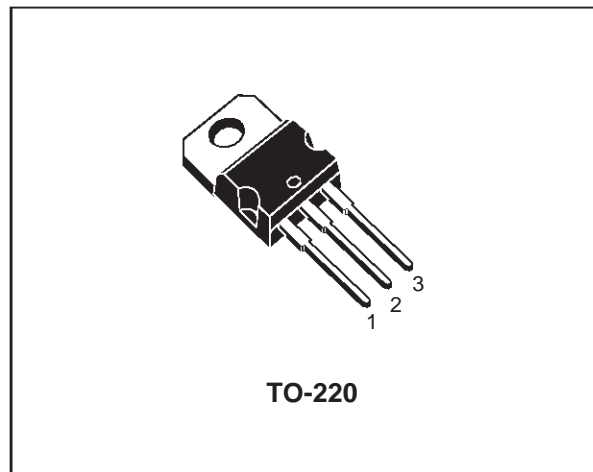
- TYPICAL R<sub>DS(on)</sub> = 1.8  $\Omega$
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

### DESCRIPTION

The PowerMESH™ II is the evolution of the first generation of MESH OVERLAY™. The layout refinements introduced greatly improve the Ron\*area figure of merit while keeping the device at the leading edge for what concerns switching speed, gate charge and ruggedness.

### APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVER



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	600	V
V <sub>DGR</sub>	Drain- gate Voltage (R <sub>GS</sub> = 20 k $\Omega$ )	600	V
V <sub>GS</sub>	Gate-source Voltage	$\pm$ 20	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 25 °C	3.6	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 100 °C	2.3	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	14	A
P <sub>tot</sub>	Total Dissipation at T <sub>c</sub> = 25 °C	75	W
	Derating Factor	0.6	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	3	V/ns
T <sub>stg</sub>	Storage Temperature	-65 to 150	°C
T <sub>j</sub>	Max. Operating Junction Temperature	150	°C

(•) Pulse width limited by safe operating area

(1) I<sub>SD</sub>  $\leq$  3.6 A, di/dt  $\leq$  60 A/ $\mu$ s, V<sub>DD</sub>  $\leq$  V<sub>(BR)DSS</sub>, T<sub>j</sub>  $\leq$  T<sub>JMAX</sub>

# IRFBC30

## THERMAL DATA

R <sub>thj-case</sub>	Thermal Resistance Junction-case	Max	1.7	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient	Max	62.5	°C/W
R <sub>thc-sink</sub>	Thermal Resistance Case-sink	Typ	0.5	°C/W
T <sub>I</sub>	Maximum Lead Temperature For Soldering Purpose		300	°C

## AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	3.6	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	300	mJ

## ELECTRICAL CHARACTERISTICS (T<sub>case</sub> = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA V <sub>GS</sub> = 0	600			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating T <sub>c</sub> = 125 °C			1 50	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V			± 100	nA

ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> I <sub>D</sub> = 250 μA	2	3	4	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V I <sub>D</sub> = 2.2 A		1.8	2.2	Ω
I <sub>D(on)</sub>	On State Drain Current	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> V <sub>GS</sub> = 10 V	3.6			A

## DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (*)	Forward Transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> I <sub>D</sub> = 2.2 A	2.5			S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V f = 1 MHz V <sub>GS</sub> = 0		475		pF
C <sub>oss</sub>	Output Capacitance			72		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			10		pF

**ELECTRICAL CHARACTERISTICS** (continued)  
SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	$V_{DD} = 250\text{ V}$ $I_D = 2.5\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 3)		14		ns
$t_r$	Rise Time			14		ns
$Q_g$	Total Gate Charge	$V_{DD} = 480\text{ V}$ $I_D = 3.6\text{ A}$ $V_{GS} = 10\text{ V}$		16.5	23.1	nC
$Q_{gs}$	Gate-Source Charge			2.5		nC
$Q_{gd}$	Gate-Drain Charge			9		nC

SWITCHING OFF

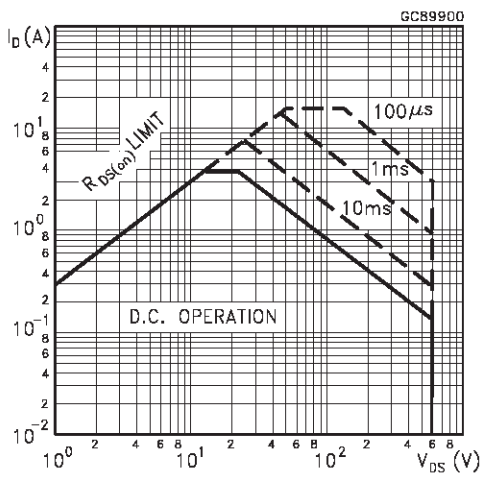
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 480\text{ V}$ $I_D = 3.6\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 5)		15		ns
$t_f$	Fall Time			19		ns
$t_c$	Cross-over Time			24		ns

SOURCE DRAIN DIODE

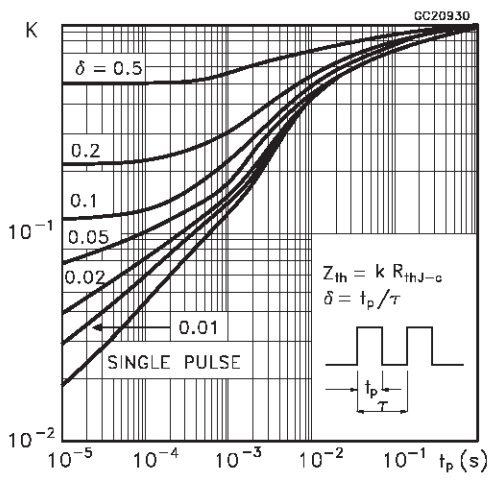
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				3.6	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				14	A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 3.6\text{ A}$ $V_{GS} = 0$			1.6	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 5\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, figure 5)		600		ns
$Q_{rr}$	Reverse Recovery Charge			2.8		$\mu\text{C}$
$I_{RRM}$	Reverse Recovery Current			9		A

(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %  
(•) Pulse width limited by safe operating area

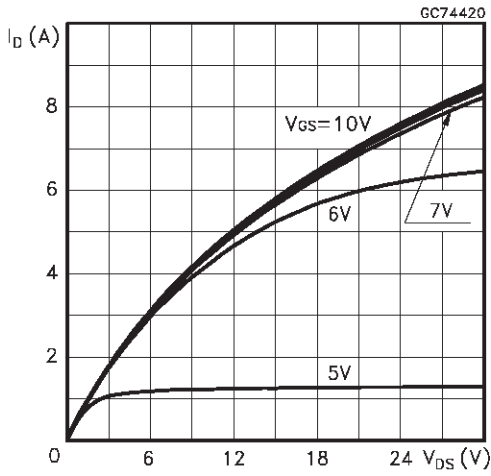
Safe Operating Area



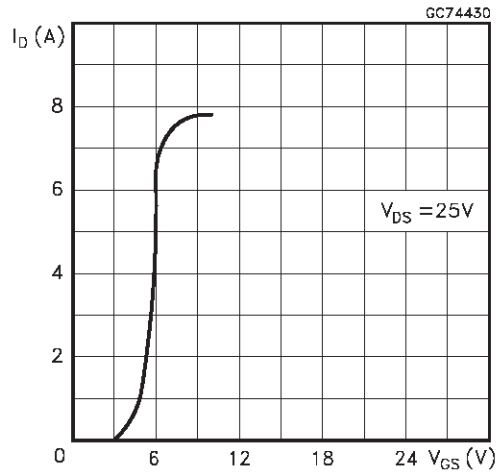
Thermal Impedance



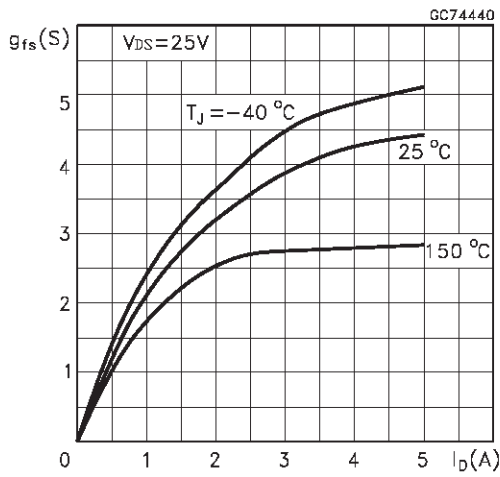
Output Characteristics



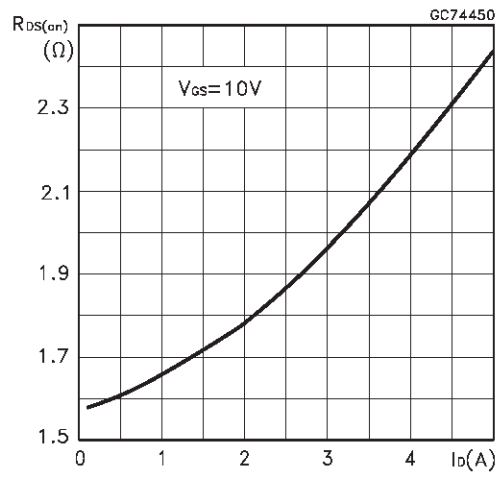
Transfer Characteristics



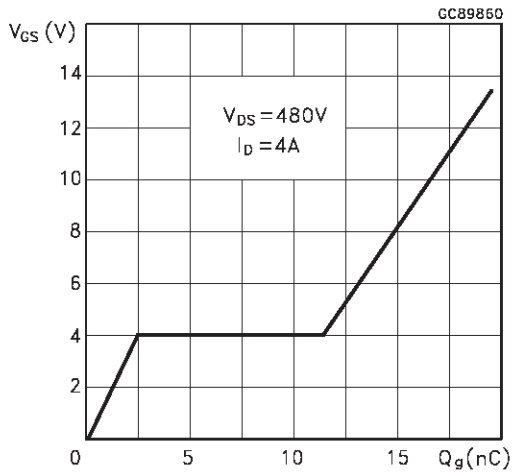
Transconductance



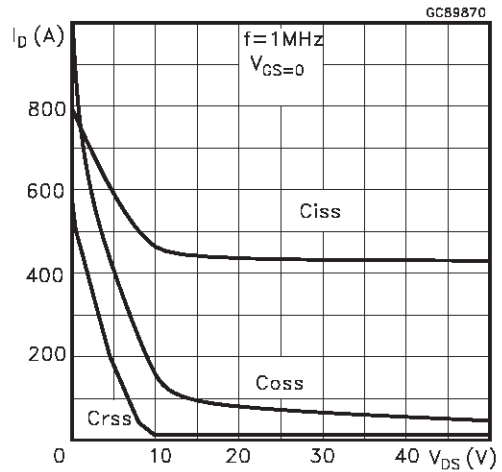
Static Drain-source On Resistance



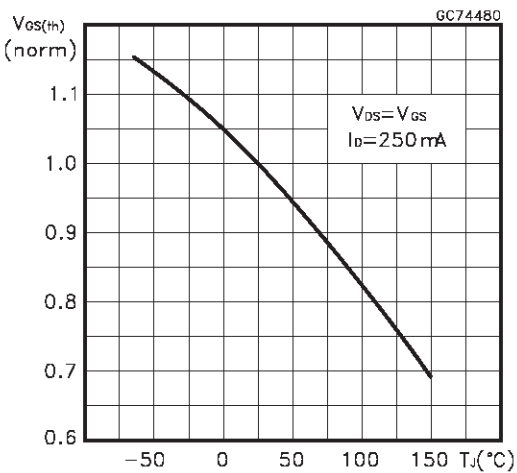
Gate Charge vs Gate-source Voltage



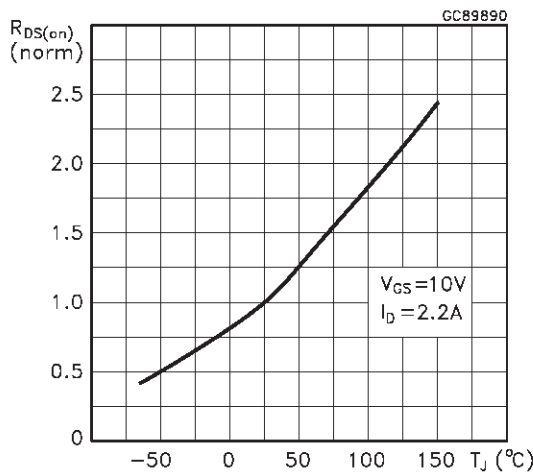
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

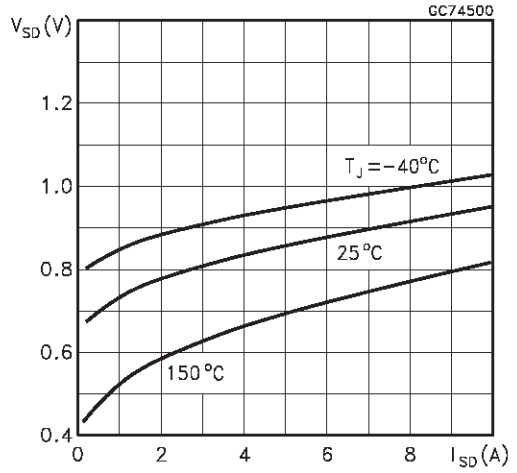


Fig. 1: Unclamped Inductive Load Test Circuit

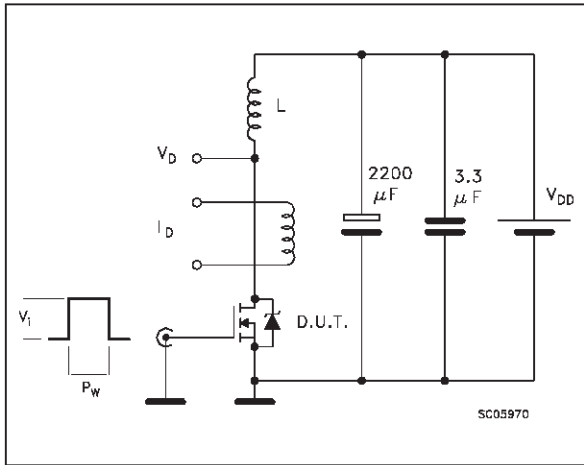


Fig. 1: Unclamped Inductive Waveform

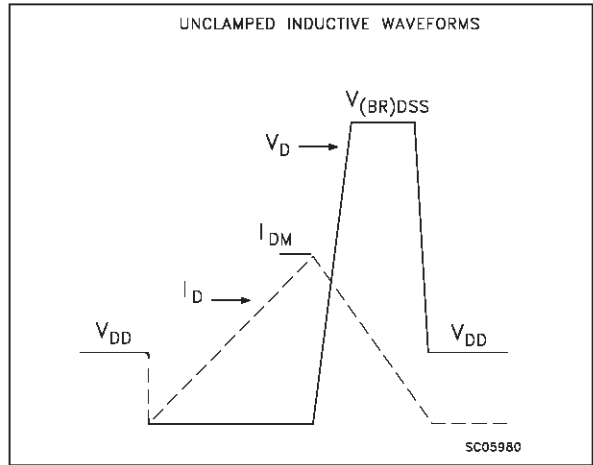


Fig. 3: Switching Times Test Circuits For Resistive Load

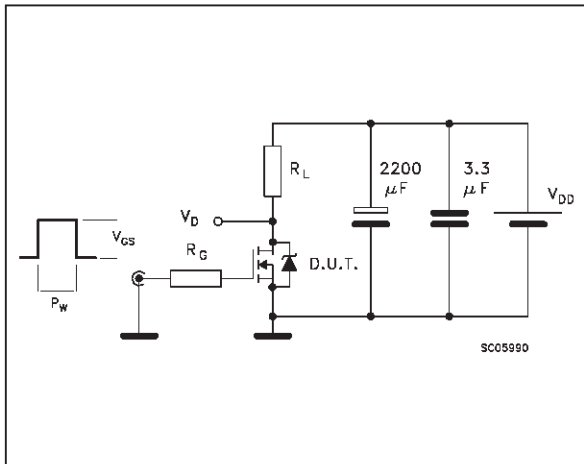


Fig. 4: Gate Charge test Circuit

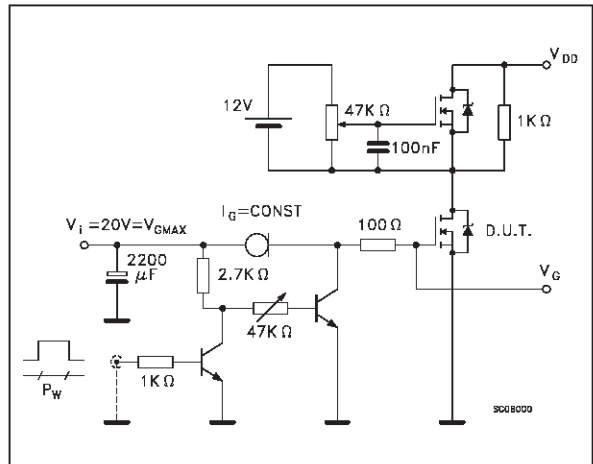
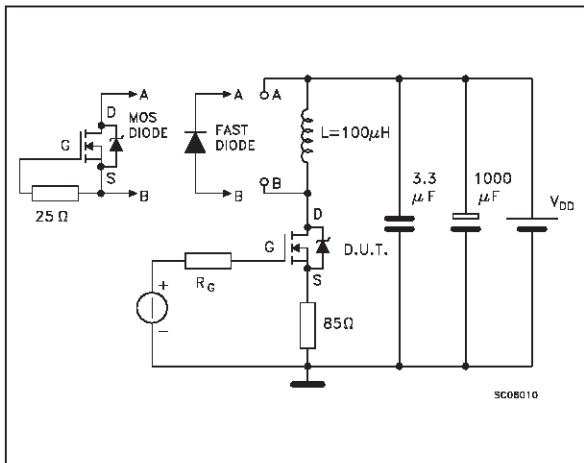
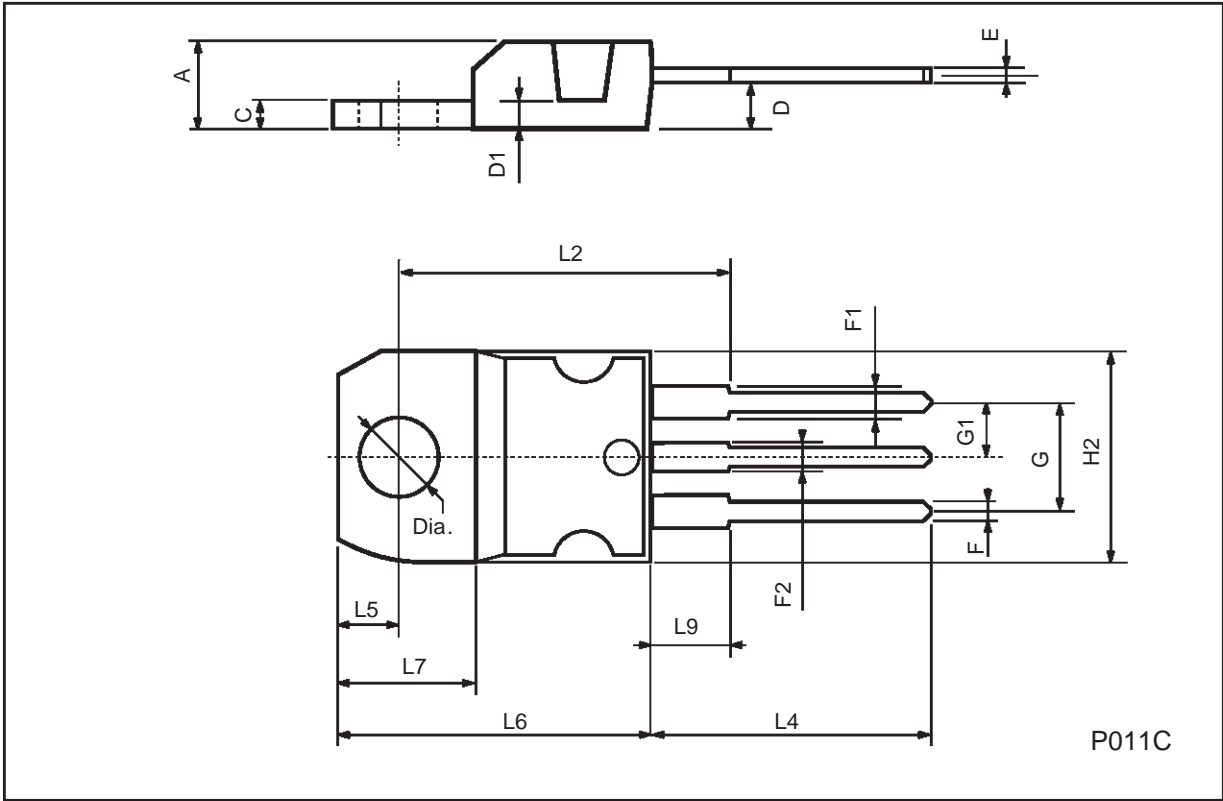


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



**TO-220 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 1999 STMicroelectronics – Printed in Italy – All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -  
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.