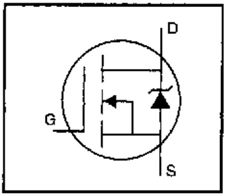
International
IOR Rectifier

IRF744

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



$V_{DSS} = 450V$

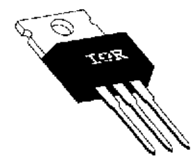
$R_{DS(on)} = 0.63\Omega$

$I_D = 8.8A$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

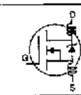
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25°C$	Continuous Drain Current, V_{GS} @ 10 V	8.8	A
I_D @ $T_C = 100°C$	Continuous Drain Current, V_{GS} @ 10 V	5.6	
I_{DM}	Pulsed Drain Current ①	35	
P_D @ $T_C = 25°C$	Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	540	mJ
I_{AR}	Avalanche Current ①	8.8	A
E_{AR}	Repetitive Avalanche Energy ①	13	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.5	V/ns
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

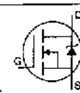
Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.0	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

Electrical Characteristics @ $T_J = 25°C$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	450	—	—	V	V_{GS}=0V, I_D= 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.59	—	V/°C	Reference to 25°C, I_D= 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.63	Ω	V_{GS}=10V, I_D=5.3A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, I_D= 250µA
g_{fs}	Forward Transconductance	4.5	—	—	S	V_{DS}=50V, I_D=5.3A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS}=450V, V_{GS}=0V
		—	—	250		V_{DS}=360V, V_{GS}=0V, T_J=125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS}=-20V
Q_g	Total Gate Charge	—	—	80	nC	I_D=8.8A
Q_{gs}	Gate-to-Source Charge	—	—	12		V_{DS}=360V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	41		V_{GS}=10V See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	8.7	—	ns	V_{DD}=225V
t_r	Rise Time	—	28	—		I_D=8.8A
$t_{d(off)}$	Turn-Off Delay Time	—	58	—		R_G=9.1Ω
t_f	Fall Time	—	27	—		R_D=25Ω See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1400	—	pF	V_{GS}=0V
C_{oss}	Output Capacitance	—	370	—		V_{DS}= 25V
C_{rss}	Reverse Transfer Capacitance	—	140	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	8.8	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	35		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	T_J=25°C, I_S=8.8A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	490	740	ns	T_J=25°C, I_F=8.8A
Q_{rr}	Reverse Recovery Charge	—	3.2	4.8	µC	di/dt=100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② V_{DD}=50V, starting T_J=25°C, L=12mH R_G=25Ω, I_{AS}=8.8A (See Figure 12)

③ I_{SD}≤8.8A, di/dt≤200A/µs, V_{DD}≤$V_{(BR)DSS}$, T_J≤150°C

④ Pulse width ≤ 300 µs; duty cycle ≤2%.

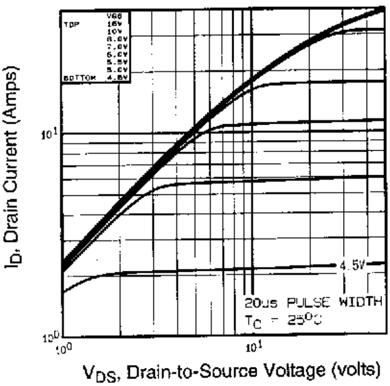


Fig 1. Typical Output Characteristics, T_C=25°C

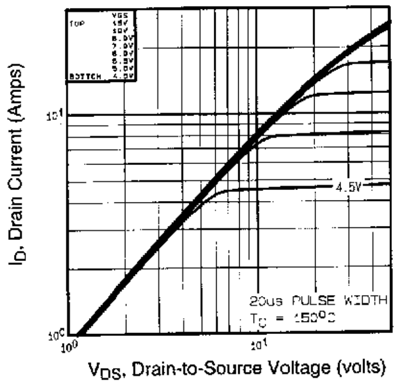


Fig 2. Typical Output Characteristics, T_C=150°C

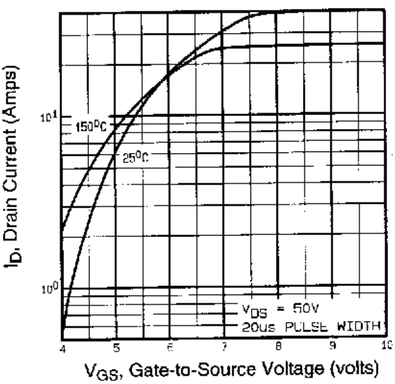


Fig 3. Typical Transfer Characteristics

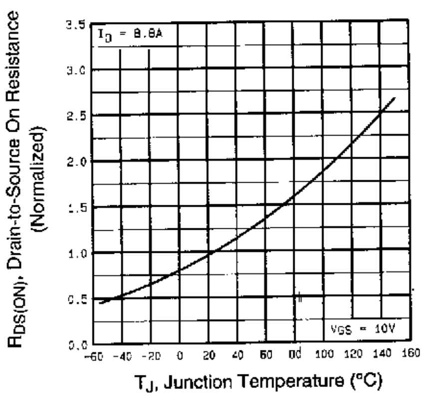


Fig 4. Normalized On-Resistance Vs. Temperature

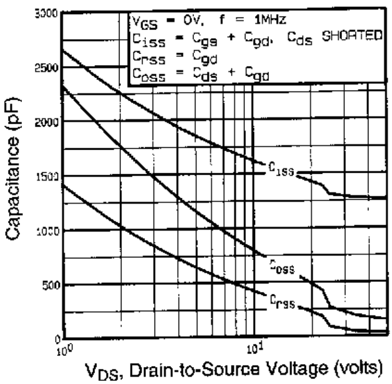


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

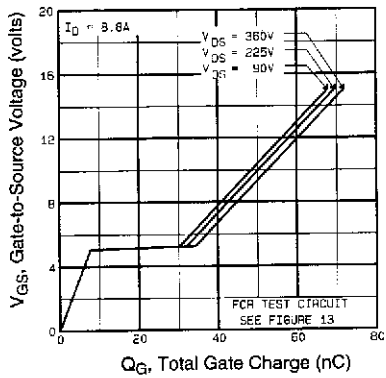


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

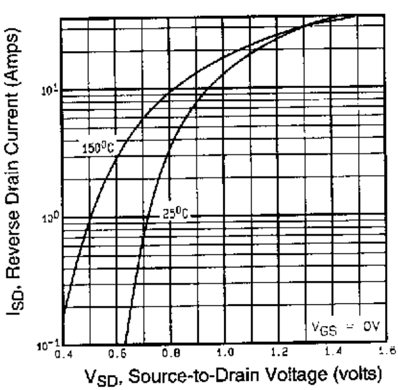


Fig 7. Typical Source-Drain Diode Forward Voltage

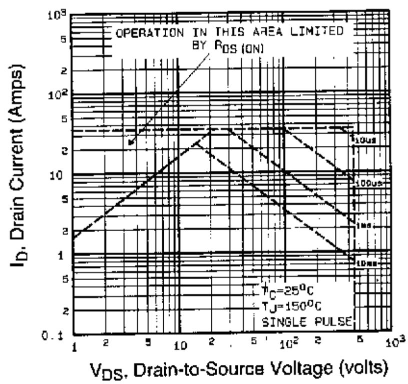


Fig 8. Maximum Safe Operating Area

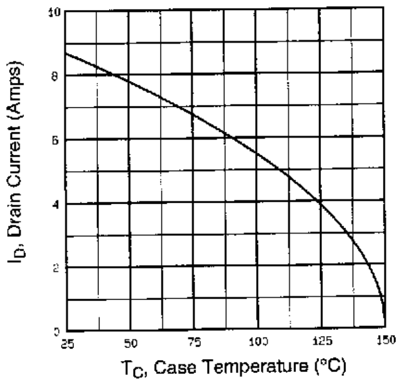


Fig 9. Maximum Drain Current Vs. Case Temperature

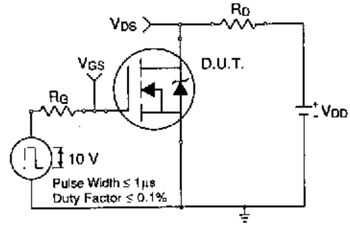


Fig 10a. Switching Time Test Circuit

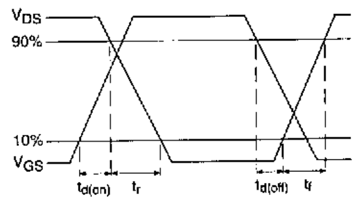


Fig 10b. Switching Time Waveforms

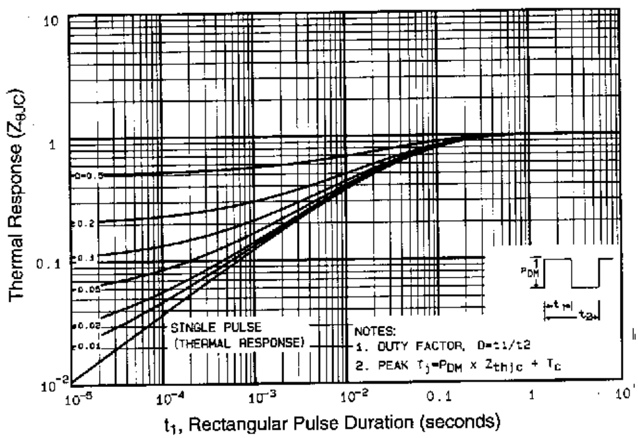


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

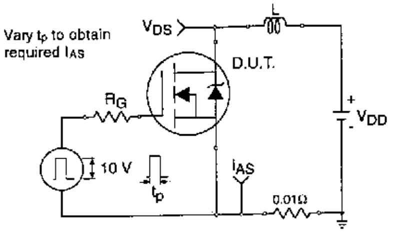


Fig 12a. Unclamped Inductive Test Circuit

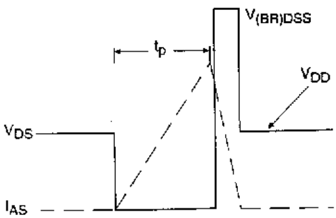


Fig 12b. Unclamped Inductive Waveforms

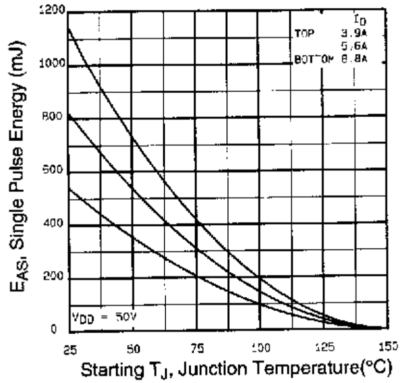


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

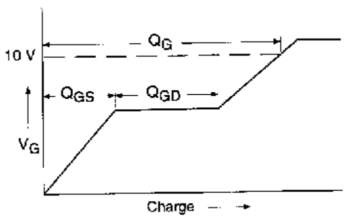


Fig 13a. Basic Gate Charge Waveform

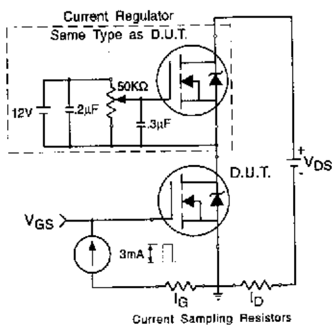
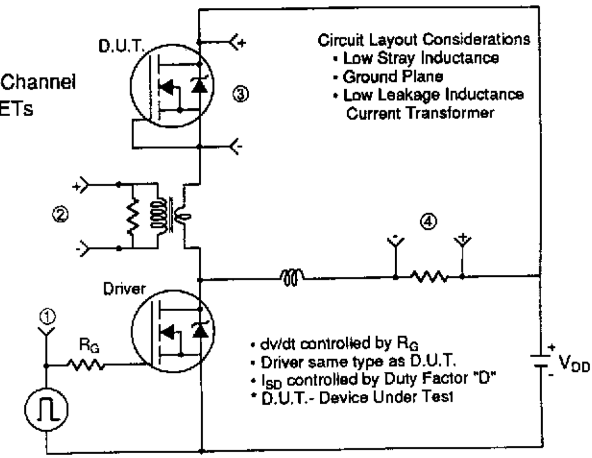


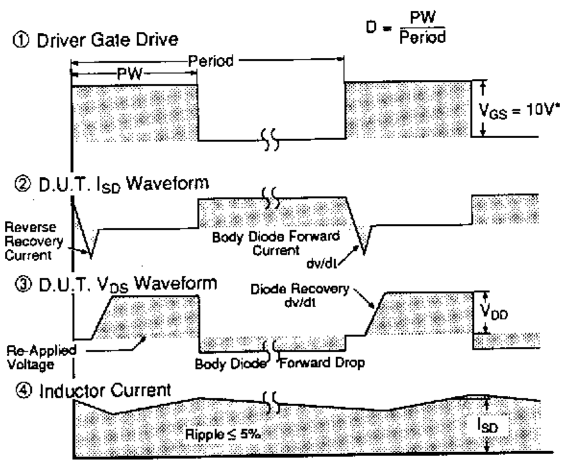
Fig 13b. Gate Charge Test Circuit

Appendix A

Peak Diode Recovery dv/dt Test Circuit

Fig 14. For N-Channel HEXFETs





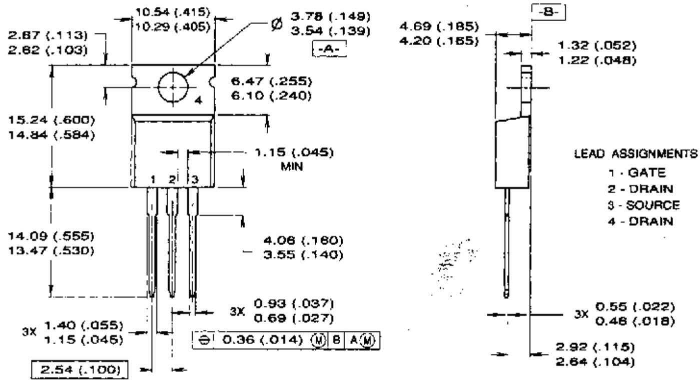
* V_{GS} = 5V for Logic Level Devices

Package Outline

Appendix B

TO-220AB Outline

Dimensions are shown in millimeters (inches)



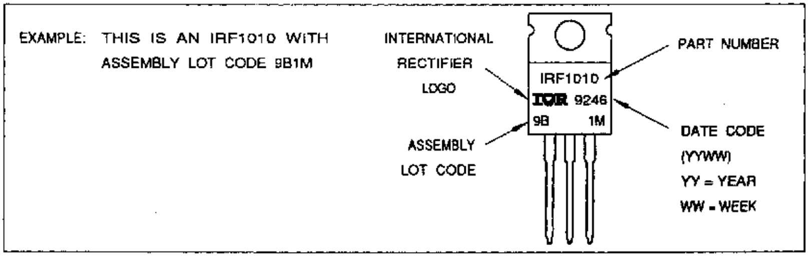
NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION : INCH.
3. OUTLINE CONFORMS TO JEDEC OUTLINE TO-220-AB.
4. HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

Part Marking Information

Appendix C

TO-220AB



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WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322-3331, Twx: 4720403
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB England, Tel: (0883) 713215, Twx: 95219

IR CANADA: 101 Bentley St., Markham, Ontario L3R 3L1, Tel: (416) 475-1897. **IR GERMANY:** Saalburgstrasse 157, D-6380 Bad Homburg, Tel: 6172-37066. **IR ITALY:** Via Liguria 49 10071 Borgaro, Torino, Tel: (011) 470 1484. **IR FAR EAST:** K&H Building, 30-4 Nishiikebukuro 3-Chome, Toshima-ku, Tokyo 171 Japan, Tel: (03) 983 0641. **IR SOUTHEAST ASIA:** 190 Middle Road, HEX 10-01 Fortune Centre, Singapore 0718, Tel: (65) 336 3922.

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