



24-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 24 BITS NO MISSING CODES
- SIMULTANEOUS 50Hz AND 60Hz REJECTION (–90dB MINIMUM)
- 0.0015% INL
- 21 BITS EFFECTIVE RESOLUTION (PGA = 1), 19 BITS (PGA = 128)
- PGA GAINS FROM 1 TO 128
- SINGLE-CYCLE SETTLING
- PROGRAMMABLE DATA OUTPUT RATES
- EXTERNAL DIFFERENTIAL REFERENCE OF 0.1V TO 5V
- ON-CHIP CALIBRATION
- SPI™ COMPATIBLE
- 2.7V TO 5.25V SUPPLY RANGE
- 600µW POWER CONSUMPTION
- UP TO EIGHT INPUT CHANNELS
- UP TO EIGHT DATA I/O

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- LIQUID/GAS CHROMATOGRAPHY
- BLOOD ANALYSIS
- SMART TRANSMITTERS
- PORTABLE INSTRUMENTATION
- WEIGHT SCALES

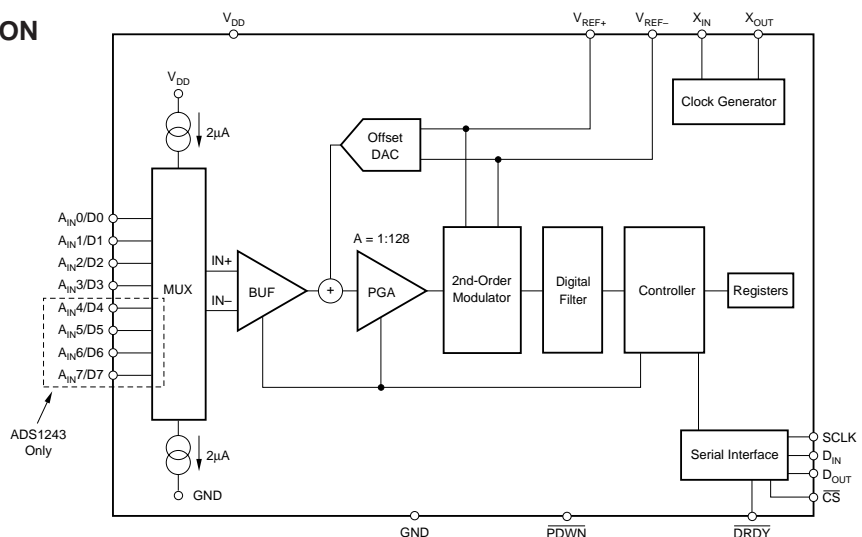
DESCRIPTION

The ADS1242 and ADS1243 are precision, wide dynamic range, delta-sigma, analog-to-digital (A/D) converters with 24-bit resolution operating from 2.7V to 5.25V supplies. These delta-sigma, A/D converters provide up to 24 bits of no missing code performance and effective resolution of 21 bits.

The input channels are multiplexed. Internal buffering can be selected to provide a very high input impedance for direct connection to transducers or low-level voltage signals. Burn-out current sources are provided that allow for the detection of an open or shorted sensor. An 8-bit digital-to-analog converter (DAC) provides an offset correction with a range of 50% of the FSR (Full-Scale Range).

The Programmable Gain Amplifier (PGA) provides selectable gains of 1 to 128 with an effective resolution of 19 bits at a gain of 128. The A/D conversion is accomplished with a second-order delta-sigma modulator and programmable FIR filter that provides a simultaneous 50Hz and 60Hz notch. The reference input is differential and can be used for ratiometric conversion.

The serial interface is SPI compatible. Up to eight bits of data I/O are also provided that can be used for input or output. The ADS1242 and ADS1243 are designed for high-resolution measurement applications in smart transmitters, industrial process control, weight scales, chromatography, and portable instrumentation.



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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | |
|---|--------------------------------------|
| V _{DD} to GND | -0.3V to +6V |
| Input Current | 100mA, Momentary |
| Input Current | 10mA, Continuous |
| A _{IN} | GND - 0.5V to V _{DD} + 0.5V |
| Digital Input Voltage to GND | -0.3V to V _{DD} + 0.3V |
| Digital Output Voltage to GND | -0.3V to V _{DD} + 0.3V |
| Maximum Junction Temperature | +150°C |
| Operating Temperature Range | -40°C to +85°C |
| Storage Temperature Range | -60°C to +100°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DEMO BOARD ORDERING INFORMATION

| PRODUCT | DESCRIPTION |
|-------------|---------------------------|
| ADS1241-EVM | ADS1241 Evaluation Module |

PACKAGE/ORDERING INFORMATION⁽¹⁾

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER ⁽²⁾ | TRANSPORT MEDIA, QUANTITY |
|---------|--------------|--------------------|-----------------------------|-----------------|--------------------------------|---------------------------|
| ADS1242 | TSSOP-16 | PW | -40°C to +85°C | ADS1242 | ADS1242IPWT | Tape and Reel, 250 |
| " | " | " | " | " | ADS1242IPWR | Tape and Reel, 2500 |
| ADS1243 | TSSOP-20 | PW | -40°C to +85°C | ADS1243 | ADS1243IPWT | Tape and Reel, 250 |
| " | " | " | " | " | ADS1243IPWR | Tape and Reel, 2500 |

NOTES: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

(2) The ordering number contains grade, temperature range, package, and transport media information. Ordering the ADS1242IPWT will get a single 250-piece tape and reel of the ADS1242, Industrial Temperature Range device in a PW package.

DIGITAL CHARACTERISTICS: T_{MIN} to T_{MAX}, V_{DD} 2.7V to 5.25V

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------------|----------------------------------|-----------------------|------|-----------------------|-------|
| Digital Input/Output Logic Family | | | CMOS | | |
| Logic Level: V _{IH} | | 0.8 • V _{DD} | | V _{DD} | V |
| V _{IL} ⁽¹⁾ | | GND | | 0.2 • V _{DD} | V |
| V _{OH} | I _{OH} = 1mA | V _{DD} - 0.4 | | | V |
| V _{OL} | I _{OL} = 1mA | GND | | GND + 0.4 | V |
| Input Leakage: I _{IH} | V _I = V _{DD} | | | 10 | μA |
| I _{IL} | V _I = 0 | -10 | | | μA |
| Master Clock Rate: f _{OSC} | | 1 | | 5 | MHz |
| Master Clock Period: t _{OSC} | 1/f _{OSC} | 200 | | 1000 | ns |

NOTE: (1) V_{IL} for X_{IN} is GND to GND + 0.05V.

ELECTRICAL CHARACTERISTICS: $V_{DD} = 5V$

All specifications T_{MIN} to T_{MAX} , $V_{DD} = +5V$, $f_{MOD} = 19.2kHz$, $PGA = 1$, Buffer ON, $f_{DATA} = 15Hz$, $V_{REF} \equiv (REF\ IN+) - (REF\ IN-) = +2.5V$, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS1242 ADS1243 | | | UNITS |
|--|--|-------------------------|--|----------------------------------|--------------------------|
| | | MIN | TYP | MAX | |
| ANALOG INPUT ($A_{IN0} - A_{IN7}$) | | | | | |
| Analog Input Range | Buffer OFF Buffer ON | GND - 0.1 GND + 0.05 | | $V_{DD} + 0.1$ $V_{DD} - 1.5$ | V V |
| Full-Scale Input Range | ($IN+$) - ($IN-$), See Block Diagram, RANGE = 0 | | | $\pm V_{REF}/PGA$ | V |
| Differential Input Impedance | RANGE = 1 Buffer OFF Buffer ON | | 5/PGA 5 | $\pm V_{REF}/(2 \cdot PGA)$ | M Ω G Ω |
| Bandwidth | | | | | |
| $f_{DATA} = 3.75Hz$ | -3dB | | 1.65 | | Hz |
| $f_{DATA} = 7.50Hz$ | -3dB | | 3.44 | | Hz |
| $f_{DATA} = 15.00Hz$ | -3dB | | 14.6 | | Hz |
| Programmable Gain Amplifier | User-Selectable Gain Ranges | 1 | | 128 | |
| Input Capacitance | | | 9 | | pF |
| Input Leakage Current | Modulator OFF, T = 25°C | | 5 | | pA |
| Burnout Current Sources | | | 2 | | μA |
| OFFSET DAC | | | | | |
| Offset DAC Range | RANGE = 0 RANGE = 1 | | $\pm V_{REF}/(2 \cdot PGA)$ $\pm V_{REF}/(4 \cdot PGA)$ | | V V |
| Offset DAC Monotonicity | | 8 | | | Bits |
| Offset DAC Gain Error | | | ± 10 | | % |
| Offset DAC Gain Error Drift | | | 1 | | ppm/°C |
| SYSTEM PERFORMANCE | | | | | |
| Resolution | No Missing Codes | 24 | | | Bits |
| Integral Nonlinearity | End Point Fit | | | ± 0.0015 | % of FS |
| Offset Error ⁽¹⁾ | | | 7.5 | | ppm of FS |
| Offset Drift ⁽¹⁾ | | | 0.02 | | ppm of FS/°C |
| Gain Error ⁽¹⁾ | | | 0.005 | | % |
| Gain Error Drift ⁽¹⁾ | | | 0.5 | | ppm/°C |
| Common-Mode Rejection | at DC | 100 | | | dB |
| | $f_{CM} = 60Hz, f_{DATA} = 15Hz$ | | 130 | | dB |
| | $f_{CM} = 50Hz, f_{DATA} = 15Hz$ | | 120 | | dB |
| Normal-Mode Rejection | $f_{SIG} = 50Hz, f_{DATA} = 15Hz$ | | 100 | | dB |
| | $f_{SIG} = 60Hz, f_{DATA} = 15Hz$ | | 100 | | dB |
| Output Noise | | | See Typical Characteristics | | |
| Power-Supply Rejection | at DC, dB = $-20 \log(\Delta V_{OUT}/V_{DD})^{(2)}$ | 80 | 95 | | dB |
| VOLTAGE REFERENCE INPUT | | | | | |
| Reference Input Range | REF IN+, REF IN- | 0 | | V_{DD} | V |
| V_{REF} | $V_{REF} \equiv (REF\ IN+) - (REF\ IN-)$, RANGE = 0 | 0.1 | 2.5 | 2.6 | V |
| | RANGE = 1 | 0.1 | | V_{DD} | V |
| Common-Mode Rejection | at DC | | 120 | | dB |
| Common-Mode Rejection | $f_{VREFCM} = 60Hz, f_{DATA} = 15Hz$ | | 120 | | dB |
| Bias Current ⁽³⁾ | $V_{REF} = 2.5V$ | | 1.3 | | μA |
| POWER-SUPPLY REQUIREMENTS | | | | | |
| Power-Supply Voltage | V_{DD} | 4.75 | | 5.25 | V |
| Current | PGA = 1, Buffer OFF | | 240 | 375 | μA |
| | PGA = 128, Buffer OFF | | 450 | 800 | μA |
| | PGA = 1, Buffer ON | | 290 | 425 | μA |
| | PGA = 128, Buffer ON | | 960 | 1400 | μA |
| | SLEEP Mode | | 60 | | μA |
| | Read Data Continuous Mode | | 230 | | μA |
| | PDWNN | | 0.5 | | nA |
| Power Dissipation | PGA = 1, Buffer OFF | | 1.2 | 1.9 | mW |
| TEMPERATURE RANGE | | | | | |
| Operating | | -40 | | +85 | °C |
| Storage | | -60 | | +100 | °C |

NOTES: (1) Calibration can minimize these errors. (2) ΔV_{OUT} is a change in digital result. (3) 12pF switched capacitor at f_{SAMP} clock frequency.

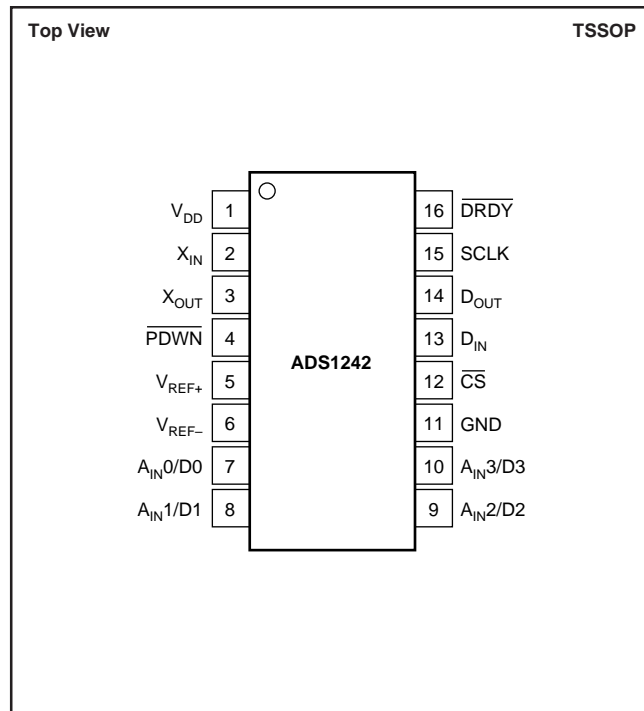
ELECTRICAL CHARACTERISTICS: $V_{DD} = 3V$

All specifications T_{MIN} to T_{MAX} , $V_{DD} = +3V$, $f_{MOD} = 19.2kHz$, $PGA = 1$, Buffer ON, $f_{DATA} = 15Hz$, $V_{REF} \equiv (REF\ IN+) - (REF\ IN-) = +1.25V$, unless otherwise specified.

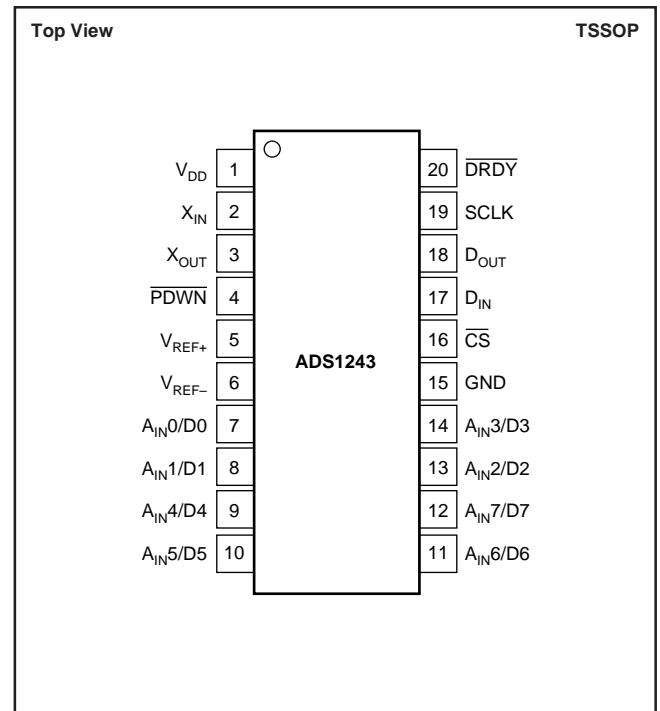
| PARAMETER | CONDITIONS | ADS1242 ADS1243 | | | UNITS |
|--|--|--------------------|----------|-----------------------------|--------------|
| | | MIN | TYP | MAX | |
| ANALOG INPUT ($A_{IN0} - A_{IN7}$) | | | | | |
| Analog Input Range | Buffer OFF | GND - 0.1 | | $V_{DD} + 0.1$ | V |
| Full-Scale Input Voltage Range | Buffer ON | GND + 0.05 | | $V_{DD} - 1.5$ | V |
| | (In+) - (In-) See Block Diagram, RANGE = 0 | | | $\pm V_{REF}/PGA$ | V |
| Input Impedance | RANGE = 1 | | | $\pm V_{REF}/(2 \cdot PGA)$ | V |
| | Buffer OFF | | 5/PGA | | M Ω |
| Bandwidth | Buffer ON | | 5 | | G Ω |
| | | | | | |
| $f_{DATA} = 3.75Hz$ | -3dB | | 1.65 | | Hz |
| $f_{DATA} = 7.50Hz$ | -3dB | | 3.44 | | Hz |
| $f_{DATA} = 15.00Hz$ | -3dB | | 14.6 | | Hz |
| Programmable Gain Amplifier | User-Selectable Gain Ranges | 1 | | 128 | |
| Input Capacitance | | | 9 | | pF |
| Input Leakage Current | Modulator OFF, T = 25°C | | 5 | | pA |
| Burnout Current Sources | | | 2 | | μA |
| OFFSET DAC | | | | | |
| Offset DAC Range | RANGE = 0 | | | $\pm V_{REF}/(2 \cdot PGA)$ | V |
| | RANGE = 1 | | | $\pm V_{REF}/(4 \cdot PGA)$ | V |
| Offset DAC Monotonicity | | 8 | | | Bits |
| Offset DAC Gain Error | | | ± 10 | | % |
| Offset DAC Gain Error Drift | | | 2 | | ppm/°C |
| SYSTEM PERFORMANCE | | | | | |
| Resolution | No Missing Codes | 24 | | | Bits |
| Integral Nonlinearity | End Point Fit | | | ± 0.0015 | % of FS |
| Offset Error ⁽¹⁾ | | | 15 | | ppm of FS |
| Offset Drift ⁽¹⁾ | | | 0.04 | | ppm of FS/°C |
| Gain Error ⁽¹⁾ | | | 0.01 | | % |
| Gain Error Drift ⁽¹⁾ | | | 1.0 | | ppm/°C |
| Common-Mode Rejection | at DC | 100 | | | dB |
| | $f_{CM} = 60Hz$, $f_{DATA} = 15Hz$ | | 130 | | dB |
| Normal-Mode Rejection | $f_{CM} = 50Hz$, $f_{DATA} = 15Hz$ | | 120 | | dB |
| | $f_{SIG} = 50Hz$, $f_{DATA} = 15Hz$ | | 100 | | dB |
| Output Noise | $f_{SIG} = 60Hz$, $f_{DATA} = 15Hz$ | | 100 | | dB |
| | | | | | |
| Power-Supply Rejection | at DC, dB = $-20 \log(\Delta V_{OUT}/V_{DD})^{(2)}$ | 75 | 90 | | dB |
| VOLTAGE REFERENCE INPUT | | | | | |
| Reference Input Range | REF IN+, REF IN- | 0 | | V_{DD} | V |
| V_{REF} | $V_{REF} \equiv (REF\ IN+) - (REF\ IN-)$, RANGE = 0 | 0.1 | 1.25 | 1.30 | V |
| | RANGE = 1 | 0.1 | 2.5 | 2.6 | V |
| Common-Mode Rejection | at DC | | 120 | | dB |
| Common-Mode Rejection | $f_{VREFCM} = 60Hz$, $f_{DATA} = 15Hz$ | | 120 | | dB |
| Bias Current ⁽³⁾ | $V_{REF} = 1.25$ | | 0.65 | | μA |
| POWER-SUPPLY REQUIREMENTS | | | | | |
| Power-Supply Voltage | V_{DD} | 2.7 | | 3.3 | V |
| Current | PGA = 1, Buffer OFF | | 190 | 375 | μA |
| | PGA = 128, Buffer OFF | | 460 | 700 | μA |
| | PGA = 1, Buffer ON | | 240 | 375 | μA |
| | PGA = 128, Buffer ON | | 870 | 1325 | μA |
| | SLEEP Mode | | 75 | | μA |
| | Read Data Continuous Mode | | 113 | | μA |
| | PDWN = 0 | | 0.5 | | nA |
| Power Dissipation | PGA = 1, Buffer OFF | | 0.6 | 1.2 | mW |
| TEMPERATURE RANGE | | | | | |
| Operating | | -40 | | +85 | °C |
| Storage | | -60 | | +100 | °C |

NOTES: (1) Calibration can minimize these errors. (2) ΔV_{OUT} is a change in digital result. (3) 12pF switched capacitor at f_{SAMP} clock frequency.

PIN CONFIGURATION (ADS1242)



PIN CONFIGURATION (ADS1243)



PIN DESCRIPTIONS (ADS1242)

| PIN NUMBER | NAME | DESCRIPTION |
|------------|-------------------|---|
| 1 | V_{DD} | Power Supply |
| 2 | X_{IN} | Clock Input |
| 3 | X_{OUT} | Clock Output, used with crystal or ceramic resonator. |
| 4 | \overline{PDWN} | Active LOW. Power Down. The power down function shuts down the analog and digital circuits. |
| 5 | V_{REF+} | Positive Differential Reference Input |
| 6 | V_{REF-} | Negative Differential Reference Input |
| 7 | $A_{IN0/D0}$ | Analog Input 0/Data I/O 0 |
| 8 | $A_{IN1/D1}$ | Analog Input 1/Data I/O 1 |
| 9 | $A_{IN2/D2}$ | Analog Input 2/Data I/O 2 |
| 10 | $A_{IN3/D3}$ | Analog Input 3/Data I/O 3 |
| 11 | GND | Ground |
| 12 | \overline{CS} | Active LOW, Chip Select |
| 13 | D_{IN} | Serial Data Input, Schmitt Trigger |
| 14 | D_{OUT} | Serial Data Output |
| 15 | SCLK | Serial Clock, Schmitt Trigger |
| 16 | \overline{DRDY} | Active LOW, Data Ready |

PIN DESCRIPTIONS (ADS1243)

| PIN NUMBER | NAME | DESCRIPTION |
|------------|-------------------|---|
| 1 | V_{DD} | Power Supply |
| 2 | X_{IN} | Clock Input |
| 3 | X_{OUT} | Clock Output, used with crystal or ceramic resonator. |
| 4 | \overline{PDWN} | Active LOW. Power Down. The power down function shuts down the analog and digital circuits. |
| 5 | V_{REF+} | Positive Differential Reference Input |
| 6 | V_{REF-} | Negative Differential Reference Input |
| 7 | $A_{IN0/D0}$ | Analog Input 0/Data I/O 0 |
| 8 | $A_{IN1/D1}$ | Analog Input 1/Data I/O 1 |
| 9 | $A_{IN4/D4}$ | Analog Input 4/Data I/O 4 |
| 10 | $A_{IN5/D5}$ | Analog Input 5/Data I/O 5 |
| 11 | $A_{IN6/D6}$ | Analog Input 6/Data I/O 6 |
| 12 | $A_{IN7/D7}$ | Analog Input 7/Data I/O 7 |
| 13 | $A_{IN2/D2}$ | Analog Input 2/Data I/O 2 |
| 14 | $A_{IN3/D3}$ | Analog Input 3/Data I/O 3 |
| 15 | GND | Ground |
| 16 | \overline{CS} | Active LOW, Chip Select |
| 17 | D_{IN} | Serial Data Input, Schmitt Trigger |
| 18 | D_{OUT} | Serial Data Output |
| 19 | SCLK | Serial Clock, Schmitt Trigger |
| 20 | \overline{DRDY} | Active LOW, Data Ready |

TIMING DIAGRAMS

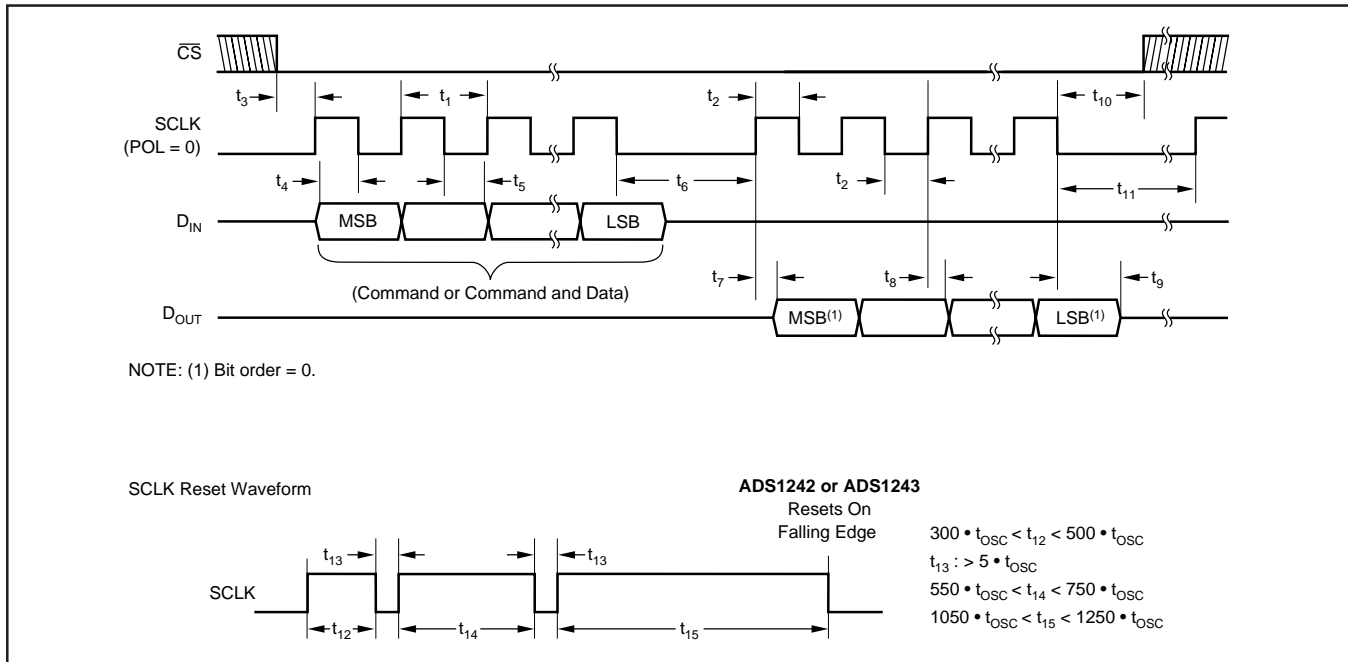


DIAGRAM 1.

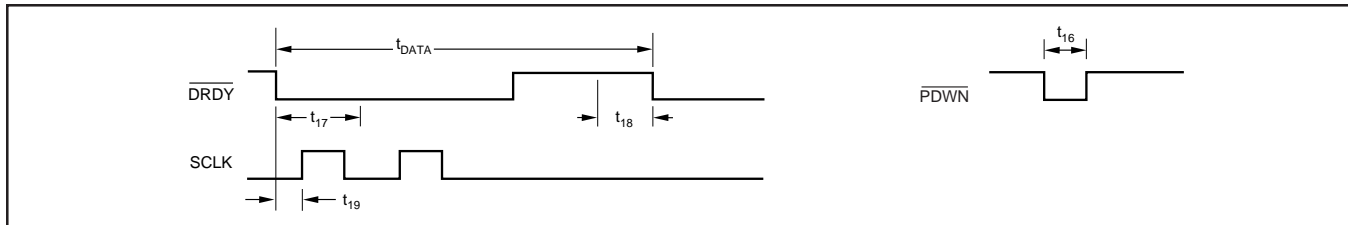


DIAGRAM 2.

TIMING CHARACTERISTICS TABLES

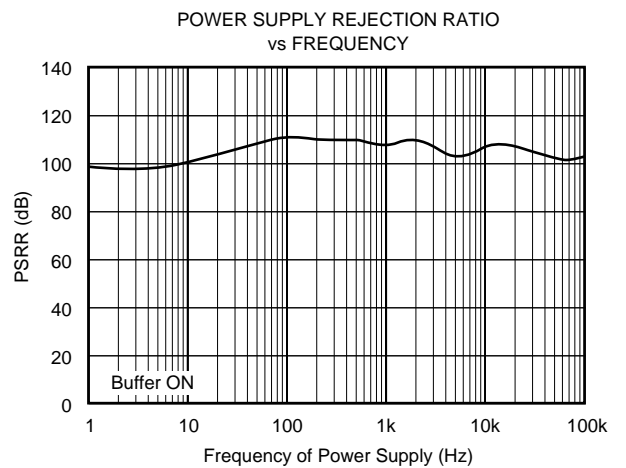
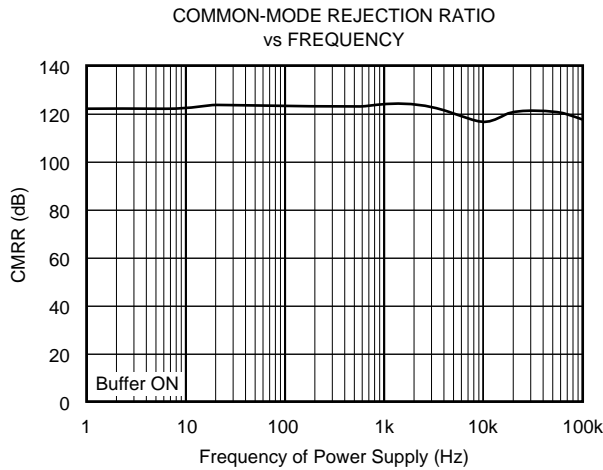
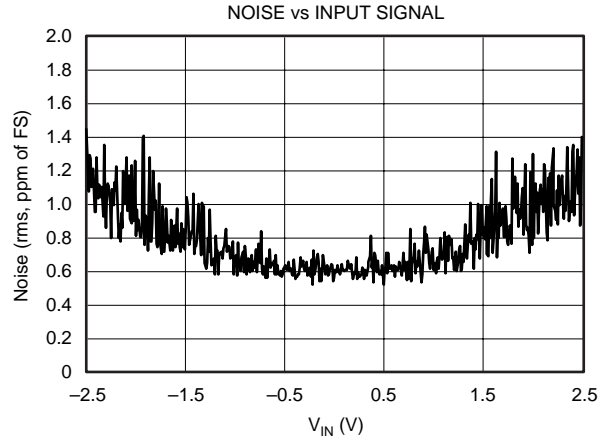
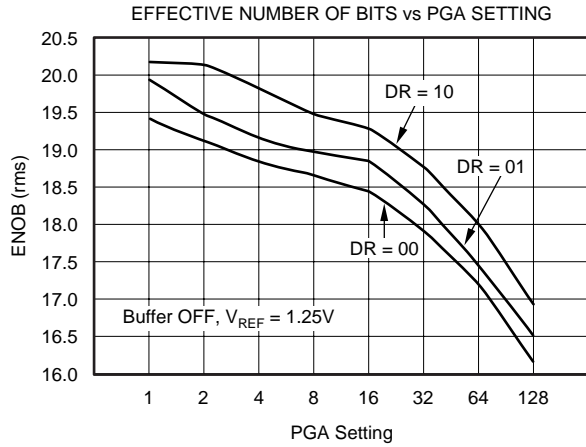
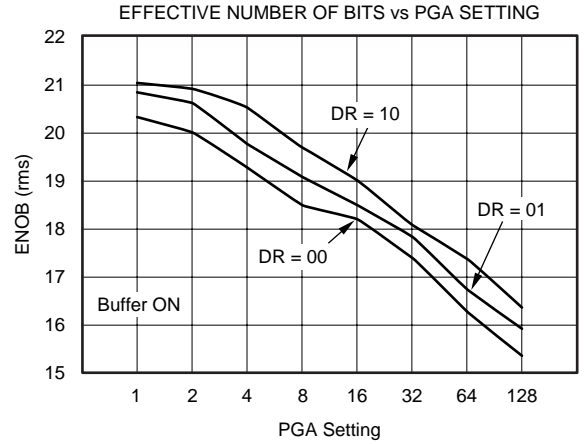
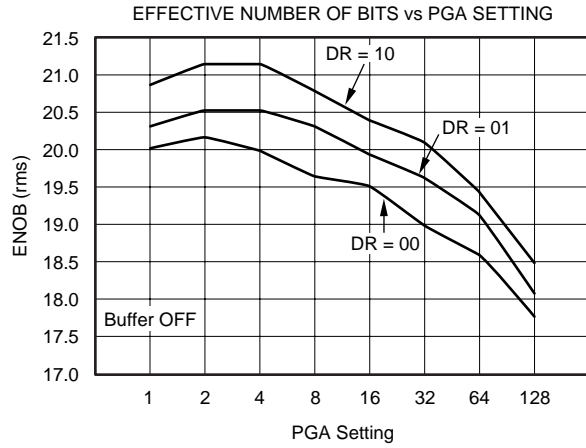
| SPEC | DESCRIPTION | MIN | MAX | UNITS |
|-------------|--|-------------------|------|--|
| t_1 | SCLK Period | 4 | 3 | t_{OSC} Periods \overline{DRDY} Periods |
| t_2 | SCLK Pulse Width, HIGH and LOW | 200 | | ns |
| t_3 | \overline{CS} low to first SCLK Edge; Setup Time ⁽²⁾ | 0 | | ns |
| t_4 | D_{IN} Valid to SCLK Edge; Setup Time | 50 | | ns |
| t_5 | Valid D_{IN} to SCLK Edge; Hold Time | 50 | | ns |
| t_6 | Delay between last SCLK edge for D_{IN} and first SCLK edge for D_{OUT} : RDATA, RDATA, RREG, WREG | 50 | | t_{OSC} Periods |
| $t_7^{(1)}$ | SCLK Edge to Valid New D_{OUT} | | 50 | ns |
| $t_8^{(1)}$ | SCLK Edge to D_{OUT} , Hold Time | 0 | | ns |
| t_9 | Last SCLK Edge to D_{OUT} Tri-State NOTE: D_{OUT} goes tri-state immediately when \overline{CS} goes HIGH. | 6 | 10 | t_{OSC} Periods |
| t_{10} | \overline{CS} LOW time after final SCLK edge. | 0 | | ns |
| t_{11} | Final SCLK edge of one command until first edge SCLK of next command: RREG, WREG, DSYNC, SLEEP, RDATA, RDATA, STOPC SELFGCAL, SELFOCAL, SYSOCAL, SYSGCAL SELFCAL RESET (also SCLK Reset) | 4 2 4 16 | | t_{OSC} Periods \overline{DRDY} Periods \overline{DRDY} Periods t_{OSC} Periods |
| t_{16} | Pulse Width | 4 | | t_{OSC} Periods |
| t_{17} | Allowed analog input change for next valid conversion. | | 5000 | t_{OSC} Periods |
| t_{18} | DOR update, DOR data not valid. | 4 | | t_{OSC} Periods |
| t_{19} | First SCLK after \overline{DRDY} goes LOW: RDATA Mode Any other mode | 10 0 | | t_{OSC} Periods t_{OSC} Periods |

NOTES: (1) Load = 20pF || 10kΩ to GND.

(2) \overline{CS} may be tied LOW.

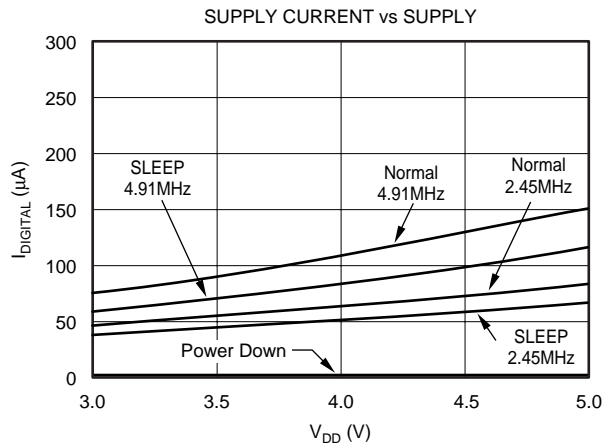
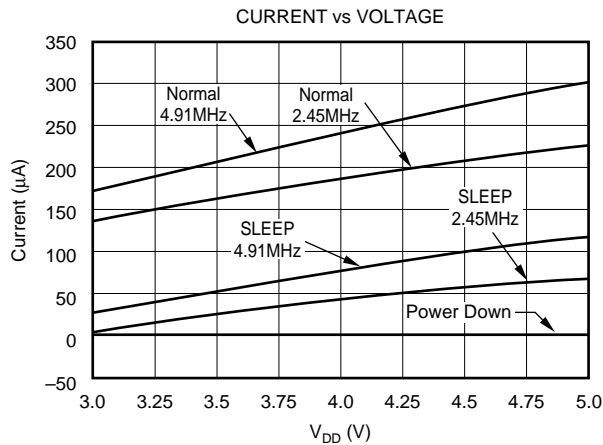
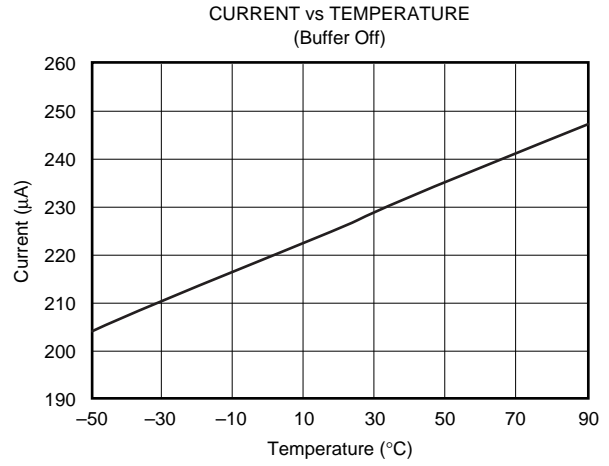
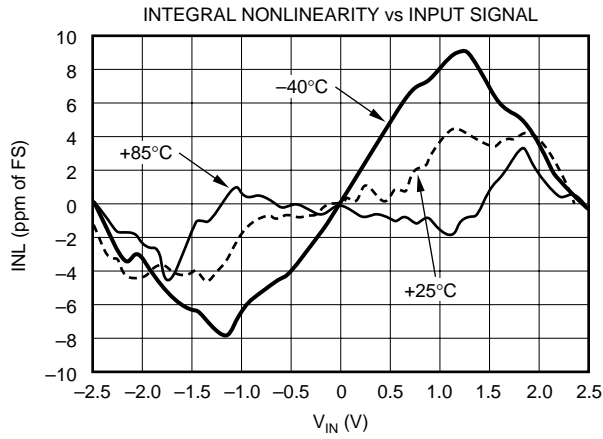
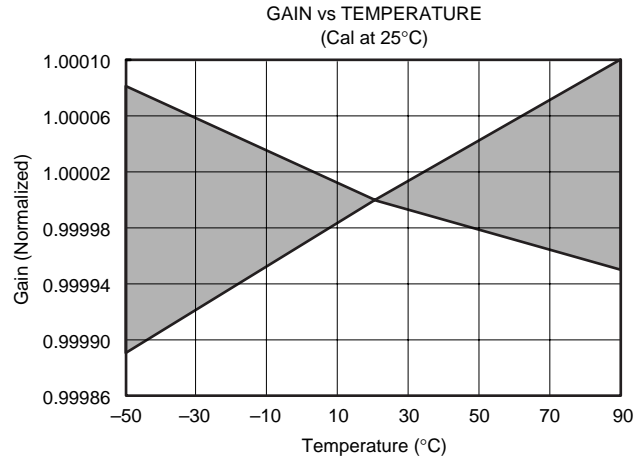
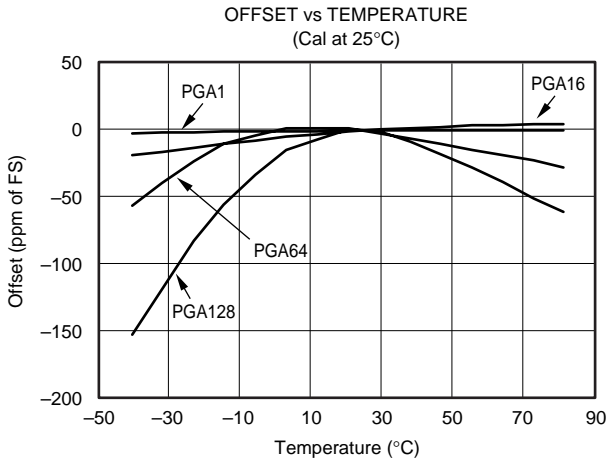
TYPICAL CHARACTERISTICS

All specifications, $V_{DD} = +5V$, $f_{OSC} = 2.4576MHz$, $PGA = 1$, $f_{DATA} = 15Hz$, and $V_{REF} \equiv (REF IN+) - (REF IN-) = +2.5V$, unless otherwise specified.



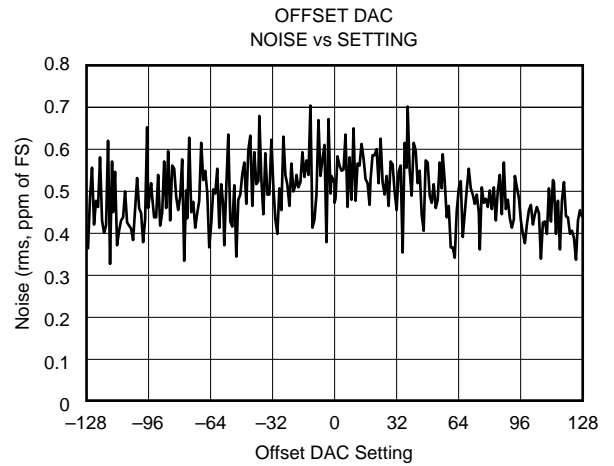
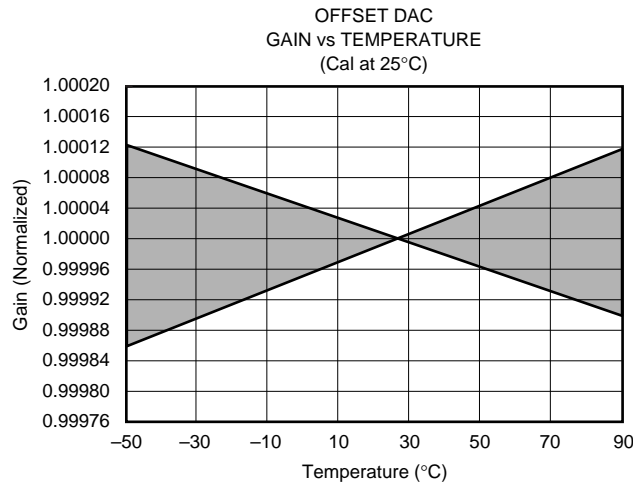
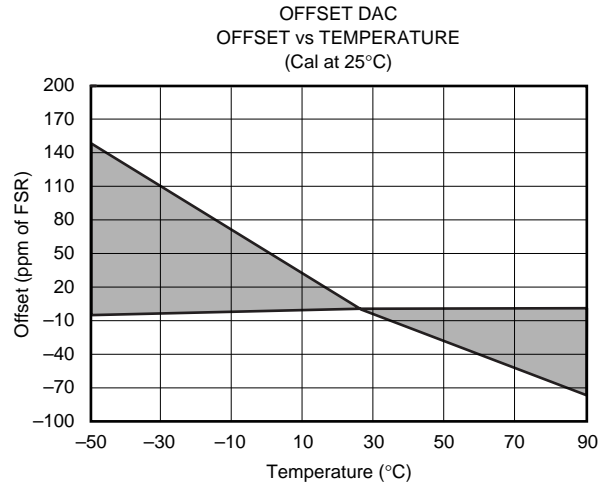
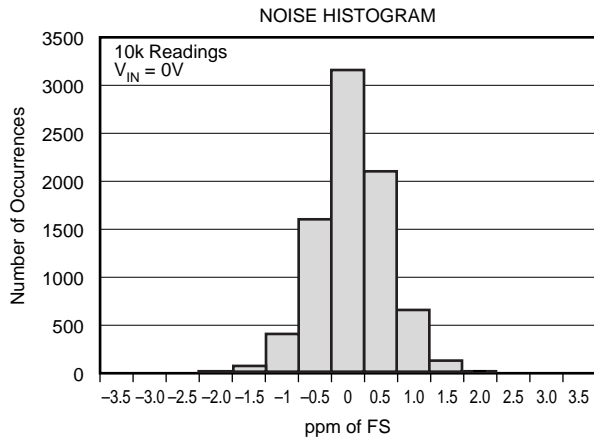
TYPICAL CHARACTERISTICS (Cont.)

All specifications, $V_{DD} = +5V$, $f_{OSC} = 2.4576MHz$, $PGA = 1$, $f_{DATA} = 15Hz$, and $V_{REF} \equiv (REF\ IN+) - (REF\ IN-) = +2.5V$, unless otherwise specified.



TYPICAL CHARACTERISTICS (Cont.)

All specifications, $V_{DD} = +5V$, $f_{OSC} = 2.4576MHz$, $PGA = 1$, $f_{DATA} = 15Hz$, and $V_{REF} \equiv (REF IN+) - (REF IN-) = +2.5V$, unless otherwise specified.



OVERVIEW

INPUT MULTIPLEXER

The input multiplexer provides for any combination of differential inputs to be selected on any of the input channels, as shown in Figure 1. For example, if A_{IN0} is selected as the positive differential input channel, any other channel can be selected as the negative terminal for the differential input

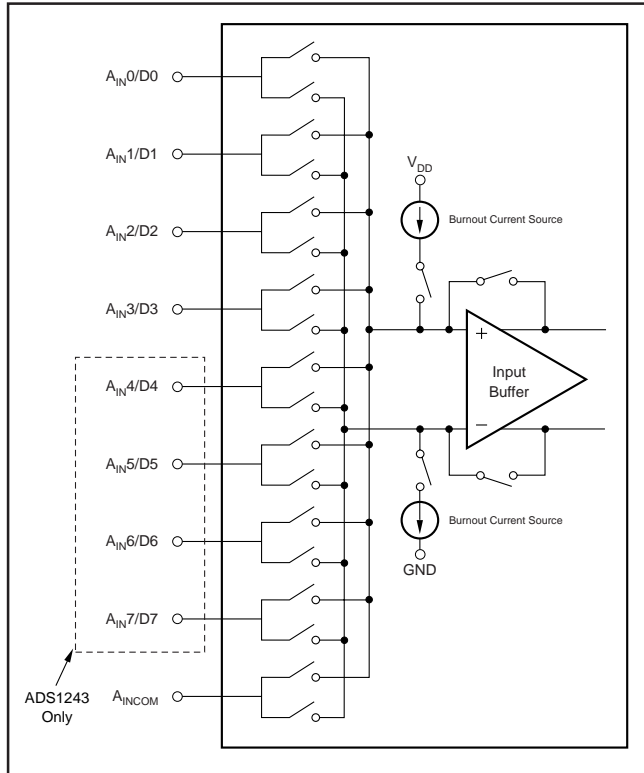


FIGURE 1. Input Multiplexer Configuration.

channel. With this method, it is possible to have up to eight single-ended input channels or four independent differential input channels for the ADS1243, and four single-ended input channels or two independent differential input channels for the ADS1242. Note that A_{INCOM} can be treated as an input channel.

The ADS1242 and ADS1243 feature a single-cycle settling digital filter that provides valid data on the first conversion after a new channel selection. In order to minimize the settling error, synchronize MUX changes to the conversion beginning, which is indicated by the falling edge of \overline{DRDY} . In other words, issuing a MUX change through the WREG command immediately after \overline{DRDY} goes LOW minimizes the settling error. Increasing the time between the conversion beginning (\overline{DRDY} goes LOW) and the MUX change command (t_{DELAY}) results in a settling error in the conversion data, as shown in Figure 2.

BURNOUT CURRENT SOURCES

The Burnout Current Sources can be used to detect sensor short-circuit or open-circuit conditions. Setting the Burnout Current Sources (BOCS) bit in the SETUP register activates two $2\mu A$ current sources called burnout current sources. One of the current sources is connected to the converter's negative input and the other is connected to the converter's positive input.

Figure 3 shows the situation for an open-circuit sensor. This is a potential failure mode for many kinds of remotely connected sensors. The current source on the positive input acts as a pull-up, causing the positive input to go to the positive analog supply, and the current source on the negative input acts as a pull-down, causing the negative input to go to ground. The ADS1242/43 therefore outputs full-scale (7FFFF Hex).

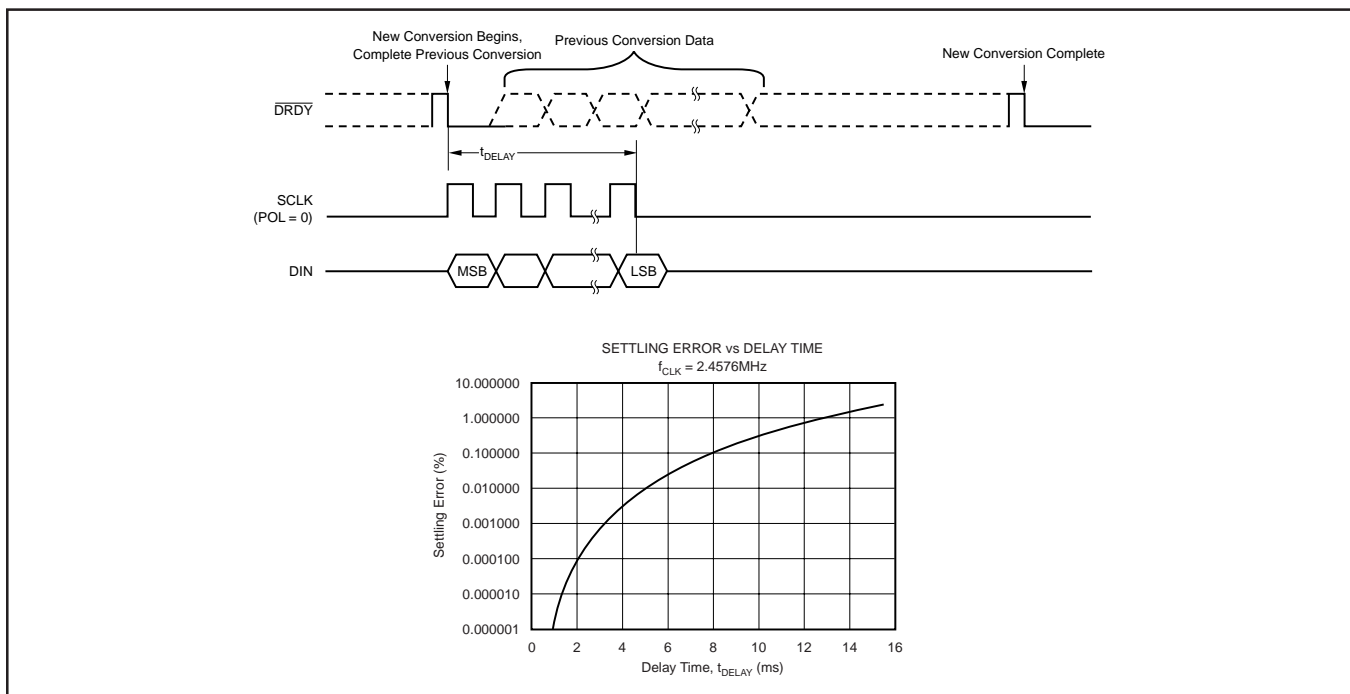


FIGURE 2. Input Multiplexer Configuration.

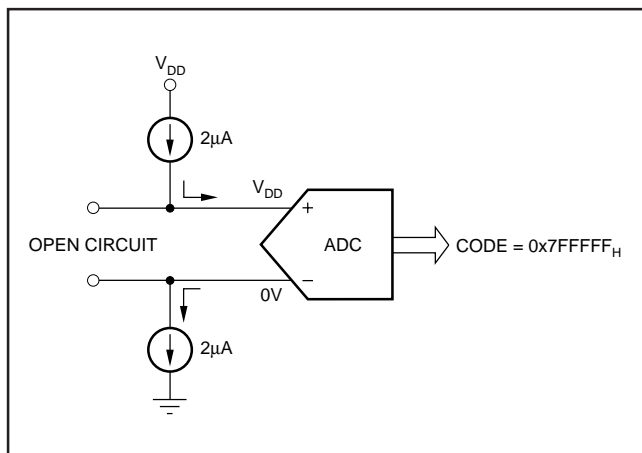


FIGURE 3. Burnout detection while sensor is open-circuited.

Figure 4 shows a short-circuited sensor. Since the inputs are shorted and at the same potential, the ADS1242/43 signal outputs are approximately zero. (Note that the code for shorted inputs is not exactly zero due to internal series resistance, low-level noise and other error sources.)

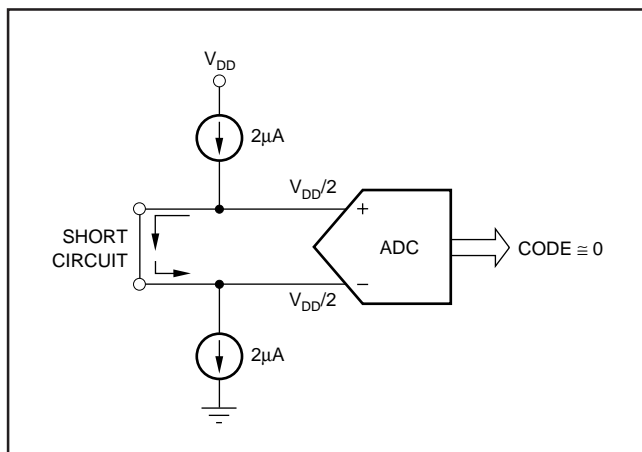


FIGURE 4. Burnout detection while sensor is short-circuited.

INPUT BUFFER

The input impedance of the ADS1242/43 without the buffer enabled is approximately $5M\Omega/PGA$. For systems requiring very high input impedance, the ADS1242/43 provides a chopper-stabilized differential FET-input voltage buffer. When activated, the buffer raises the ADS1242/43 input impedance to approximately $5G\Omega$.

The buffer's input range is approximately 50mV to $V_{DD} - 1.5V$. The buffer's linearity will degrade beyond this range. Differential signals should be adjusted so that both signals are within the buffer's input range.

The buffer can be enabled using the BUFEN pin or the BUFEN bit in the ACR register. The buffer is on when the BUFEN pin is high and the BUFEN bit is set to one. If the BUFEN pin is low, the buffer is disabled. If the BUFEN bit is set to zero, the buffer is also disabled.

The buffer draws additional current when activated. The current required by the buffer depends on the PGA setting. When the PGA is set to 1, the buffer uses approximately $50\mu A$; when the PGA is set to 128, the buffer uses approximately $500\mu A$.

PGA

The Programmable Gain Amplifier (PGA) can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Using the PGA can improve the effective resolution of the A/D converter. For instance, with a PGA of 1 on a 5V full-scale signal, the A/D converter can resolve down to $1\mu V$. With a PGA of 128 and a full-scale signal of 39mV, the A/D converter can resolve down to $75nV$. V_{DD} current increases with PGA settings higher than 4.

OFFSET DAC

The input to the PGA can be shifted by half the full-scale input range of the PGA using the Offset DAC (ODAC) register. The ODAC register is an 8-bit value; the MSB is the sign and the seven LSBs provide the magnitude of the offset. Using the offset DAC does not reduce the performance of the A/D converter. For more details on the ODAC in the ADS1242/43, please refer to TI application report SBAA077 (available through the TI website).

MODULATOR

The modulator is a single-loop second-order system. The modulator runs at a clock speed (f_{MOD}) that is derived from the external clock (f_{OSC}). The frequency division is determined by the SPEED bit in the SETUP register, as shown in Table I.

| f_{OSC} | SPEED BIT | f_{MOD} | DR BITS | | | 1st NOTCH FREQ. |
|-----------|-----------|-----------|---------|--------|---------|-----------------|
| | | | 00 | 01 | 10 | |
| 2.4576MHz | 0 | 19,200Hz | 15Hz | 7.5Hz | 3.75Hz | 50/60Hz |
| | 1 | 9,600Hz | 7.5Hz | 3.75Hz | 1.875Hz | 25/30Hz |
| 4.9152MHz | 0 | 38,400Hz | 30Hz | 15Hz | 7.5Hz | 100/120Hz |
| | 1 | 19,200Hz | 15Hz | 7.5Hz | 3.75Hz | 50/60Hz |

TABLE I. Output Configuration.

CALIBRATION

The offset and gain errors can be minimized with calibration. The ADS1242 and ADS1243 support both self and system calibration.

Self-calibration of the ADS1242 and ADS1243 corrects internal offset and gain errors and is handled by three commands: SELFCAL, SELFGAL, and SELFOCAL. The SELFCAL command performs both an offset and gain calibration. SELFGAL performs a gain calibration and SELFOCAL performs an offset calibration, each of which takes two t_{DATA} periods to complete. During self-calibration, the ADC inputs are disconnected internally from the input pins. The PGA must be set to 1 prior to issuing a SELFCAL or SELFGAL command. Any PGA is allowed when issuing a SELFOCAL command. For

example, if using $PGA = 64$, first set $PGA = 1$ and issue `SELFGCAL`. Afterwards, set $PGA = 64$ and issue `SELFOCAL`. For operation with a reference voltage greater than $(V_{DD} - 1.5)$ volts, the buffer must also be turned off during gain self-calibration to avoid exceeding the buffer input range.

System calibration corrects both internal and external offset and gain errors. While performing system calibration, the appropriate signal must be applied to the inputs. The system offset calibration command (`YSOCAL`) requires a zero input differential signal (see Table IV, page 18). It then computes the offset that nullifies the offset in the system. The system gain calibration command (`YSGCAL`) requires a positive full-scale input signal. It then computes a value to nullify the gain error in the system. Each of these calibrations takes two t_{DATA} periods to complete. System gain calibration is recommended for the best gain calibration at higher PGAs.

Calibration should be performed after power on, a change in temperature, or a change of the PGA. The `RANGE` bit (ACR bit 2) must be zero during calibration.

Calibration removes the effects of the ODAC; therefore, disable the ODAC during calibration, and enable again after calibration is complete.

At the completion of calibration, the \overline{DRDY} signal goes low, indicating the calibration is finished. The first data after calibration should be discarded since it may be corrupt from calibration data remaining in the filter. The second data is always valid.

EXTERNAL VOLTAGE REFERENCE

The ADS1242 and ADS1243 require an external voltage reference. The selection for the voltage reference value is made through the ACR register.

The external voltage reference is differential and is represented by the voltage difference between the pins: $+V_{REF}$ and $-V_{REF}$. The absolute voltage on either pin, $+V_{REF}$ or $-V_{REF}$, can range from GND to V_{DD} . However, the following limitations apply:

For $V_{DD} = 5.0V$ and `RANGE = 0` in the ACR, the differential V_{REF} must not exceed 2.5V.

For $V_{DD} = 5.0V$ and `RANGE = 1` in the ACR, the differential V_{REF} must not exceed 5V.

For $V_{DD} = 3.0V$ and `RANGE = 0` in the ACR, the differential V_{REF} must not exceed 1.25V.

For $V_{DD} = 3.0V$ and `RANGE = 1` in the ACR, the differential V_{REF} must not exceed 2.5V.

CLOCK GENERATOR

The clock source for the ADS1242 and ADS1243 can be provided from a crystal, oscillator, or external clock. When the clock source is a crystal, external capacitors must be provided to ensure start-up and stable clock frequency. This is shown in both Figure 5 and Table II. X_{OUT} is only for use with external crystals and it should not be used as a clock driver for external circuitry.

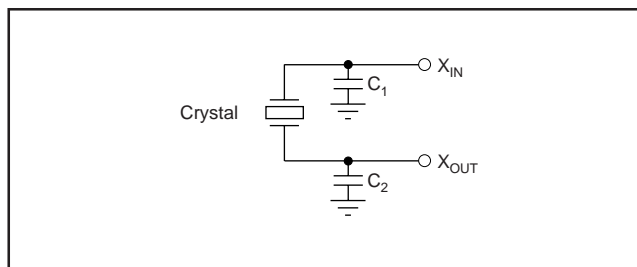


FIGURE 5. Crystal Connection.

| CLOCK SOURCE | FREQUENCY | C ₁ | C ₂ | PART NUMBER |
|--------------|-----------|----------------|----------------|---------------------|
| Crystal | 2.4576 | 0-20pF | 0-20pF | ECS, ECSD 2.45 - 32 |
| Crystal | 4.9152 | 0-20pF | 0-20pF | ECS, ECSL 4.91 |
| Crystal | 4.9152 | 0-20pF | 0-20pF | ECS, ECS4 4.91 |
| Crystal | 4.9152 | 0-20pF | 0-20pF | CTS, MP 042 4M9182 |

TABLE II. Recommended Crystals.

DIGITAL FILTER

The ADS1242 and ADS1243 have a 1279 tap linear phase Finite Impulse Response (FIR) digital filter that a user can configure for various output data rates. When a 2.4576MHz crystal is used, the device can be programmed for an output data rate of 15Hz, 7.5Hz, or 3.75Hz. Under these conditions, the digital filter rejects both 50Hz and 60Hz interference. Figure 6 shows the digital filter frequency response for data output rates of 15Hz, 7.5Hz, and 3.75Hz.

If a different data output rate is desired, a different crystal frequency can be used. However, the rejection frequencies shift accordingly. For example, a 3.6864MHz master clock with the default register condition has:

$$(3.6864\text{MHz}/2.4576\text{MHz}) \cdot 15\text{Hz} = 22.5\text{Hz data output rate}$$

and the first and second notch is:

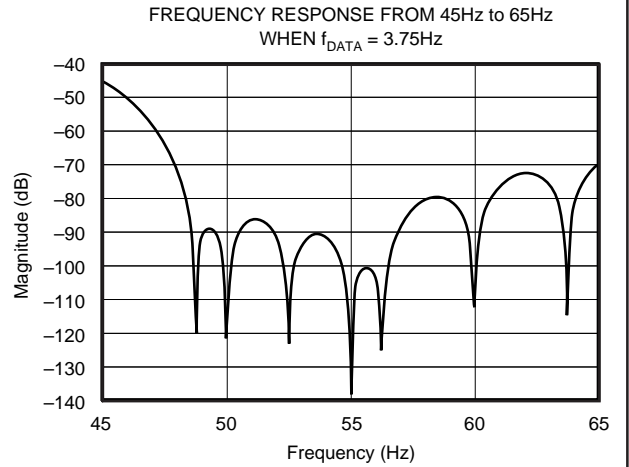
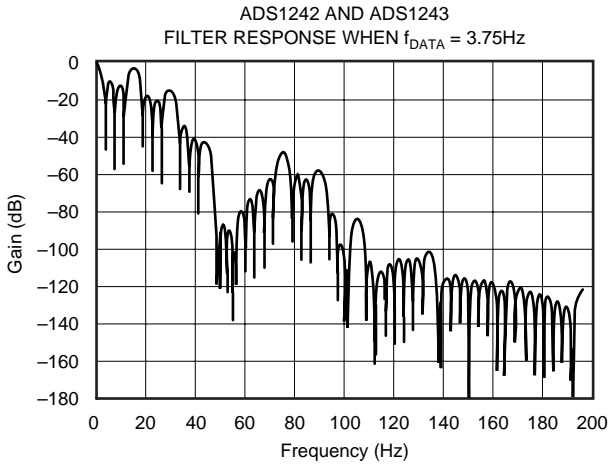
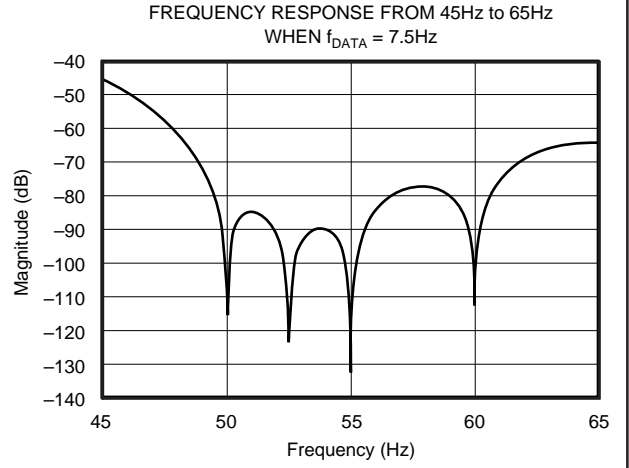
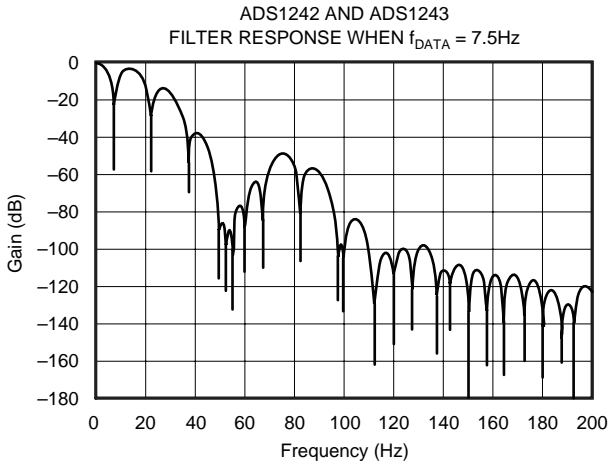
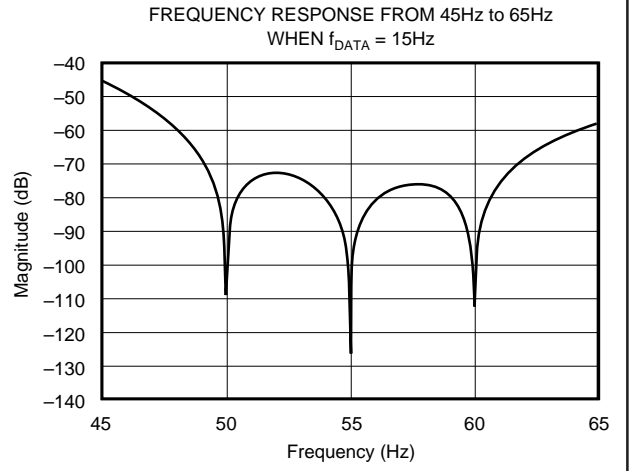
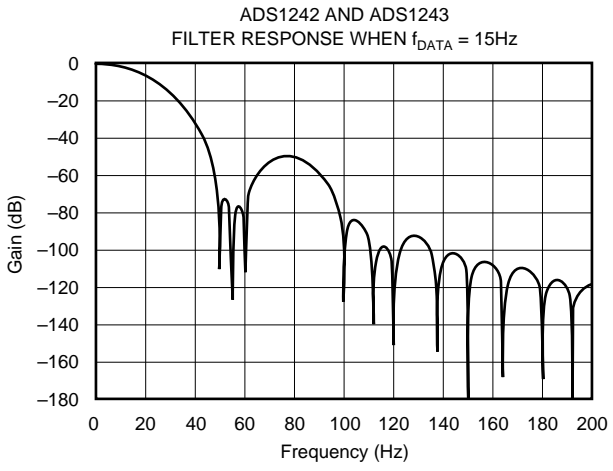
$$1.5 \cdot (50\text{Hz and } 60\text{Hz}) = 75\text{Hz and } 90\text{Hz}$$

DATA I/O INTERFACE

The ADS1242 has four pins and the ADS1243 has eight pins that serve a dual purpose as both analog inputs and data I/O. These pins are configured through the IOCON, DIR, and DIO registers and can be individually configured as either analog inputs or data I/O. See Figure 7 (page 14) for the equivalent schematic of an Analog/Data I/O pin.

The IOCON register defines the pin as either an analog input or data I/O. The power-up state is an analog input. If the pin is configured as an analog input in the IOCON register, the DIR and DIO registers have no effect on the state of the pin.

If the pin is configured as data I/O in the IOCON register, then DIR and DIO are used to control the state of the pin. The DIR register controls the direction of the data pin, either as an input or output. If the pin is configured as an input in the DIR register, then the corresponding DIO register bit reflects the state of the pin. Make sure the pin is driven to a logic one or zero when configured as an input to prevent



$f_{OSC} = 2.4576\text{MHz}$, SPEED = 0 or $f_{OSC} = 4.9152\text{MHz}$, SPEED = 1

| DATA OUTPUT RATE | -3dB BANDWIDTH | ATTENUATION | | | |
|------------------|----------------|--------------------------------|--------------------------------|------------------------------|------------------------------|
| | | $f_{IN} = 50 \pm 0.3\text{Hz}$ | $f_{IN} = 60 \pm 0.3\text{Hz}$ | $f_{IN} = 50 \pm 1\text{Hz}$ | $f_{IN} = 60 \pm 1\text{Hz}$ |
| 15Hz | 14.6Hz | -80.8dB | -87.3dB | -68.5dB | -76.1dB |
| 7.5Hz | 3.44Hz | -85.9dB | -87.4dB | -71.5dB | -76.2dB |
| 3.75Hz | 1.65Hz | -93.8dB | -88.6dB | -86.8dB | -77.3dB |

FIGURE 6. Filter Frequency Responses.

excess current dissipation. If the pin is configured as an output in the DIR register, then the corresponding DIO register bit value determines the state of the output pin (0 = GND, 1 = V_{DD}).

It is still possible to perform A/D conversions on a pin configured as data I/O. This may be useful as a test mode, where the data I/O pin is driven and an A/D conversion is done on the pin.

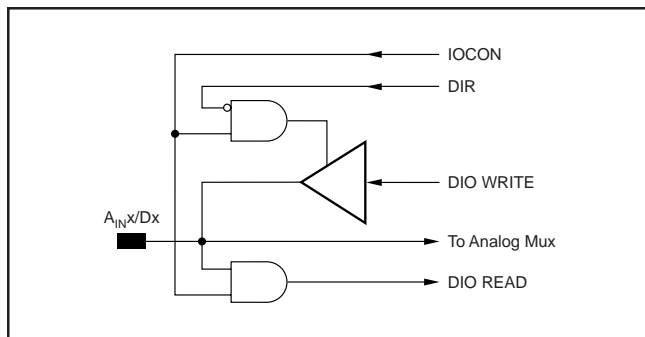


FIGURE 7. Analog/Data Interface Pin.

SERIAL PERIPHERAL INTERFACE

The Serial Peripheral Interface (SPI) allows a controller to communicate synchronously with the ADS1242 and ADS1243. The ADS1242 and ADS1243 operate in slave-only mode. The serial interface is a standard four-wire SPI (\overline{CS} , SCLK, D_{IN} and D_{OUT}) interface.

Chip Select (\overline{CS})

The chip select (\overline{CS}) input must be externally asserted before communicating with the ADS1242 or ADS1243. \overline{CS} must stay LOW for the duration of the communication. Whenever \overline{CS} goes HIGH, the serial interface is reset. \overline{CS} may be hard-wired LOW.

Serial Clock (SCLK)

The serial clock (SCLK) features a Schmitt-triggered input and is used to clock D_{IN} and D_{OUT} data. Make sure to have a clean SCLK to prevent accidental double-shifting of the data. If SCLK is not toggled within three \overline{DRDY} pulses, the

serial interface resets on the next SCLK pulse and starts a new communication cycle. A special pattern on SCLK resets the entire chip; see the RESET section for additional information.

Data Input (D_{IN}) and Data Output (D_{OUT})

The data input (D_{IN}) and data output (D_{OUT}) receive and send data from the ADS1242 and ADS1243. D_{OUT} is high impedance when not in use to allow D_{IN} and D_{OUT} to be connected together and driven by a bidirectional bus. Note: the Read Data Continuous Mode (RDATA) command should not be issued when D_{IN} and D_{OUT} are connected. While in RDATA mode, D_{IN} looks for the STOPC or RESET command. If either of these 8-bit bytes appear on D_{OUT} (which is connected to D_{IN}), the RDATA mode ends.

DATA READY (\overline{DRDY}) PIN

The \overline{DRDY} line is used as a status signal to indicate when data is ready to be read from the internal data register. \overline{DRDY} goes LOW when a new data word is available in the DOR register. It is reset HIGH when a read operation from the data register is complete. It also goes HIGH prior to the updating of the output register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated.

The status of \overline{DRDY} can also be obtained by interrogating bit 7 of the ACR register (address 2_H). The serial interface can operate in 3-wire mode by tying the \overline{CS} input LOW. In this case, the SCLK, D_{IN} , and D_{OUT} lines are used to communicate with the ADS1242 and ADS1243. This scheme is suitable for interfacing to microcontrollers. If \overline{CS} is required as a decoding signal, it can be generated from a port bit of the microcontroller.

POWER-UP—SUPPLY VOLTAGE RAMP RATE

The power-on reset circuitry was designed to accommodate digital supply ramp rates as slow as 1V/10ms. To ensure proper operation, the power supply should ramp monotonically.

ADS1242 AND ADS1243 REGISTERS

The operation of the device is set up through individual registers. Collectively, the registers contain all the information needed to configure the part, such as data format,

multiplexer settings, calibration settings, data rate, etc. The 16 registers are shown in Table III.

| ADDRESS | REGISTER | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|-----------------|----------|--------------------------|--------------------------------|-------|-------|-----------|-------|-------|-------|
| 00 _H | SETUP | ID | ID | ID | ID | BOCS | PGA2 | PGA1 | PGA0 |
| 01 _H | MUX | PSEL3 | PSEL2 | PSEL1 | PSEL0 | NSEL3 | NSEL2 | NSEL1 | NSEL0 |
| 02 _H | ACR | $\overline{\text{DRDY}}$ | $\text{U}/\overline{\text{B}}$ | SPEED | BUFEN | BIT ORDER | RANGE | DR1 | DR0 |
| 03 _H | ODAC | SIGN | OSET6 | OSET5 | OSET4 | OSET3 | OSET2 | OSET1 | OSET0 |
| 04 _H | DIO | DIO_7 | DIO_6 | DIO_5 | DIO_4 | DIO_3 | DIO_2 | DIO_1 | DIO_0 |
| 05 _H | DIR | DIR_7 | DIR_6 | DIR_5 | DIR_4 | DIR_3 | DIR_2 | DIR_1 | DIR_0 |
| 06 _H | IOCON | IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 |
| 07 _H | OCR0 | OCR07 | OCR06 | OCR05 | OCR04 | OCR03 | OCR02 | OCR01 | OCR00 |
| 08 _H | OCR1 | OCR15 | OCR14 | OCR13 | OCR12 | OCR11 | OCR10 | OCR09 | OCR08 |
| 09 _H | OCR2 | OCR23 | OCR22 | OCR21 | OCR20 | OCR19 | OCR18 | OCR17 | OCR16 |
| 0A _H | FSR0 | FSR07 | FSR06 | FSR05 | FSR04 | FSR03 | FSR02 | FSR01 | FSR00 |
| 0B _H | FSR1 | FSR15 | FSR14 | FSR13 | FSR12 | FSR11 | FSR10 | FSR09 | FSR08 |
| 0C _H | FSR2 | FSR23 | FSR22 | FSR21 | FSR20 | FSR19 | FSR18 | FSR17 | FSR16 |
| 0D _H | DOR2 | DOR23 | DOR22 | DOR21 | DOR20 | DOR19 | DOR18 | DOR17 | DOR16 |
| 0E _H | DOR1 | DOR15 | DOR14 | DOR13 | DOR12 | DOR11 | DOR10 | DOR09 | DOR08 |
| 0F _H | DOR0 | DOR07 | DOR16 | FSR21 | DOR04 | DOR03 | DOR02 | DOR01 | DOR00 |

TABLE III. Registers.

DETAILED REGISTER DEFINITIONS

SETUP (Address 00_H) Setup Register

Reset Value = iiiii0000

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ID | ID | ID | ID | BOCS | PGA2 | PGA1 | PGA0 |

bit 7-4 Factory Programmed Bits

bit 3 BOCS: Burnout Current Source
0 = Disabled (default)
1 = Enabled

bit 2-0 PGA2: PGA1: PGA0: Programmable Gain Amplifier Gain Selection
000 = 1 (default)
001 = 2
010 = 4
011 = 8
100 = 16
101 = 32
110 = 64
111 = 128

MUX (Address 01_H) Multiplexer Control Register

Reset Value = 01_H

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PSEL3 | PSEL2 | PSEL1 | PSEL0 | NSEL3 | NSEL2 | NSEL1 | NSEL0 |

bit 7-4 PSEL3: PSEL2: PSEL1: PSEL0: Positive Channel Select

0000 = A_{IN}0 (default)

0001 = A_{IN}1

0010 = A_{IN}2

0011 = A_{IN}3

0100 = A_{IN}4

0101 = A_{IN}5

0110 = A_{IN}6

0111 = A_{IN}7

1xxx = AINCOM (except when xxx = 111)

1111 = Reserved

bit 3-0 NSEL3: NSEL2: NSEL1: NSEL0: Negative Channel Select

0000 = A_{IN}0

0001 = A_{IN}1 (default)

0010 = A_{IN}2

0011 = A_{IN}3

0100 = A_{IN}4

0101 = A_{IN}5

0110 = A_{IN}6

0111 = A_{IN}7

1xxx = AINCOM (except when xxx = 111)

1111 = Reserved

ACR (Address 02_H) Analog Control RegisterReset Value = X0_H

| | | | | | | | |
|-------|-------|-------|-------|-----------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| DRDY | U/B | SPEED | BUFEN | BIT ORDER | RANGE | DR1 | DR0 |

bit 7 **DRDY: Data Ready (Read Only)**
This bit duplicates the state of the DRDY pin.

bit 6 **U/B: Data Format**
0 = Bipolar (default)
1 = Unipolar

| U/B | ANALOG INPUT | DIGITAL OUTPUT (Hex) |
|-----|--------------|----------------------|
| 0 | +FSR | 0x7FFFFFFF |
| | Zero | 0x000000 |
| | -FSR | 0x800000 |
| 1 | +FSR | 0xFFFFFFFF |
| | Zero | 0x000000 |
| | -FSR | 0x000000 |

bit 5 **SPEED: Modulator Clock Speed**

0 = $f_{MOD} = f_{OSC}/128$ (default)
1 = $f_{MOD} = f_{OSC}/256$

bit 4 **BUFEN: Buffer Enable**
0 = Buffer Disabled (default)
1 = Buffer Enabled

bit 3 **BIT ORDER: Data Output Bit Order**
0 = Most Significant Bit Transmitted First (default)
1 = Least Significant Bit Transmitted First
Data is always shifted in or out MSB first.

bit 2 **RANGE: Range Select**
0 = Full-Scale Input Range equal to $\pm V_{REF}$ (default).
1 = Full-Scale Input Range equal to $\pm 1/2 V_{REF}$

NOTE: This allows reference voltages as high as V_{DD} , but even with a 5V reference voltage the calibration must be performed with this bit set to 0.

bit 1-0 **DR1: DR0: Data Rate**
($f_{OSC} = 2.4576\text{MHz}$, $SPEED = 0$)
00 = 15Hz (default)
01 = 7.5Hz
10 = 3.75Hz
11 = Reserved

ODAC (Address 03) Offset DACReset Value = 00_H

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| SIGN | OSET6 | OSET5 | OSET4 | OSET3 | OSET2 | OSET1 | OSET0 |

bit 7 **Sign**
0 = Positive
1 = Negative

$$\text{Offset} = \frac{V_{REF}}{2 \cdot \text{PGA}} \cdot \left(\frac{\text{OSET}[6:0]}{127} \right) \quad \text{RANGE} = 0$$

$$\text{Offset} = \frac{V_{REF}}{4 \cdot \text{PGA}} \cdot \left(\frac{\text{OSET}[6:0]}{127} \right) \quad \text{RANGE} = 1$$

NOTE: The offset DAC must be enabled after calibration or the calibration nullifies the effects.

DIO (Address 04_H) Data I/OReset Value = 00_H

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| DIO7 | DIO6 | DIO5 | DIO4 | DIO3 | DIO2 | DIO1 | DIO0 |

If the IOCON register is configured for data, a value written to this register appears on the data I/O pins if the pin is configured as an output in the DIR register. Reading this register returns the value of the data I/O pins.

Bits 4 to 7 are not used in ADS1242.

DIR (Address 05_H) Direction Control for Data I/OReset Value = FF_H

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| DIR7 | DIR6 | DIR5 | DIR4 | DIR3 | DIR2 | DIR1 | DIR0 |

Each bit controls whether the corresponding data I/O pin is an output (= 0) or input (= 1). The default power-up state is as inputs.

Bits 4 to 7 are not used in ADS1242.

IOCON (Address 06_H) I/O Configuration RegisterReset Value = 00_H

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 |

bit 7-0 **IO7: IO0: Data I/O Configuration**
0 = Analog (default)
1 = Data

Configuring the pin as a data I/O pin allows it to be controlled through the DIO and DIR registers.

Bits 4 to 7 are not used in ADS1242.

OCR0 (Address 07_H) Offset Calibration Coefficient

(Least Significant Byte)

Reset Value = 00_H

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| OCR07 | OCR06 | OCR05 | OCR04 | OCR03 | OCR02 | OCR01 | OCR00 |

OCR1 (Address 08_H) Offset Calibration Coefficient
(Middle Byte)

Reset Value = 00_H

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| OCR15 | OCR14 | OCR13 | OCR12 | OCR11 | OCR10 | OCR09 | OCR08 |

OCR2 (Address 09_H) Offset Calibration Coefficient
(Most Significant Byte)

Reset Value = 00_H

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| OCR23 | OCR22 | OCR21 | OCR20 | OCR19 | OCR18 | OCR17 | OCR16 |

FSR0 (Address 0A_H) Full-Scale Register
(Least Significant Byte)

Reset Value = 59_H

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| FSR07 | FSR06 | FSR05 | FSR04 | FSR03 | FSR02 | FSR01 | FSR00 |

FSR1 (Address 0B_H) Full-Scale Register
(Middle Byte)

Reset Value = 55_H

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| FSR15 | FSR14 | FSR13 | FSR12 | FSR11 | FSR10 | FSR09 | FSR08 |

FSR2 (Address 0C_H) Full-Scale Register
(Most Significant Byte)

Reset Value = 55_H

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| FSR23 | FSR22 | FSR21 | FSR20 | FSR19 | FSR18 | FSR17 | FSR16 |

DOR2 (Address 0D_H) Data Output Register
(Most Significant Byte) (Read Only)

Reset Value = 00_H

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| DOR23 | DOR22 | DOR21 | DOR20 | DOR19 | DOR18 | DOR17 | DOR16 |

DOR1 (Address 0E_H) Data Output Register
(Middle Byte) (Read Only)

Reset Value = 00_H

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| DOR15 | DOR14 | DOR13 | DOR12 | DOR11 | DOR10 | DOR09 | DOR08 |

DOR0 (Address 0F_H) Data Output Register
(Least Significant Byte) (Read Only)

Reset Value = 00_H

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| DOR07 | DOR06 | DOR05 | DOR04 | DOR03 | DOR02 | DOR01 | DOR00 |

ADS1242 AND ADS1243 CONTROL COMMAND DEFINITIONS

The commands listed in Table IV control the operations of the ADS1242 and ADS1243. Some of the commands are stand-alone commands (for example, RESET) while others require additional bytes (for example, WREG requires the count and data bytes).

Operands:

n = count (0 to 127)

r = register (0 to 15)

x = don't care

| COMMANDS | DESCRIPTION | OP CODE | 2nd COMMAND BYTE |
|-----------|-------------------------------|------------------------------|-------------------------|
| RDATA | Read Data | 0000 0001 (01 _H) | — |
| RDATA C | Read Data Continuously | 0000 0011 (03 _H) | — |
| STOPC | Stop Read Data Continuously | 0000 1111 (0F _H) | — |
| RREG | Read from REG "rrrr" | 0001 rrrr (1x _H) | xxxx_nnnn (# of regs-1) |
| WREG | Write to REG "rrrr" | 0101 rrrr (5x _H) | xxxx_nnnn (# of regs-1) |
| SELF CAL | Offset and Gain Self Cal | 1111 0000 (F0 _H) | — |
| SELF OCAL | Self Offset Cal | 1111 0001 (F1 _H) | — |
| SELF GCAL | Self Gain Cal | 1111 0010 (F2 _H) | — |
| SYSOCAL | Sys Offset Cal | 1111 0011 (F3 _H) | — |
| SYS GCAL | Sys Gain Cal | 1111 0100 (F4 _H) | — |
| WAKEUP | Wakeup from SLEEP Mode | 1111 1011 (FB _H) | — |
| DSYNC | Sync $\overline{\text{DRDY}}$ | 1111 1100 (FC _H) | — |
| SLEEP | Put in SLEEP Mode | 1111 1101 (FD _H) | — |
| RESET | Reset to Power-Up Values | 1111 1110 (FE _H) | — |

NOTE: The received data format is always MSB first; the data out format is set by the BIT ORDER bit in the ACR register.

TABLE IV. Command Summary.

RDATA—Read Data

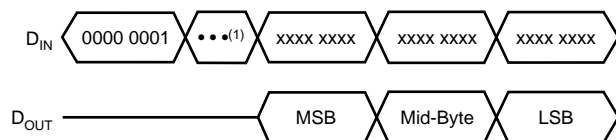
Description: Read the most recent conversion result from the Data Output Register (DOR). This is a 24-bit value.

Operands: None

Bytes: 1

Encoding: 0000 0001

Data Transfer Sequence:



NOTE: (1) For wait time, refer to timing specification.

RDATA C—Read Data Continuous

Description: Read Data Continuous mode enables the continuous output of new data on each $\overline{\text{DRDY}}$. This command eliminates the need to send the Read Data Command on each $\overline{\text{DRDY}}$. This mode may be terminated by either the STOPC command or the RESET command. Wait at least 10 f_{OSC} after $\overline{\text{DRDY}}$ falls before reading.

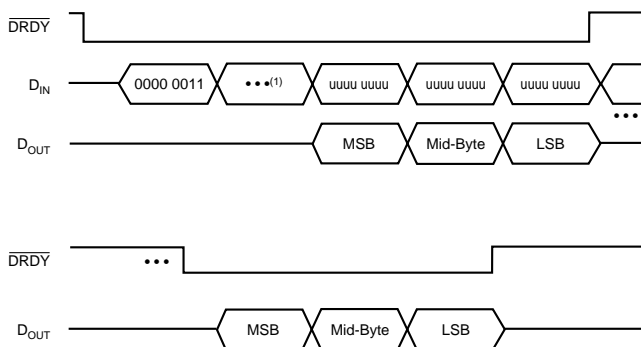
Operands: None

Bytes: 1

Encoding: 0000 0011

Data Transfer Sequence:

Command terminated when "uuuu uuuu" equals STOPC or RESET.



NOTE: (1) For wait time, refer to timing specification.

STOPC–Stop Continuous

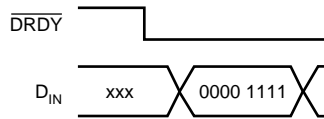
Description: Ends the continuous data output mode. Issue after DRDY goes LOW.

Operands: None

Bytes: 1

Encoding: 0000 1111

Data Transfer Sequence:



RREG–Read from Registers

Description: Output the data from up to 16 registers starting with the register address specified as part of the instruction. The number of registers read will be one plus the second byte count. If the count exceeds the remaining registers, the addresses wrap back to the beginning.

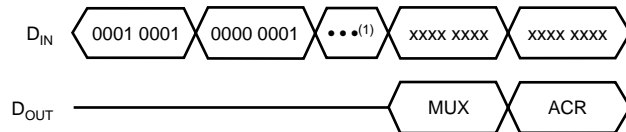
Operands: r, n

Bytes: 2

Encoding: 0001 rrrr xxxx nnnn

Data Transfer Sequence:

Read Two Registers Starting from Register 01_H (MUX)



NOTE: (1) For wait time, refer to timing specification.

WREG–Write to Registers

Description: Write to the registers starting with the register address specified as part of the instruction. The number of registers that will be written is one plus the value of the second byte.

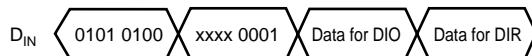
Operands: r, n

Bytes: 2

Encoding: 0101 rrrr xxxx nnnn

Data Transfer Sequence:

Write Two Registers Starting from 04_H (DIO)



SELFAL–Offset and Gain Self Calibration

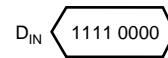
Description: Starts the process of self calibration. The Offset Calibration Register (OCR) and the Full-Scale Register (FSR) are updated with new values after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0000

Data Transfer Sequence:



SELFOCAL–Offset Self Calibration

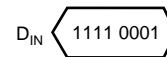
Description: Starts the process of self-calibration for offset. The Offset Calibration Register (OCR) is updated after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0001

Data Transfer Sequence:



SELFGCAL–Gain Self Calibration

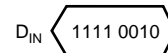
Description: Starts the process of self-calibration for gain. The Full-Scale Register (FSR) is updated with new values after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0010

Data Transfer Sequence:



SYSOCAL—System Offset Calibration

Description: Initiates a system offset calibration. The input should be set to 0V, and the ADS1242 and ADS1243 compute the OCR value that compensates for offset errors. The Offset Calibration Register (OCR) is updated after this operation. The user must apply a zero input signal to the appropriate analog inputs. The OCR register is automatically updated afterwards.

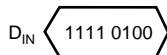
Operands: None
Bytes: 1
Encoding: 1111 0011
Data Transfer Sequence:



SYSGCAL—System Gain Calibration

Description: Starts the system gain calibration process. For a system gain calibration, the input should be set to the reference voltage and the ADS1242 and ADS1243 compute the FSR value that will compensate for gain errors. The FSR is updated after this operation. To initiate a system gain calibration, the user must apply a full-scale input signal to the appropriate analog inputs. FCR register is updated automatically.

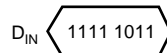
Operands: None
Bytes: 1
Encoding: 1111 0100
Data Transfer Sequence:



WAKEUP

Description: Wakes the ADS1242 and ADS1243 from SLEEP mode.

Operands: None
Bytes: 1
Encoding: 1111 1011
Data Transfer Sequence:



DSYNC—Sync $\overline{\text{DRDY}}$

Description: Synchronizes the ADS1242 and ADS1243 to an external event.

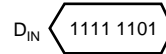
Operands: None
Bytes: 1
Encoding: 1111 1100
Data Transfer Sequence:



SLEEP—Sleep Mode

Description: Puts the ADS1242 and ADS1243 into a low power sleep mode. To exit sleep mode, issue the WAKEUP command.

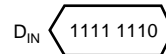
Operands: None
Bytes: 1
Encoding: 1111 1101
Data Transfer Sequence:



RESET—Reset to Default Values

Description: Restore the registers to their power-up values. This command stops the Read Continuous mode.

Operands: None
Bytes: 1
Encoding: 1111 1110
Data Transfer Sequence:



APPLICATION EXAMPLES

GENERAL-PURPOSE WEIGHT SCALE

Figure 8 shows a typical schematic of a general-purpose weight scale application using the ADS1242. In this example, the internal PGA is set to either 64 or 128 (depending on the maximum output voltage of the load cell) so that the

load cell output can be directly applied to the differential inputs of ADS1242.

HIGH PRECISION WEIGHT SCALE

Figure 9 shows the typical schematic of a high-precision weight scale application using the ADS1242. The front-end differential amplifier helps maximize the dynamic range.

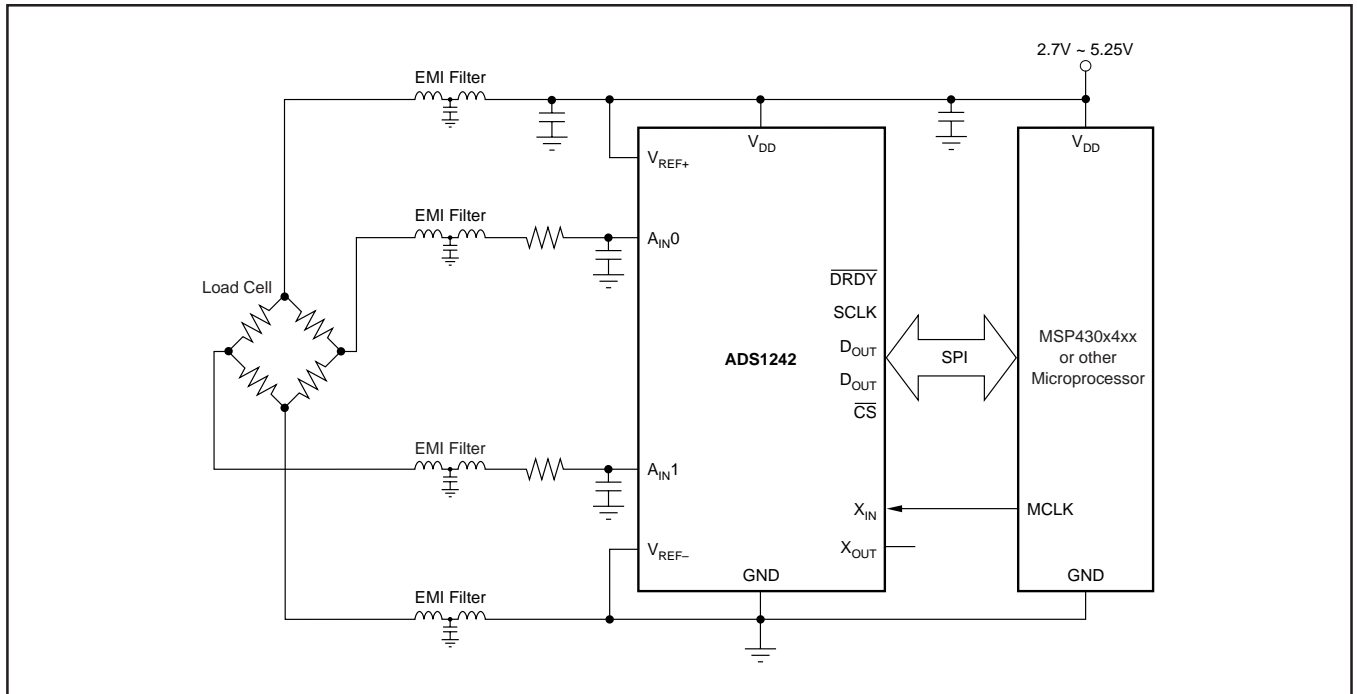


FIGURE 8. Schematic of a General-Purpose Weight Scale.

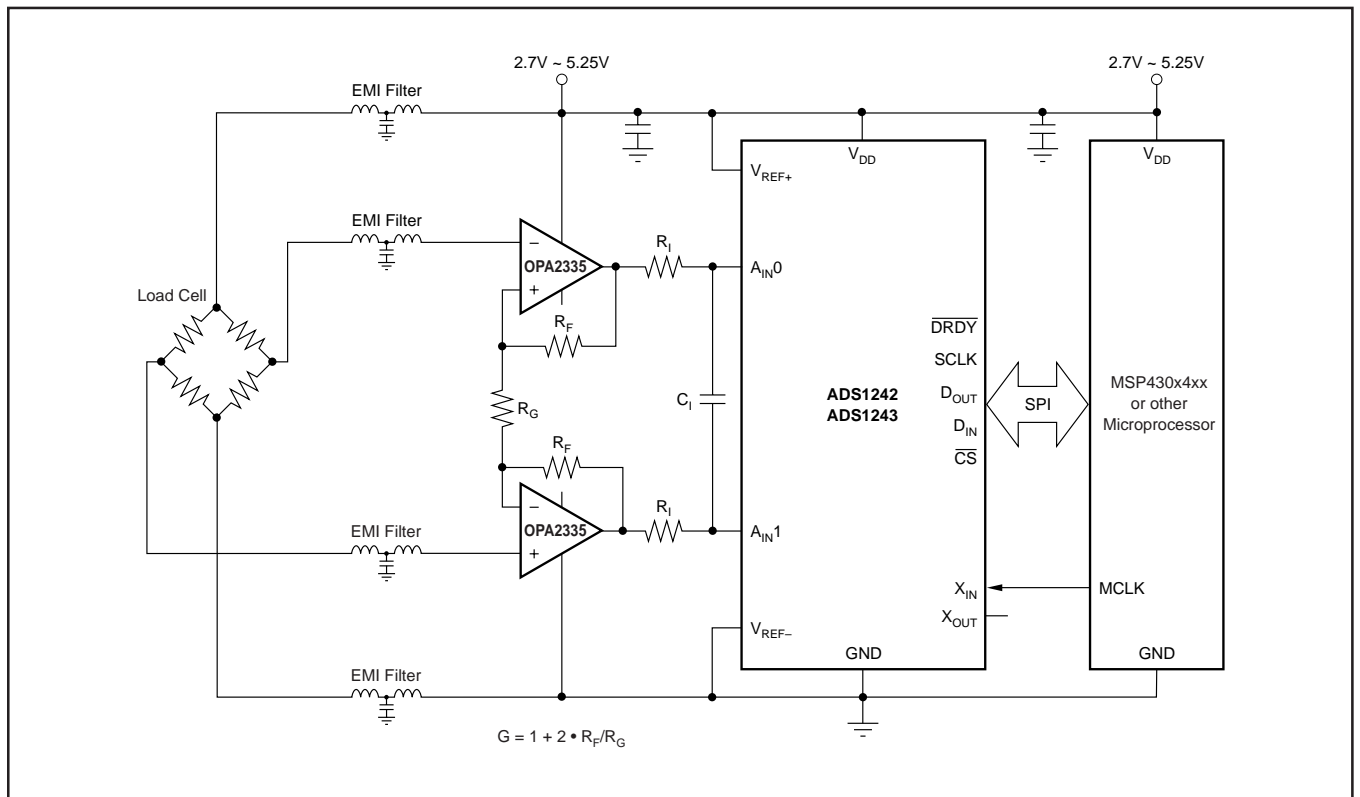


FIGURE 9. Block Diagram for a High-Precision Weight Scale.

DEFINITION OF TERMS

An attempt has been made to be consistent with the terminology used in this data sheet. In that regard, the definition of each term is given as follows:

Analog Input Voltage—the voltage at any one analog input relative to GND.

Analog Input Differential Voltage—given by the following equation: (IN+) – (IN–). Thus, a positive digital output is produced whenever the analog input differential voltage is positive, while a negative digital output is produced whenever the differential is negative.

For example, when the converter is configured with a 2.5V reference and placed in a gain setting of 1, the positive full-scale output is produced when the analog input differential is 2.5V. The negative full-scale output is produced when the differential is –2.5V. In each case, the actual input voltages must remain within the GND to V_{DD} range.

Conversion Cycle—the term *conversion cycle* usually refers to a discrete A/D conversion operation, such as that performed by a successive approximation converter. As used here, a conversion cycle refers to the t_{DATA} time period.

Data Rate—The rate at which conversions are completed. See definition for f_{DATA}.

$$f_{DATA} = \frac{f_{OSC}}{128 \cdot 2^{SPEED} \cdot 1280 \cdot 2^{DR}}$$

SPEED = 0,1
DR = 0,1, 2

f_{OSC}—the frequency of the crystal oscillator or CMOS compatible input signal at the X_{IN} input of the ADS1242 and ADS1243.

f_{MOD}—the frequency or speed at which the modulator of the ADS1242 and ADS1243 is running. This depends on the SPEED bit as given by the following equation:

| | SPEED = 0 | SPEED = 1 |
|---------|-----------|-----------|
| mfactor | 128 | 256 |

$$f_{MOD} = \frac{f_{OSC}}{mfactor} = \frac{f_{OSC}}{128 \cdot 2^{SPEED}}$$

| PGA SETTING | SAMPLING FREQUENCY |
|-------------|--|
| 1, 2, 4, 8 | $f_{SAMP} = \frac{f_{OSC}}{mfactor}$ |
| 16 | $f_{SAMP} = \frac{f_{OSC} \cdot 2}{mfactor}$ |
| 32 | $f_{SAMP} = \frac{f_{OSC} \cdot 4}{mfactor}$ |
| 64, 128 | $f_{SAMP} = \frac{f_{OSC} \cdot 8}{mfactor}$ |

f_{SAMP}—the frequency, or switching speed, of the input sampling capacitor. The value is given by one of the following equations:

f_{DATA}—the frequency of the digital output data produced by the ADS1242 and ADS1243, f_{DATA} is also referred to as the Data Rate.

Full-Scale Range (FSR)—as with most A/D converters, the full-scale range of the ADS1242 and ADS1243 is defined as the input, that produces the positive full-scale digital output minus the input, that produces the negative full-scale digital output.

For example, when the converter is configured with a 2.5V reference and is placed in a gain setting of 2, the full-scale range is: [1.25V (positive full-scale) minus –1.25V (negative full-scale)] = 2.5V.

Least Significant Bit (LSB) Weight—this is the theoretical amount of voltage that the differential voltage at the analog input has to change in order to observe a change in the output data of one least significant bit. It is computed as follows:

$$LSB \text{ Weight} = \frac{\text{Full - Scale Range}}{2^N - 1}$$

where N is the number of bits in the digital output.

t_{DATA}—the inverse of f_{DATA}, or the period between each data output.

| GAIN SETTING | +5V SUPPLY ANALOG INPUT ⁽¹⁾ | | | GENERAL EQUATIONS | | | |
|--------------|--|--|------------------|-------------------|--|-----------------------------------|-----------------------------------|
| | FULL-SCALE RANGE | DIFFERENTIAL INPUT VOLTAGES ⁽²⁾ | PGA OFFSET RANGE | FULL-SCALE RANGE | DIFFERENTIAL INPUT VOLTAGES ⁽²⁾ | PGA SHIFT RANGE | |
| 1 | 5V | ±2.5V | ±1.25V | RANGE = 0 | | | |
| 2 | 2.5V | ±1.25V | ±0.625V | | | | |
| 4 | 1.25V | ±0.625V | ±312.5mV | | | | |
| 8 | 0.625V | ±312.5mV | ±156.25mV | | | | |
| 16 | 312.5mV | ±156.25mV | ±78.125mV | | | | |
| 32 | 156.25mV | ±78.125mV | ±39.0625mV | | | | |
| 64 | 78.125mV | ±39.0625mV | ±19.531mV | RANGE = 1 | $\frac{V_{REF}}{PGA}$ | $\frac{\pm V_{REF}}{2 \cdot PGA}$ | $\frac{\pm V_{REF}}{4 \cdot PGA}$ |
| 128 | 39.0625mV | ±19.531mV | ±9.766mV | | | | |

NOTES: (1) With a +2.5V reference. (2) Refer to electrical specification for analog input voltage range.

TABLE VI. Full-Scale Range versus PGA Setting.

PACKAGING INFORMATION

| ORDERABLE DEVICE | STATUS(1) | PACKAGE TYPE | PACKAGE DRAWING | PINS | PACKAGE QTY |
|------------------|-----------|--------------|-----------------|------|-------------|
| ADS1242IPWR | ACTIVE | TSSOP | PW | 16 | 2500 |
| ADS1242IPWT | ACTIVE | TSSOP | PW | 16 | 250 |
| ADS1243IPWR | ACTIVE | TSSOP | PW | 20 | 2500 |
| ADS1243IPWT | ACTIVE | TSSOP | PW | 20 | 250 |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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