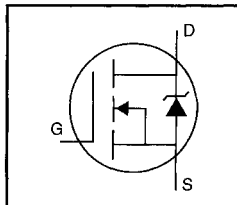


### HEXFET® Power MOSFET

- Dynamic  $dv/dt$  Rating
- Repetitive Avalanche Rated
- Surface Mount (IRLR110)
- Straight Lead (IRLU110)
- Available in Tape & Reel
- Logic-Level Gate Drive
- $R_{DS(on)}$  Specified at  $V_{GS}=4V$  &  $5V$



$$V_{DSS} = 100V$$

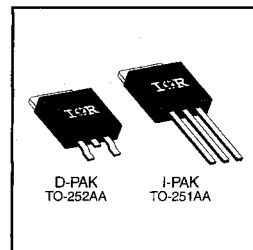
$$R_{DS(on)} = 0.54\Omega$$

$$I_D = 4.3A$$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



DATA SHEETS

### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 5.0 V$	4.3	A
$I_D$ @ $T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 5.0 V$	2.7	
$I_{DM}$	Pulsed Drain Current ①	17	
$P_D$ @ $T_C = 25^\circ C$	Power Dissipation	25	W
$P_D$ @ $T_A = 25^\circ C$	Power Dissipation (PCB Mount)**	2.5	
	Linear Derating Factor	0.20	W/°C
	Linear Derating Factor (PCB Mount)**	0.020	
$V_{GS}$	Gate-to-Source Voltage	$\pm 10$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	100	mJ
$I_{AR}$	Avalanche Current ①	4.3	A
$E_{AR}$	Repetitive Avalanche Energy ①	2.5	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ ③	5.5	V/ns
$T_J, T_{STG}$	Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	260 (1.6mm from case)	


### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	5.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	—	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	—	110	


\*\* When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

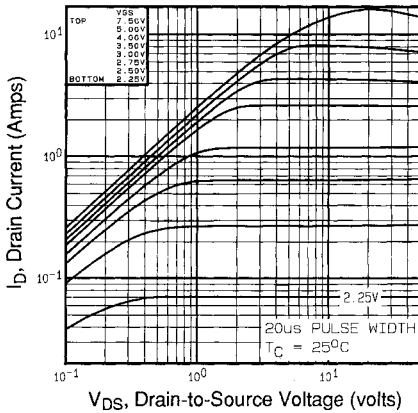
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS}=0\text{V}$ , $I_D=250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.12	—	$\text{V}/^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.54	$\Omega$	$V_{GS}=5.0\text{V}$ , $I_D=2.6\text{A}$ ④
		—	—	0.76		$V_{GS}=4.0\text{V}$ , $I_D=2.2\text{A}$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$
$g_{fs}$	Forward Transconductance	2.3	—	—	S	$V_{DS}=50\text{V}$ , $I_D=2.6\text{A}$ ④
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu\text{A}$	$V_{DS}=100\text{V}$ , $V_{GS}=0\text{V}$
		—	—	250		$V_{DS}=80\text{V}$ , $V_{GS}=0\text{V}$ , $T_J=125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=10\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS}=-10\text{V}$
$Q_g$	Total Gate Charge	—	—	6.1	nC	$I_D=5.6\text{A}$
$Q_{gs}$	Gate-to-Source Charge	—	—	2.0		$V_{DS}=80\text{V}$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	3.3		$V_{GS}=5.0\text{V}$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	9.3	—	ns	$V_{DD}=50\text{V}$
$t_r$	Rise Time	—	47	—		$I_D=5.6\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	16	—		$R_G=12\Omega$
$t_f$	Fall Time	—	17	—		$R_D=8.4\Omega$ See Figure 10 ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	250	—	pF	$V_{GS}=0\text{V}$
$C_{oss}$	Output Capacitance	—	80	—		$V_{DS}=25\text{V}$
$C_{rss}$	Reverse Transfer Capacitance	—	15	—		$f=1.0\text{MHz}$ See Figure 5

## Source-Drain Ratings and Characteristics

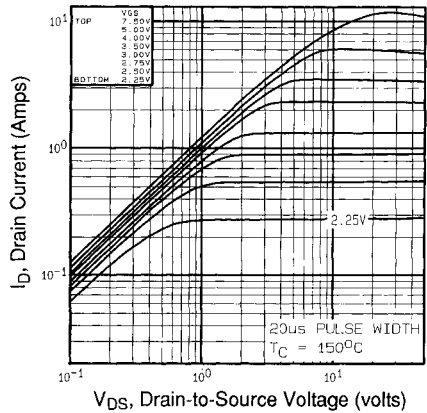
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	4.3	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	17		
$V_{SD}$	Diode Forward Voltage	—	—	2.5	V	$T_J=25^\circ\text{C}$ , $I_S=4.3\text{A}$ , $V_{GS}=0\text{V}$ ④
$t_{rr}$	Reverse Recovery Time	—	100	130	ns	$T_J=25^\circ\text{C}$ , $I_F=5.6\text{A}$
$Q_{rr}$	Reverse Recovery Charge	—	0.50	0.65	$\mu\text{C}$	$di/dt=100\text{A}/\mu\text{s}$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

### Notes:

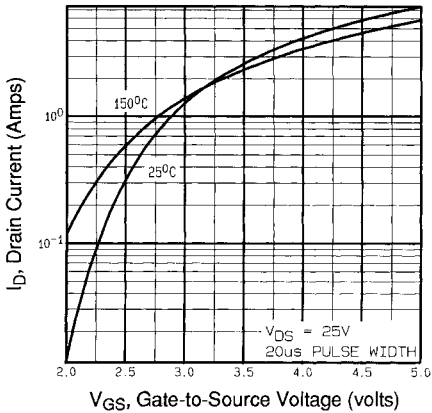
- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ②  $V_{DD}=25\text{V}$ , starting  $T_J=25^\circ\text{C}$ ,  $L=8.1\text{mH}$ ,  $R_G=25\Omega$ ,  $I_{AS}=4.3\text{A}$  (See Figure 12)
- ③  $I_{SD}\leq 5.6\text{A}$ ,  $di/dt\leq 140\text{A}/\mu\text{s}$ ,  $V_{DD}\leq V_{(BR)DSS}$ ,  $T_J\leq 150^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .



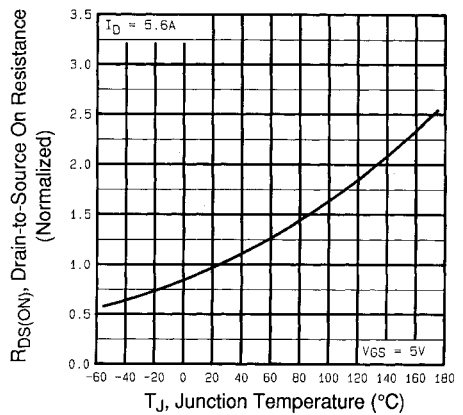
**Fig 1.** Typical Output Characteristics,  
 $T_C = 25^\circ\text{C}$



**Fig 2.** Typical Output Characteristics,  
 $T_C = 150^\circ\text{C}$

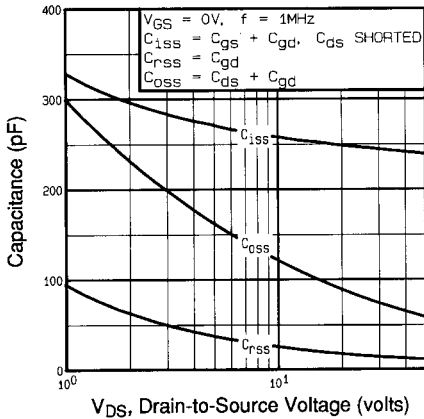


**Fig 3.** Typical Transfer Characteristics

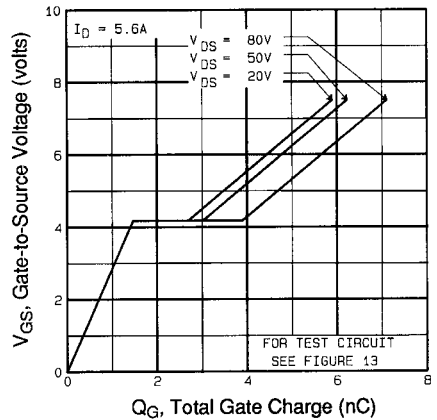


**Fig 4.** Normalized On-Resistance  
Vs. Temperature

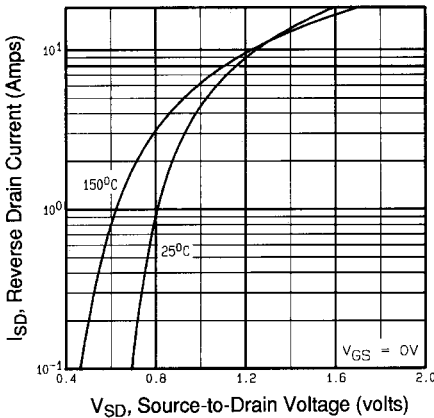
DATA SHEETS



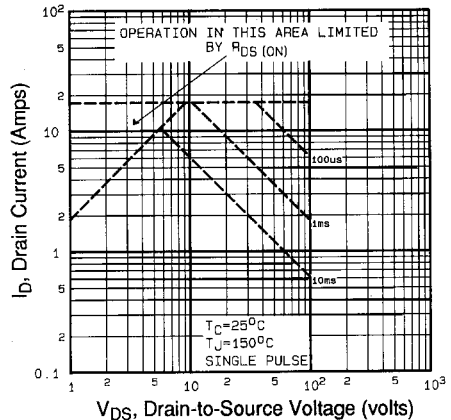
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



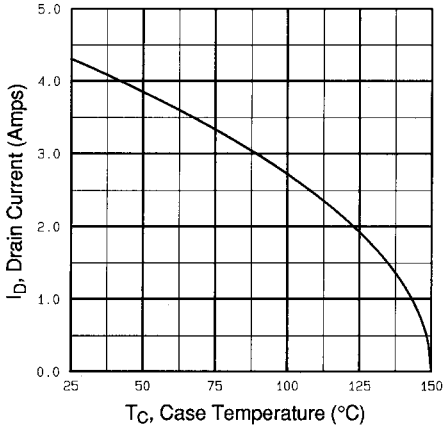
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



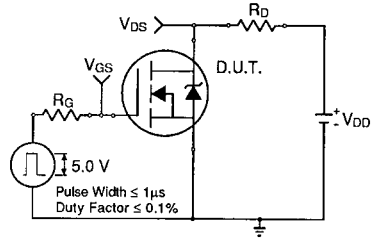
**Fig 7.** Typical Source-Drain Diode Forward Voltage



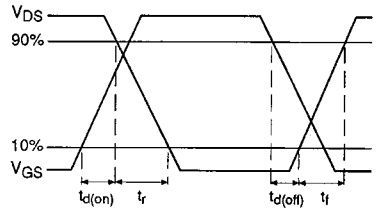
**Fig 8.** Maximum Safe Operating Area



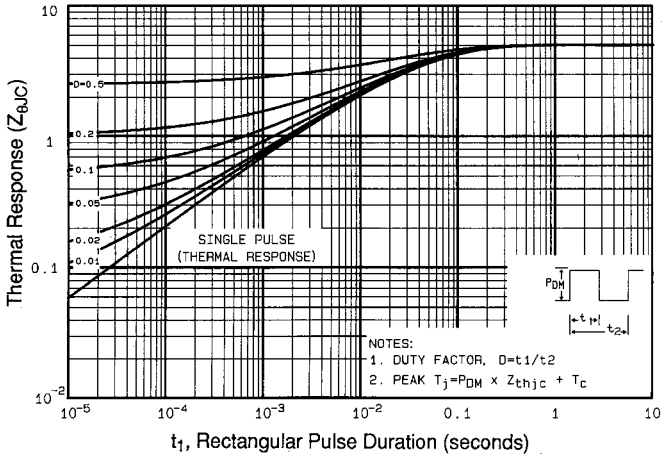
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

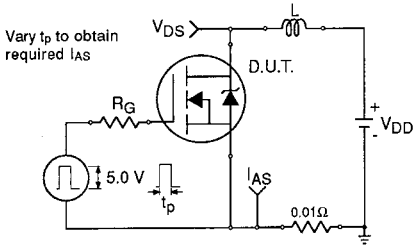


**Fig 10b.** Switching Time Waveforms

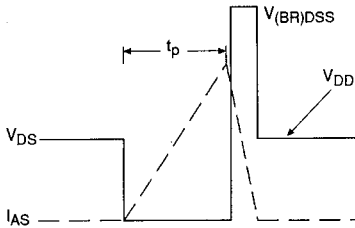


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

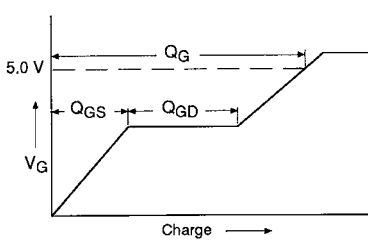
DATA SHEETS



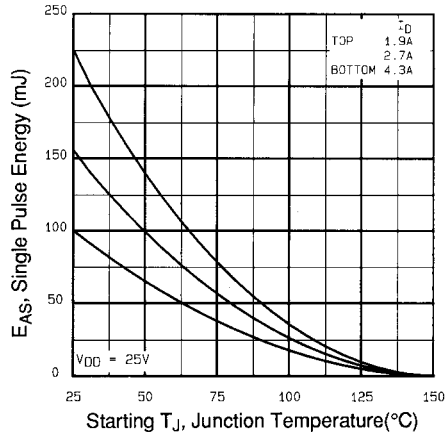
**Fig 12a.** Unclamped Inductive Test Circuit



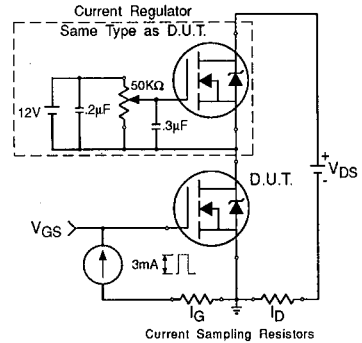
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

**Appendix A:** Figure 14, Peak Diode Recovery  $dv/dt$  Test Circuit – See page 1505

**Appendix B:** Package Outline Mechanical Drawing – See pages 1512, 1513

**Appendix C:** Part Marking Information – See page 1518

**Appendix D:** Tape & Reel Information – See page 1523