National Semiconductor

January 1988

MM54HCT03/MM74HCT03
Quad 2-Input NAND Gate (Open Drain)

General Description

The MM54HCT03/MM74HCT03 are logic functions fabricated by using advanced silicon-gate CMOS technology which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. These devices are input and output characteristic and pinout compatible with standard DM54LS/74LS logic families. All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

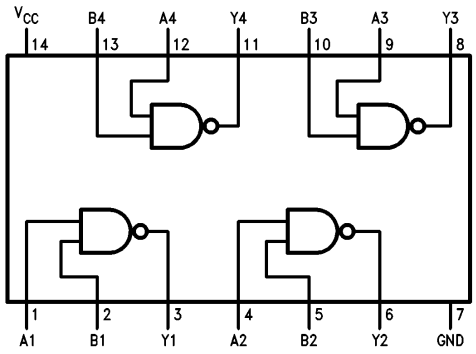
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL, LS pin-out and threshold compatible
- Fast switching: t_{PLH}, t_{PHL} = 12 ns (typ)
- Low power: 10 μW at DC
- High fan-out, 10 LS-TTL loads

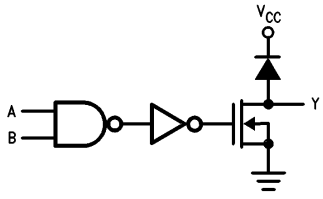
Connection and Logic Diagrams

Dual-In-Line Package



TL/F/9395–1

Order Number MM54HCT03 or MM74HCT03



TL/F/9395–2

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to +85°C	54HCT T_A = −55°C to +125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{LKG}	Minimum High Level Output Leakage Current	V_{IN} = V_{IH} or V_{IL}, V_{OUT} = V_{CC}		0.5	5.0	10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA		2.0	20	40	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		1.2	1.4	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package; −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, t_r = t_f = 6 ns, unless otherwise noted

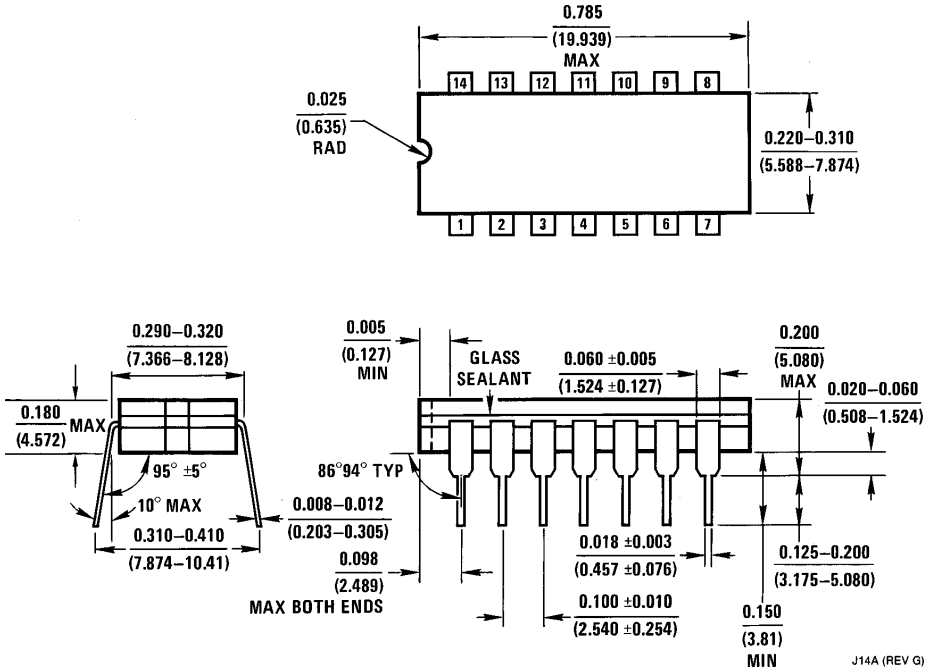
Symbol	Parameter	Conditions	Typ	Units
t_{PZL}	Maximum Propagation Delay	R_L = 1 kΩ	7	ns
t_{PLZ}	Maximum Propagation Delay	R_L = 1 kΩ	10	ns

AC Electrical Characteristics V_{CC} = 5.0V ±10%, C_L = 50 pF, t_r = t_f = 6 ns, unless otherwise specified

Symbol	Parameter	Conditions	T_A = 25°C		74HCT T_A = −40°C to +85°C	54HCT T_A = −55°C to +125°C	Units
			Typ	Guaranteed Limits			
t_{PZL}	Maximum Propagation Delay	R_L = 1 kΩ	10	20	25	30	ns
t_{PLZ}	Maximum Propagation Delay	R_L = 1 kΩ	12	20	25	30	ns
t_{THL}	Maximum Output Fall Time		10	15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate) R_L = ∞		14			pF
C_{IN}	Maximum Input Capacitance			5	10	10	pF

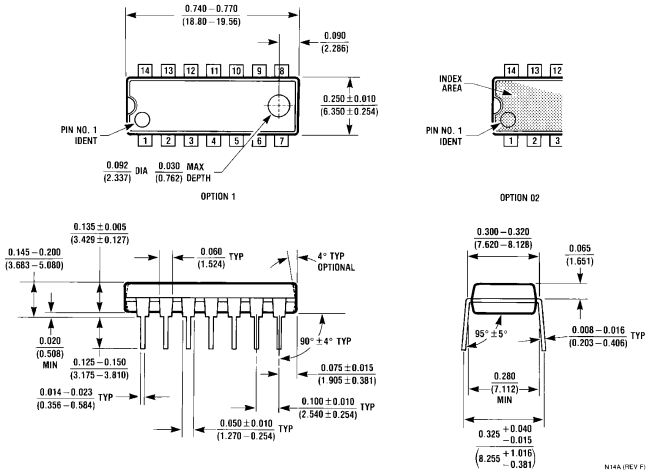
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54HCT03J or MM74HCT03J
NS Package Number J14A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number MM74HCT03N
NS Package Number N14A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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