

# CD74HC147, CD74HCT147

## High Speed CMOS Logic 10-to-4 Line Priority Encoder

September 1997

### Features

- Buffered Inputs and Outputs
- Typical Propagation Delay: 13ns at  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^\circ C$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^\circ C$  to  $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The Harris CD74HC147 and CD74HCT147 are high speed silicon-gate CMOS devices and are pin-compatible with low power Schottky TTL (LSTTL).

The CD74HC147 and CD74HCT147 9-input priority encoders accept data from nine active LOW inputs ( $I_1$  to  $I_9$ ) and provide binary representation on the four active LOW outputs ( $\bar{Y}_0$  to  $\bar{Y}_3$ ). A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line  $I_9$  having the highest priority.

These devices provide the 10-line to 4-line priority encoding function by use of the implied decimal "zero". The "zero" is encoded when all nine data inputs are HIGH, forcing all four outputs HIGH.

### Ordering Information

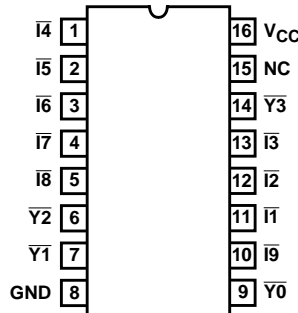
| PART NUMBER | TEMP. RANGE ( $^\circ C$ ) | PACKAGE    | PKG. NO. |
|-------------|----------------------------|------------|----------|
| CD74HC147E  | -55 to 125                 | 16 Ld PDIP | E16.3    |
| CD74HCT147E | -55 to 125                 | 16 Ld PDIP | E16.3    |
| CD74HC147M  | -55 to 125                 | 16 Ld SOIC | M16.15   |
| CD74HCT147M | -55 to 125                 | 16 Ld SOIC | M16.15   |

#### NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer or die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

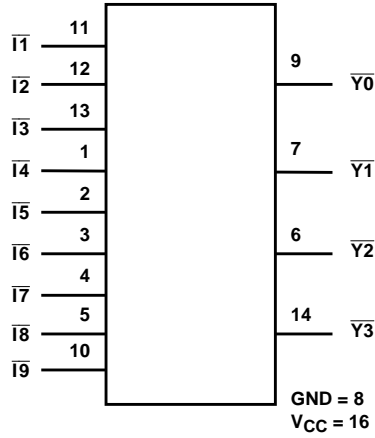
### Pinout

CD74HC147, CD74HCT147  
(PDIP, SOIC)  
TOP VIEW



**CD74HC147, CD74HCT147**

**Functional Diagram**



**TRUTH TABLE**

| INPUTS     |            |            |            |            |            |            |            |            | OUTPUTS    |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|
| $\bar{I}1$ | $\bar{I}2$ | $\bar{I}3$ | $\bar{I}4$ | $\bar{I}5$ | $\bar{I}6$ | $\bar{I}7$ | $\bar{I}8$ | $\bar{I}9$ | $\bar{Y}3$ | $\bar{Y}2$ | $\bar{Y}1$ | $\bar{Y}0$ |
| H          | H          | H          | H          | H          | H          | H          | H          | H          | H          | H          | H          | H          |
| X          | X          | X          | X          | X          | X          | X          | X          | L          | L          | H          | H          | L          |
| X          | X          | X          | X          | X          | X          | X          | L          | H          | L          | H          | H          | H          |
| X          | X          | X          | X          | X          | X          | L          | H          | H          | H          | L          | L          | L          |
| X          | X          | X          | X          | X          | L          | H          | H          | H          | H          | L          | L          | H          |
| X          | X          | X          | X          | L          | H          | H          | H          | H          | H          | L          | H          | L          |
| X          | X          | X          | L          | H          | H          | H          | H          | H          | H          | L          | H          | H          |
| X          | X          | L          | H          | H          | H          | H          | H          | H          | H          | H          | L          | L          |
| X          | L          | H          | H          | H          | H          | H          | H          | H          | H          | H          | L          | H          |
| L          | H          | H          | H          | H          | H          | H          | H          | H          | H          | H          | H          | L          |

NOTE: H = High Logic Level, L = Low Logic Level, X = Don't Care

# CD74HC147, CD74HCT147

## Absolute Maximum Ratings

|  |             |
|--|-------------|
| DC Supply Voltage, $V_{CC}$ .....                          | -0.5V to 7V |
| DC Input Diode Current, $I_{IK}$                           |             |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....           | $\pm 20mA$  |
| DC Output Diode Current, $I_{OK}$                          |             |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....           | $\pm 20mA$  |
| DC Output Source or Sink Current per Output Pin, $I_O$     |             |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....           | $\pm 25mA$  |
| DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ ..... | $\pm 50mA$  |

## Thermal Information

|  |                                  |
|--|----------------------------------|
| Thermal Resistance (Typical, Note 3)           | $\theta_{JA}$ (°C/W)             |
| PDIP Package .....                             | 90                               |
| SOIC Package .....                             | 160                              |
| Maximum Junction Temperature .....             | 150°C                            |
| Maximum Storage Temperature Range .....        | -65°C to 150°C                   |
| Maximum Lead Temperature (Soldering 10s) ..... | 300°C<br>(SOIC - Lead Tips Only) |

## Operating Conditions

|   |                |
|---|----------------|
| Temperature Range ( $T_A$ ) .....               | -55°C to 125°C |
| Supply Voltage Range, $V_{CC}$                  |                |
| HC Types .....                                  | .2V to 6V      |
| HCT Types .....                                 | .4.5V to 5.5V  |
| DC Input or Output Voltage, $V_I$ , $V_O$ ..... | 0V to $V_{CC}$ |
| Input Rise and Fall Time                        |                |
| 2V .....  | 1000ns (Max)   |
| 4.5V .....                                      | 500ns (Max)    |
| 6V .....  | 400ns (Max)    |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## DC Electrical Specifications

| PARAMETER                               | SYMBOL   | TEST CONDITIONS      |            | $V_{CC}$ (V) | 25°C |     |           | -40°C TO 85°C |         | -55°C TO 125°C |         | UNITS   |
|---|----------|----------------------|------------|--------------|------|-----|-----------|---------------|---------|----------------|---------|---------|
|   |          | $V_I$ (V)            | $I_O$ (mA) |              | MIN  | TYP | MAX       | MIN           | MAX     | MIN            | MAX     |         |
| <b>HC TYPES</b>                         |          |                      |            |              |      |     |           |               |         |                |         |         |
| High Level Input Voltage                | $V_{IH}$ | -                    | -          | 2            | 1.5  | -   | -         | 1.5           | -       | 1.5            | -       | V       |
|   |          |                      |            | 4.5          | 3.15 | -   | -         | 3.15          | -       | 3.15           | -       | V       |
|   |          |                      |            | 6            | 4.2  | -   | -         | 4.2           | -       | 4.2            | -       | V       |
| Low Level Input Voltage                 | $V_{IL}$ | -                    | -          | 2            | -    | -   | 0.5       | -             | 0.5     | -              | 0.5     | V       |
|   |          |                      |            | 4.5          | -    | -   | 1.35      | -             | 1.35    | -              | 1.35    | V       |
|   |          |                      |            | 6            | -    | -   | 1.8       | -             | 1.8     | -              | 1.8     | V       |
| High Level Output Voltage<br>CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02      | 2            | 1.9  | -   | -         | 1.9           | -       | 1.9            | -       | V       |
|   |          |                      | -0.02      | 4.5          | 4.4  | -   | -         | 4.4           | -       | 4.4            | -       | V       |
|   |          |                      | -0.02      | 6            | 5.9  | -   | -         | 5.9           | -       | 5.9            | -       | V       |
| High Level Output Voltage<br>TTL Loads  | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -          | -            | -    | -   | -         | -             | -       | -              | -       | V       |
|   |          |                      | -4         | 4.5          | 3.98 | -   | -         | 3.84          | -       | 3.7            | -       | V       |
|   |          |                      | -5.2       | 6            | 5.48 | -   | -         | 5.34          | -       | 5.2            | -       | V       |
| Low Level Output Voltage<br>CMOS Loads  | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02       | 2            | -    | -   | 0.1       | -             | 0.1     | -              | 0.1     | V       |
|   |          |                      | 0.02       | 4.5          | -    | -   | 0.1       | -             | 0.1     | -              | 0.1     | V       |
|   |          |                      | 0.02       | 6            | -    | -   | 0.1       | -             | 0.1     | -              | 0.1     | V       |
| Low Level Output Voltage<br>TTL Loads   | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | -          | -            | -    | -   | -         | -             | -       | -              | -       | V       |
|   |          |                      | 4          | 4.5          | -    | -   | 0.26      | -             | 0.33    | -              | 0.4     | V       |
|   |          |                      | 5.2        | 6            | -    | -   | 0.26      | -             | 0.33    | -              | 0.4     | V       |
| Input Leakage Current                   | $I_I$    | $V_{CC}$ or GND      | -          | 6            | -    | -   | $\pm 0.1$ | -             | $\pm 1$ | -              | $\pm 1$ | $\mu A$ |
| Quiescent Device Current                | $I_{CC}$ | $V_{CC}$ or GND      | 0          | 6            | -    | -   | 8         | -             | 80      | -              | 160     | $\mu A$ |

## CD74HC147, CD74HCT147

### DC Electrical Specifications (Continued)

| PARAMETER  | SYMBOL           | TEST CONDITIONS                    |                     | V <sub>CC</sub> (V) | 25°C |     |      | -40°C TO 85°C |      | -55°C TO 125°C |     | UNITS |
|--|------------------|------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
|  |                  | V <sub>I</sub> (V)                 | I <sub>O</sub> (mA) |                     | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX |       |
| <b>HCT TYPES</b>   |                  |                                    |                     |                     |      |     |      |               |      |                |     |       |
| High Level Input Voltage                                       | V <sub>IH</sub>  | -                                  | -                   | 4.5 to 5.5          | 2    | -   | -    | 2             | -    | 2              | -   | V     |
| Low Level Input Voltage  | V <sub>IL</sub>  | -                                  | -                   | 4.5 to 5.5          | -    | -   | 0.8  | -             | 0.8  | -              | 0.8 | V     |
| High Level Output Voltage<br>CMOS Loads                        | V <sub>OH</sub>  | V <sub>IH</sub> or V <sub>IL</sub> | -0.02               | 4.5                 | 4.4  | -   | -    | 4.4           | -    | 4.4            | -   | V     |
| High Level Output Voltage<br>TTL Loads                         |                  |                                    | -4                  | 4.5                 | 3.98 | -   | -    | 3.84          | -    | 3.7            | -   | V     |
| Low Level Output Voltage<br>CMOS Loads                         | V <sub>OL</sub>  | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 4.5                 | -    | -   | 0.1  | -             | 0.1  | -              | 0.1 | V     |
| Low Level Output Voltage<br>TTL Loads                          |                  |                                    | 4                   | 4.5                 | -    | -   | 0.26 | -             | 0.33 | -              | 0.4 | V     |
| Input Leakage Current  | I <sub>I</sub>   | V <sub>CC</sub> and GND            | 0                   | 5.5                 | -    | -   | ±0.1 | -             | ±1   | -              | ±1  | μA    |
| Quiescent Device Current                                       | I <sub>CC</sub>  | V <sub>CC</sub> or GND             | 0                   | 5.5                 | -    | -   | 8    | -             | 80   | -              | 160 | μA    |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ΔI <sub>CC</sub> | V <sub>CC</sub> -2.1               | -                   | 4.5 to 5.5          | -    | 100 | 360  | -             | 450  | -              | 490 | μA    |

NOTE: For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

### HCT Input Loading Table

| INPUT   | UNIT LOADS |
|---|------------|
| $\bar{1}_1, \bar{1}_2, \bar{1}_3, \bar{1}_6, \bar{1}_7$ | 1.1        |
| $\bar{1}_4, \bar{1}_5, \bar{1}_8, \bar{1}_9$            | 1.5        |

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

### Switching Specifications Input t<sub>r</sub>, t<sub>f</sub> = 6ns

| PARAMETER                                     | SYMBOL                              | TEST CONDITIONS       | V <sub>CC</sub> (V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|---|-------------------------------------|-----------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|   |                                     |                       |                     | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| <b>HC TYPES</b>                               |                                     |                       |                     |      |     |     |               |     |                |     |       |
| Propagation Delay, Input to Output (Figure 1) | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 160 | -             | 200 | -              | 240 | ns    |
|   |                                     |                       | 4.5                 | -    | -   | 32  | -             | 40  | -              | 48  | ns    |
|   |                                     |                       | 5                   | -    | 13  | -   | -             | -   | -              | -   | ns    |
|   |                                     |                       | 6                   | -    | -   | 27  | -             | 34  | -              | 41  | ns    |
| Transition Times (Figure 1)                   | t <sub>TLH</sub> , t <sub>THL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 75  | -             | 95  | -              | 110 | ns    |
|   |                                     |                       | 4.5                 | -    | -   | 15  | -             | 19  | -              | 22  | ns    |
|   |                                     |                       | 6                   | -    | -   | 13  | -             | 16  | -              | 19  | ns    |
| Input Capacitance                             | C <sub>IN</sub>                     | -                     | -                   | -    | -   | 10  | -             | 10  | -              | 10  | pF    |

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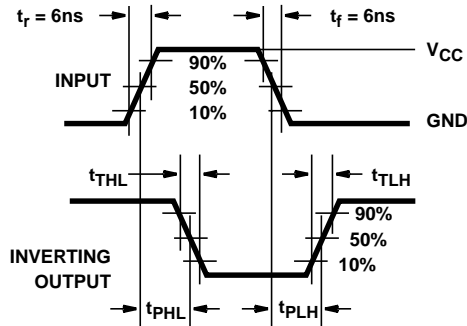
### Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

| PARAMETER  | SYMBOL             | TEST CONDITIONS     | $V_{CC}$ (V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|--|--------------------|---------------------|--------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|  |                    |                     |              | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| Power Dissipation Capacitance<br>(Notes 4, 5)    | $C_{PD}$           | -                   | 5            | -    | 32  | -   | -             | -   | -              | -   | pF    |
| <b>HCT TYPES</b>                                 |                    |                     |              |      |     |     |               |     |                |     |       |
| Propagation Delay,<br>Input to Output (Figure 2) | $t_{PLH}, t_{PHL}$ | $C_L = 50\text{pF}$ | 4.5          | -    | -   | 35  | -             | 44  | -              | 53  | ns    |
|  |                    |                     | 5            | -    | 14  | -   | -             | -   | -              | -   | ns    |
| Transition Times (Figure 2)                      | $t_{TLH}, t_{THL}$ | $C_L = 50\text{pF}$ | 4.5          | -    | -   | 15  | -             | 19  | -              | 22  | ns    |
| Input Capacitance                                | $C_{IN}$           | -                   | -            | -    | -   | 10  | -             | 10  | -              | 10  | pF    |
| Power Dissipation Capacitance<br>(Notes 4, 5)    | $C_{PD}$           | -                   | 5            | -    | 42  | -   | -             | -   | -              | -   | pF    |

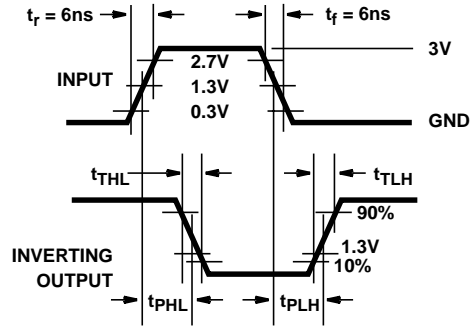
**NOTES:**

4.  $C_{PD}$  is used to determine the dynamic power consumption, per gate.
5.  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = Input Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

### Test Circuits and Waveforms



**FIGURE 6. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**



**FIGURE 7. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

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