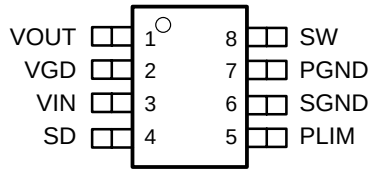
# UCC2941–3, UCC2941–5, UCC2941–ADJ, UCC3941–3, UCC3941–5, UCC3941–ADJ
# 1-V SYNCHRONOUS BOOST CONVERTER

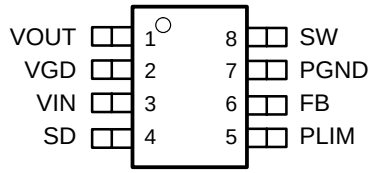
SLUS242B – JANUARY 1999 – REVISED JUNE 2001

- **1-V Input Voltage Operation Start-up Ensured Under Full Load on Main Output With Operation Down to 0.4 V**
- **Input Voltage Range of 1 V to $V_{OUT}$ + 0.5 V**
- **500-mW Output Power at Battery Voltages as Low as 0.8 V**
- **Secondary 9-V Supply From a Single Inductor**
- **Adjustable Output Power Limit Control**
- **Output Fully Disconnected in Shutdown**
- **Adaptive Current-Mode Control for Optimum Efficiency**
- **8-μA Shutdown Supply Current**

**D OR N PACKAGE**
**(TOP VIEW)**




**UCC3941–ADJ ONLY**
**(TOP VIEW)**




## description

The UCC3941 family of low-input-voltage single-inductor boost-converters are optimized to operate from a single- or dual-alkaline cell, and step up to a 3.3-V, 5-V, or an adjustable output at 500 mW. The UCC3941 family also provides an auxiliary 9-V, 100-mW output, primarily for the gate drive supply, which can be used for applications requiring an auxiliary output such as a 5-V supply by linear regulating. The primary output starts up under full load at input voltages typically as low as 0.8 V, with a guaranteed maximum of 1 V, and operates down to 0.4 V once the converter is operating, maximizing battery utilization.

Demanding applications such as pagers and personal digital assistants require high efficiency from several milliwatts to several hundred milliwatts, and the UCC3941 family accommodates these applications with > 80% typical efficiencies over the wide range of operation. The high-efficiency at low-output current is achieved by optimizing switching and conduction losses along with low-quiescent current. At higher output current the 0.25-Ω charge switch, and the 0.4-Ω synchronous rectifier, along with continuous-mode conduction, provide high efficiency. The wide input-voltage range on the UCC3941 family can accommodate other power sources such as NiCd and NiMH.

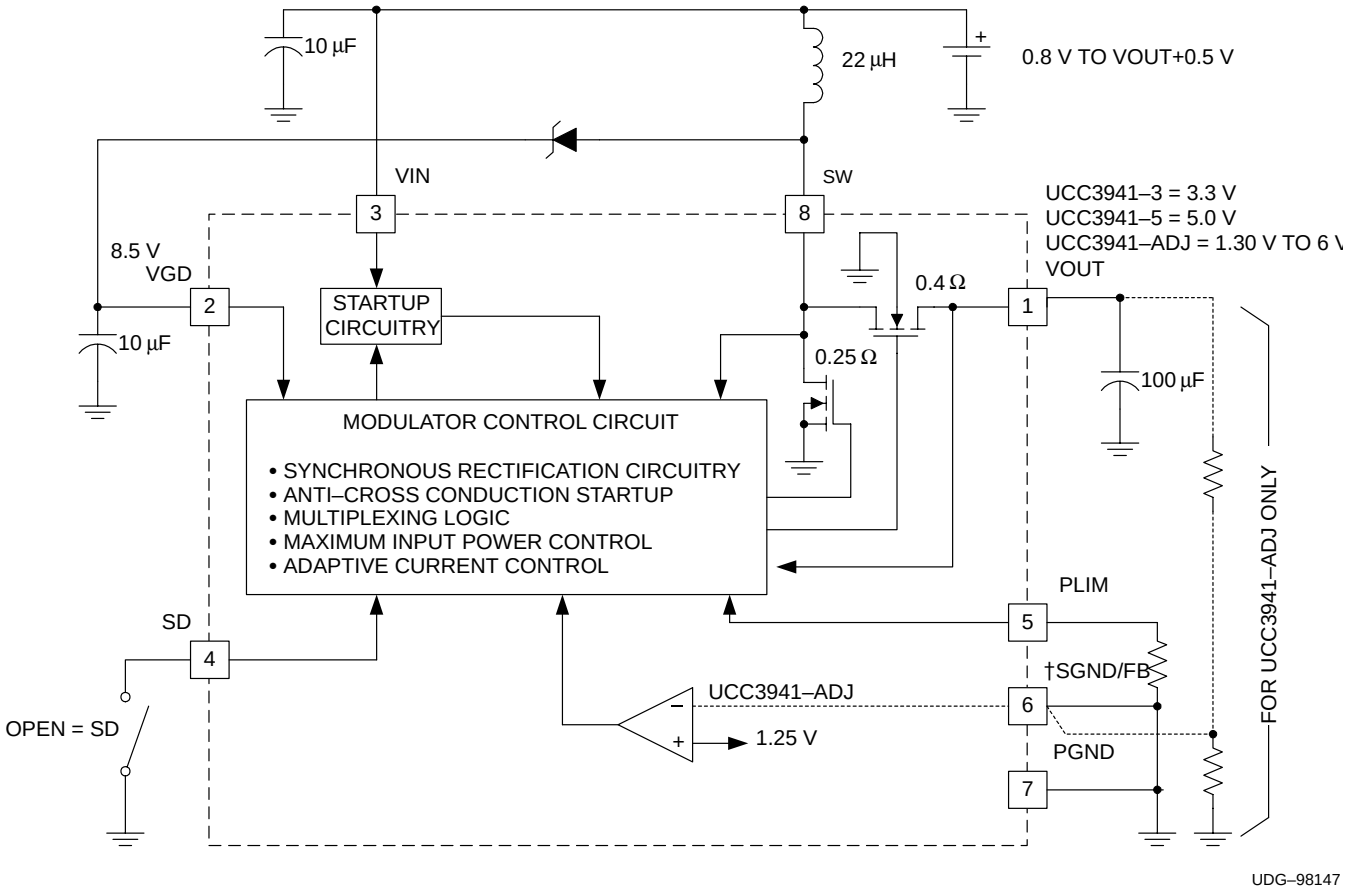
Other features include maximum power control and shutdown control. The device is available in 8-pin SOIC (D) and 8-pin DIP (N).

**AVAILABLE OPTIONS**

| $T_A$ | PACKAGED DEVICES | | | | | |
|---|---|---|---|---|---|---|
| | SOIC (D)† | | | DIP (N) | | |
| | $V_{OUT}$ (V) | | | | | |
| | 3.3 | 5.0 | Adjustable (1.3 V to 6 V) | 3.3 | 5.0 | Adjustable (1.3 V to 6 V) |
| –40°C to 85°C | UCC2941D–3 | UCC2941D–5 | UCC2941D–ADJ | UCC2941N–3 | UCC2941N–5 | UCC2941N–ADJ |
| 0°C to 70°C | UCC3941D–3 | UCC3941D–5 | UCC3941D–ADJ | UCC3941N–3 | UCC3941N–5 | UCC3941N–ADJ |

† The SOIC (D) package is available left end taped and reeled. Add an R suffix to the device type (e.g., UCC2941DR–3) to order quantities of 2500 devices per reel.

## functional block diagram

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† For UCC3941–ADJ only: Pin 7 = SGND & PGND, Pin 6 = output sense feedback, FB

## Terminal Functions

| TERMINAL | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| | UCC2941–3<br>UCC2941–5<br>UCC3941–3<br>UCC3941–5 | UCC2941–ADJ<br>UCC3941–ADJ | | |
| FB | – | 6 | I | Feedback control pin used in the UCC3941–ADJ version only. The internal reference for this comparator is 1.25V and external resistors provide the gain to the output voltage. |
| PGND | 7 | 7 | – | Power ground of the IC. The inductor charging current flows through this pin. For the UCC3941–ADJ signal ground and power ground lines are tied to a common pin. |
| PLIM | 5 | 5 | I | Peak current limit |
| SGND | 6 | – | – | Signal ground of the IC. For the UCC3941–ADJ signal ground and power ground lines are tied to a common pin |
| SD | 4 | 4 | I | Shutdown pin |
| SW | 8 | 8 | I | Inductor connection |
| VGD | 2 | 2 | O | Gate drive supply |
| VIN | 3 | 3 | I | Input voltage to supply the IC during startup. After the output is running the IC draws power from VOUT or VGD |
| VOUT | 1 | 1 | O | Main output voltage |

## detailed description

### peak limit (PLIM)

The PLIM pin is programmed to set the maximum input power for the converter. For example a 1-A current limit at 1 V would have a 333-mA limit at 3 V input keeping the input power constant at 1 W. The peak current at VIN = 1 V is programmed to 1.5 A (1.5 W) when this pin is grounded. The power limit is given by:

$$PL_W = \left(\frac{11.8 \times n}{R_{PL} + 6.7}\right) + \left(V_{IN} \times 0.26\right) \quad (1)$$

where $R_{PL}$ is equal to the external resistor from the PLIM pin to ground and *n* is the expected efficiency of the converter. The peak current limit is given by:

$$I_{PK(A)} = \frac{11.8 \times n}{V_{IN} \times \left(R_{PL} + 6.7\right)} + 0.26 \quad (2)$$

Constant power gives several advantages over constant current such as lower output ripple.

### shutdown (SD)

When the SD pin is open, the built-in 7-μA current source pulls up on the pin and programs the IC to go into shutdown mode. This pin requires an open circuit for shutdown and does not operate correctly when driven to a logic level high with TTL or CMOS logic. When this pin is connected to ground, (either directly or with a transistor) the IC is enabled and both output voltages regulate.

## detailed description (continued)

### needs a name (SW)

The SW pin inductor is connected between this node and VIN. The VGD (gate drive supply) flyback diode is also connected to this pin. When servicing the 3.3-V supply, this pin goes low charging the inductor, then shut off, dumping the energy through the synchronous rectifier to the output. When servicing the VGD supply, the internal synchronous rectifier stays off, and the energy is diverted to VGD through the flyback diode. During discontinuous portions of the inductor current a MOSFET resistively connects VIN to SW damping excess circulating energy to eliminate undesired high frequency ringing.

### gate drive supply (VGD)

The VGD pin is coarsely regulated around 9 V, and is primarily used for the gate drive supply for the power switches in the IC. This pin can be loaded with up to 10 mA as long as it does not present a load at voltages below 2 V. This ensures proper startup of the IC. The VGD supply can go as low as 7.5 V without interfering with the servicing of the 3.3-V output. Below 7.5 V, VGD has the highest priority, although in practice the voltage should not decay to that level if the output capacitor is sized properly.

### output voltage (VOUT)

Main output voltage (3.3 V, 5 V, or adjustable) which has highest priority in the multiplexing scheme, as long as VGD is above the critical level of 7.5 V. Loads over 150 mA are achievable at an input voltage of 1-V. This output starts up with 1-V input at full load.

## absolute maximum ratings over operating free–air temperature range (unless otherwise noted)†

Input voltage VIN, PLIM . . . . . –0.3 V to 10 V
Voltage range, VGD, SW . . . . . –0.3 V to 15 V
Voltage range, SD . . . . . –0.3 V to VIN
Output voltage range, VOUT . . . . . –0.3 V to 10 V
Operating virtual junction temperature range, $T_J$ . . . . . –55°C to 150°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C
. . . . . CDM 1 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability. Currents are positive into, negative out of the specified terminal.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 85°C$ POWER RATING |
|---|---|---|---|
| D | 760 mW | 6.1 mW/°C | 390 mW |
| N | 980 mW | 7.9 mW/°C | 510 mW |

## recommended operating conditions

| | MIN | MAX | UNIT |
|---|---|---|---|
| Input voltage | 0.8 | 5.0 | V |
| Output voltage | 1.8 | 5.5 | V |
| Output current | 0 | 200 | mA |

**electrical characteristics over recommended operating junction temperature range, for UCC3941, $T_A$ = 0°C to 70°C, for UCC2941, $T_A$ = –40°C to 85°C, VIN = 1.25 V, $T_A$ = $T_J$ (unless otherwise noted)**

### input voltage

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Minumum startup voltage | $T_J$ = 25°C, $I_{OUT}$ = 100 mA, No external VGD load, See Note 1 | | 0.8 | 1.0 | V |
| | $T_J$ = 0°C to 85°C, $I_{OUT}$ = 100 mA, No external VGD load, See Note 1 | | 0.9 | 1.1 | V |
| | $T_J$ = –40°C to 0°C, $I_{OUT}$ = 100 mA, No external VGD load, See Note 1 | | 0.9 | 1.5 | V |
| Minumum dropout voltage | $I_{OUT}$ = 0 mA, VGD = 6.3 V, No external VGD load, | | | 0.5 | V |
| Input voltage range | | 1 | | VOUT + 0.5 | V |
| Quiescent supply current | See note 2 | | 13 | 25 | µA |
| Shutdown supply current | SD = open | | 8 | 20 | µA |

### output voltage

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Quiescent supply current | | See note 2 | | 32 | 80 | µA |
| Shutdown supply current | | SD = open | | 6 | 15 | µA |
| Regulation voltage | UCC3941–3 | 1 V < VIN < 3 V | 3.18 | 3.25 | 3.37 | V |
| | | 1 V < VIN < 3 V, 0 mA < $I_{OUT}$ < 150 mA, See Note 1 | 3.17 | 3.30 | 3.43 | V |
| | UCC3941–5 | 1 V < VIN < 5 V | 4.85 | 5.00 | 5.15 | V |
| | | 1 V < VIN < 5 V, 0 mA < $I_{OUT}$ < 100 mA, See Note 1 | 4.8 | 5.0 | 5.2 | V |
| Feedback voltage | UCC3941–ADJ | 1 V < VIN < 3 V | 1.212 | 1.250 | 1.288 | V |

### VGD output

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Quiescent supply current | See note 2 | | 25 | 60 | µA |
| Shutdown supply current | SD = open | | 8 | 20 | µA |
| Regulation voltage | 1 V < VIN < 3 V | 7.5 | 8.7 | 9.2 | V |
| | 1 V < VIN < 3 V, 0 mA < $I_{OUT}$ < 10 mA, See Note 1 | 7.4 | 87 | 9.3 | V |

NOTE 1: Performance from application circuit shown in Figures 3, 4, and 5. Ensured by design. Not 100% production tested.
NOTE 2: For the UCC3941–3, VOUT = 3.47 V and VGD = 9.3 V. For the UCC3941–5, VOUT = 5.25 V, VGD = 9.3 V. For the UCC3941–ADJ, FB = 1.315 V, VGD = 9.3 V.

**electrical characteristics over recommended operating junction temperature range, for UCC3941, $T_A$ = 0°C to 70°C, for UCC2941, $T_A$ = –40°C to 85°C, VIN = 1.25 V, $T_A = T_J$ (unless otherwise noted) (continued)**

### inductor charging (L = 22 μH)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Peak discontinuous current | Over operating range | | 0.05 | 0.85 | A |
| Peak continuous current | $R_{PLIM}$ = 6.2 Ω, See Note 1 | 0.5 | 0.9 | 1.3 | A |
| Charge switch $R_{DS(on)}$ | N and D package, I = 200 mA | | 0.25 | 0.40 | Ω |
| Current limit delay | See Note 1 | | 50 | | ns |

### synchronous rectifier

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Rectifier $R_{DS(on)}$ | UCC3941N–ADJ<br>UCC3941D–ADJ | I = 200 mA, $V_{OUT}$ = 3.3 V | | 0.35 | 0.6 | Ω |
| | UCC3941N–3<br>UCC3941D–3 | I = 200 mA | | 0.35 | 0.6 | Ω |
| | UCC3941N–5<br>UCC3941D–5 | I = 200 mA | | 0.5 | 0.8 | Ω |

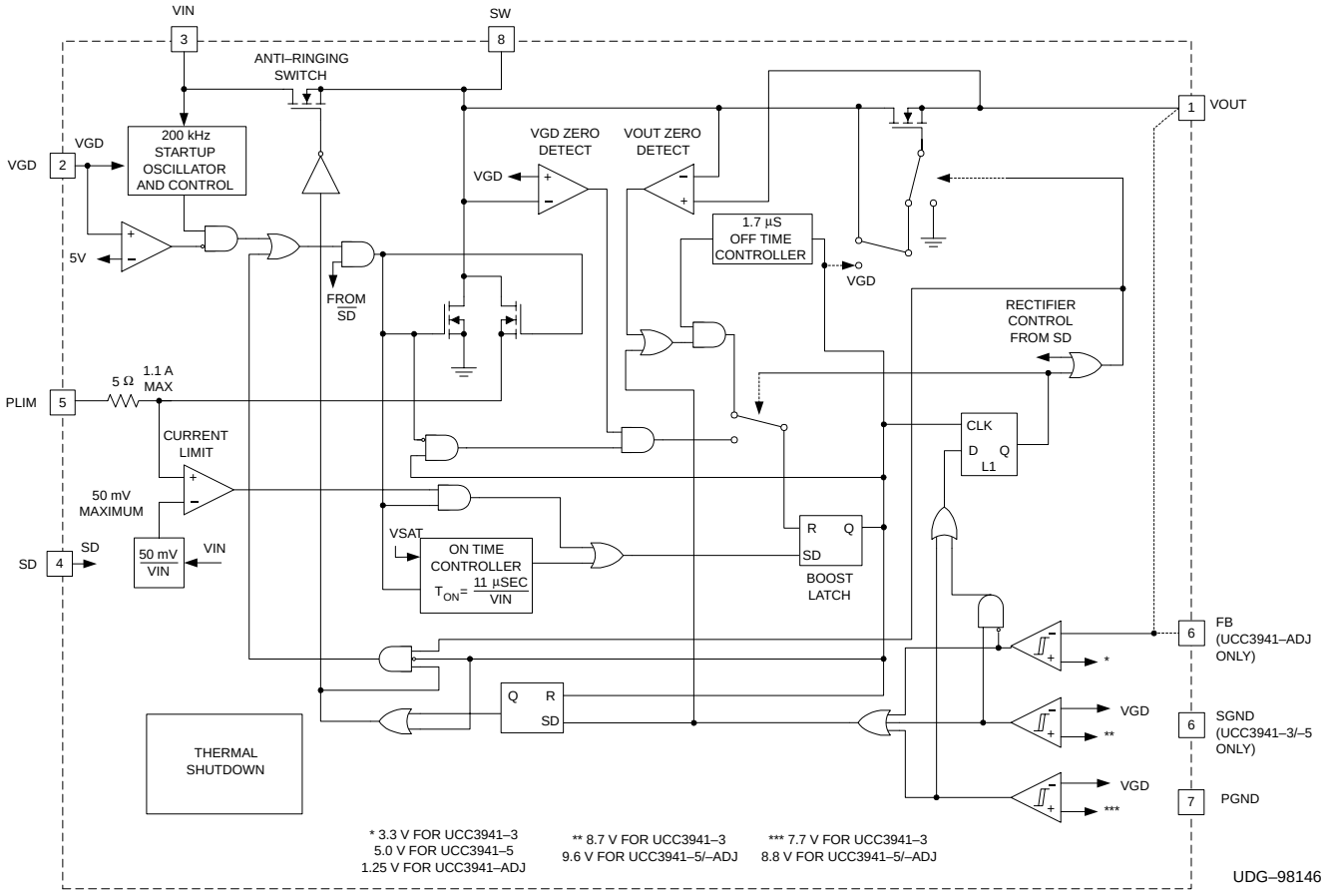
### shutdown

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Shutdown bias current | SD = 0 V | –10 | –7 | | μA |

NOTE 1: Performance from application circuit shown in Figures 3, 4, and 5. Ensured by design. Not 100% production tested.
NOTE 2: For the UCC3941–3, VOUT = 3.47 V and VGD = 9.3 V. For the UCC3941–5, VOUT = 5.25 V, VGD = 9.3 V. For the UCC3941–ADJ, FB = 1.315 V, VGD = 9.3 V.

## APPLICATION INFORMATION

A detailed block diagram of the UCC3941 is shown in Figure 1. Unique control circuitry provides high-efficiency power conversion for both light and heavy loads by transitioning between discontinuous and continuous conduction based on load conditions. Figure 2 depicts converter waveforms for the application circuit shown in Figure 3. A single 22-µH inductor provides the energy pulses required for a highly efficient 3.3-V converter at up to 500 mW output power.




NOTE: Switches are shown in the logic low state; external $R_{PLIM}$ = 6.2 Ω

**Figure 1. 1–V Synchronous Boost**

## APPLICATION INFORMATION

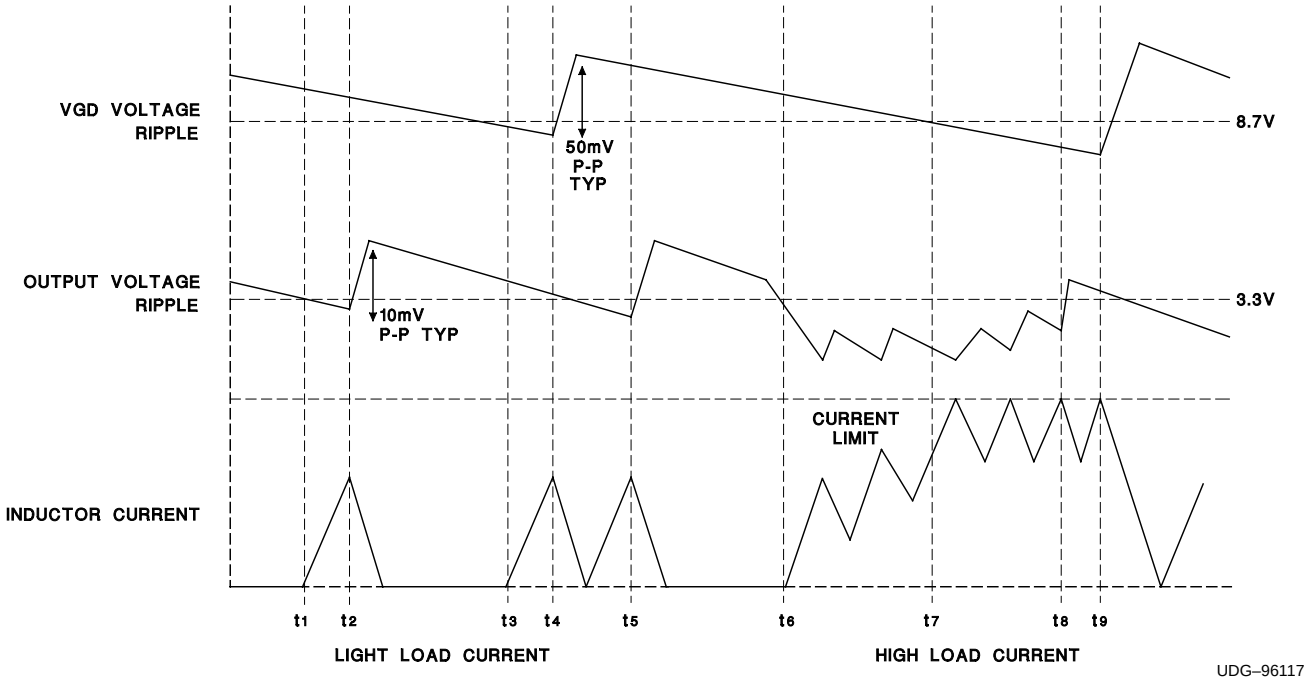



**Figure 2. Inductor Current and Output Ripple Waveforms**

At time t1, the 3.3-V output drops below its lower threshold, and the inductor is charged with an on time determined by:

$$t_{ON} = \frac{12\ \mu s}{VIN} \tag{3}$$

For a 1.25-V input, and a 22-µH inductor, the resulting peak current is approximately 500 mA. At time t2, the inductor begins to discharge with a minimum off time of 1.7 µs. Under lightly loaded conditions, the amount of energy delivered in this single pulse satisfies the voltage-control loop, and the converter does not command any more energy pulses until the output again drops below the lower voltage threshold.

At time t3, the VGD supply has dropped below its lower threshold, but the output voltage is still above its threshold point. This results in an energy pulse to the gate drive supply at t4. However, while the gate drive is being serviced, the output voltage has dropped below its lower threshold, so the state machine commands an energy pulse to the output as soon as the gate drive pulse is completed.

Time t6, represents a transition between light and heavy load. A single energy pulse is not sufficient to force the output voltage above its upper threshold before the minimum off-time has expired, and a second charge cycle is commanded. Since the inductor current does not reach zero in this case, the peak current is greater than 0.5 A at the end of the next charge on time. This results in a ratcheting of the inductor current until either the output voltage is satisfied, or the converter reaches its programmed current limit. At time t7, the gate drive voltage has dropped below its threshold but the converter continues to service the output because it has highest priority, unless VGD drops below 7.5 V.

Between t7 and t8, the converter reaches its peak current limit which is determined by $R_{PL}$ and VIN. Once the limit is reached, the converter operates in continuous mode with approximately 200 mA of ripple current. At time t8, the output voltage is satisfied, and the converter can service VGD, which occurs at t9.

## APPLICATION INFORMATION

### programming the power limit

The UCC3941 incorporates an adaptive power limit control that modifies the converter current limit as a function of input voltage. In order to program the function, the user simply determines the output power requirements and makes an initial converter efficiency estimate. The programming resistor is chosen by:

$$R_{PL} = \frac{11.8 \times n}{P_{OUT} - \left(0.26 \times n \times V_{BAT}\right)} - 6.7 \tag{4}$$

Where *n* is the initial efficiency estimate. For 500 mW of output power, with a 1.0 V input, and an efficiency estimate of 0.75:

$$R_{PL} = \frac{11.8 \times 0.75}{0.5 - (0.26 \times 0.75 \times 1.0)} - 6.7 = 22\ \Omega \tag{5}$$

For decreasing values of $R_{PL}$, the power limit increases. Therefore, to ensure that the converter can supply 500 mW of output power, a power limiting resistor of less than 22 Ω must be chosen.

$$P_L = V_{BAT} \times I_L = \left(\frac{11.8}{22 + 6.7}\right) + (1.0 \times 0.26) = 0.67\ W \tag{6}$$

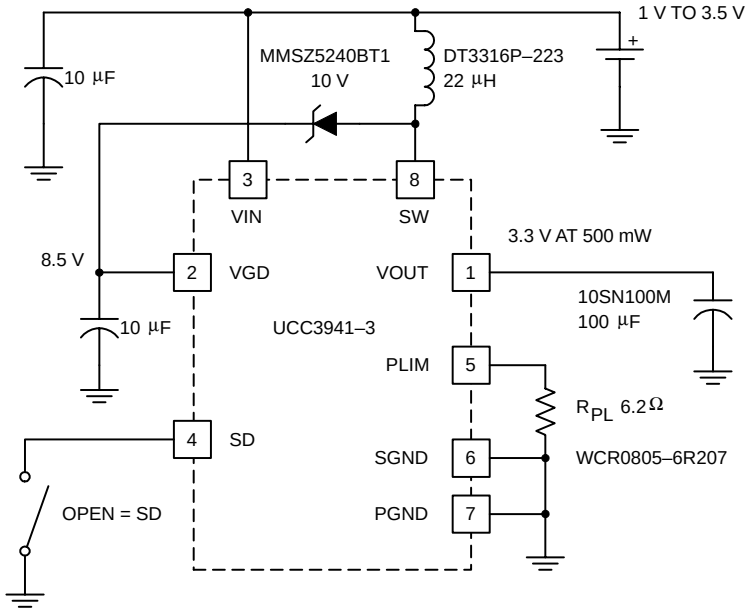



**Figure 3. Dual Output Synchronous Boost, 3.3-V Version**

## APPLICATION INFORMATION

### programming the power limit (continued)

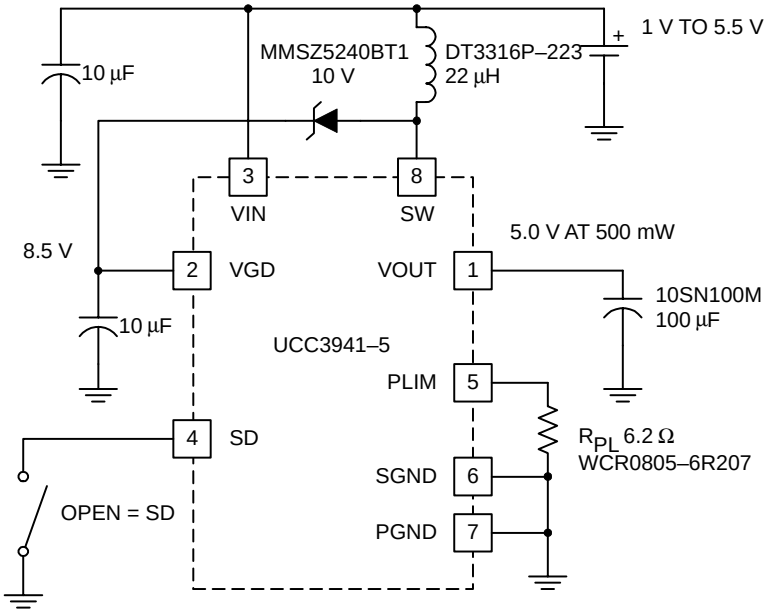



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**Figure 4. Dual Output Synchronous Boost, 5-V Version**

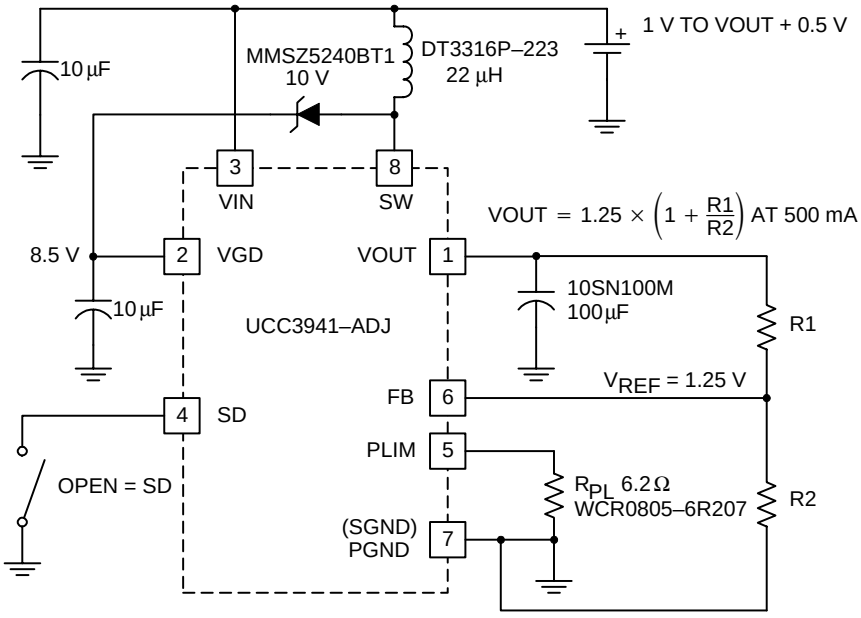


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**Figure 5. Dual Output Synchronous Boost, Adjustable Version**

## APPLICATION INFORMATION

### programming the power limit (continued)

This power limiting setting supports 0.5 W of output power. It should be noted that the power limit equation contains an approximation which results in slightly less actual input power than the equation predicts. This discrepancy results from the fact that the average current delivered to the load is less than the peak current set by the power limit function due to current ripple. However, if the ripple component of the current is kept low, the power limit equation can be used as an adequate estimate of input power. Furthermore, since an initial efficiency estimate was required, sufficient margin can be built into this estimate to ensure proper converter operation. The 6.2-Ω external power limit resistor (shown in Figures 3, 4, and 5) results in approximately 700 mW of power capability with a 1.0-V input.

### inductor selection

An inductor value of 22 μH works well in most applications, but values between 10 μH and 100 μH are also acceptable. Lower-value inductors typically offer lower ESR and smaller physical size. Due to the nature of the *bang–bang* controllers, larger inductor values typically results in larger overall voltage ripple, because once the output voltage level is satisfied the converter goes discontinuous, resulting in the residual energy of inductor causing overshoot.

It is recommended to keep the ESR of the inductor below 0.15 Ω for 500-mW applications. A Coilcraft DT3316P–223 surface mount inductor is one choice since it has a current rating of 1.5 A and an ESR of 84 mΩ. Other choices for surface mount inductors are shown in Table 1.

**Table 1. Inductor Suppliers**

| MANUFACTURER | CONTACT INFORMATION | PART NUMBERS |
|---|---|---|
| Coilcraft | Cary, Illinois<br>Tel: (708) 639–2361 Fax: (708) 639–1469 | DT Series |
| Coiltronics | Boca Raton, Florida<br>Tel: (407) 241–7878 | CTX Series |

## APPLICATION INFORMATION

### output capacitor selection

Once the inductor value is selected, the capacitor value determines the ripple of the converter. The worst case peak-to-peak ripple of a cycle is determined by two components, one is due to the charge storage characteristic, and the other is the ESR of the capacitor. The worst-case ripple occurs when the inductor is operating at maximum current and is expressed as follows:

$$\Delta V = \frac{\left(I_{CL}\right)^2 \times L}{2 \times C \times \left(V_O - V_I\right)} + \left(I_{CL} \times C_{ESR}\right) \quad (7)$$

where

- $I_{CL}$ = the peak inductor current $\left(I_{CL} = \frac{\text{Power Limit}}{V_{IN}}\right)$
- $\Delta V$ = output ripple
- $V_O$ = output voltage
- $V_I$ = input voltage
- $C_{ESR}$ = ESR of the output capacitor

A Sanyo OS–CON series surface mount capacitor (10SN100M) is one recommendation. This part has an ESR rating of 90 μW at 100 μF. Other potential capacitor sources are shown in Table 2.

**Table 2. Capacitor Suppliers**

| MANUFACTURER | CONTACT INFORMATION | PART NUMBERS |
|---|---|---|
| Sanyo Video Components | San Diego, California<br>Tel: (619) 661–6322<br>Fax: (619) 661–1055 | OS–CON Series |
| AVX | Sanford, Maine<br>Tel: (207) 282–5111<br>Fax: (207) 283–1941 | TPS Series |
| Sprague | Concord, New Hampshire<br>Tel: (603) 224–1961 | 695D Series |

### input capacitor selection

Since the UCC3941 family does not require a large decoupling capacitor on the input voltage to operate properly, a 10-μF capacitor is sufficient for most applications. Optimum efficiency occurs when the capacitor value is large enough to decouple the source impedance. This usually occurs for capacitor values in excess of 100 μF.

## APPLICATION INFORMATION

### system shutdown

The UCC3941 is enabled by shorting the SD pin to ground either directly or through a transistor.The UCC3941 is shut down when the SD pin is floated (an internal current source pulls up on the SD pin). Since the SD pin is not TTL compatible, 0 V enables the part but 3 V or even 5 V does not properly shut down the device.

The recommended circuit for a system requiring shutdown control is shown below. The enable line is driven from a microprocessor or system logic. If enable is low, the SD pin is floated since Q1 base voltage is too low to turn on. If enable is high, Q1 turns on and SD is grounded, enabling the UCC3941. A 1-MΩ resistor to VGD allows Q1 to turn on if the enable pin is high impedance during startup. If shutdown control is not required for the application, SD should be grounded directly.

**CAUTION:**

**The UCC3941 should be allowed sufficient time to properly shutdown in a controlled manner. This is accomplished by ensuring that enable is held low at least 500 μs before subsequently being brought high. Not adhering to the timings in Figure 7 can result in DEVICE FAILURE.**

**SHUTDOWN INTERFACE CIRCUIT**

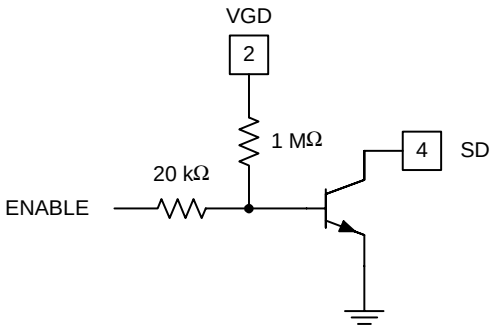



**Figure 6**

**PROPOGATION DELAY AND RISE TIME**

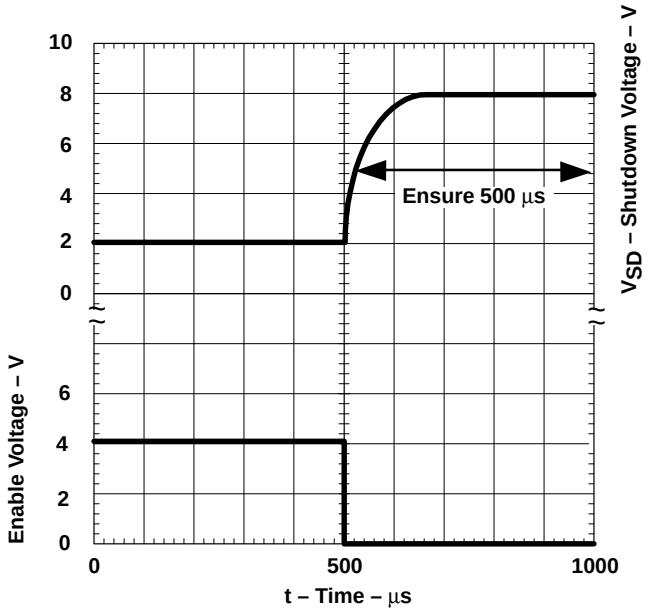



**Figure 7. SD Timings**

## APPLICATION INFORMATION

### SD interface circuit

#### reducing inrush current

A switch mode boost converter requires $V_{IN}$ to be less than $V_{OUT}$ in order to control current in the inductor. Forward voltage is applied across the inductor during the $t_{ON}$ time (increasing current) while reverse voltage is applied during the $t_{OFF}$ time (decreasing current). During startup, $V_{OUT}$ is less than $V_{IN}$, resulting in inrush current until the output is charged.

The UCC3941 has two outputs; VGD and $V_{OUT}$. Inrush current in a two cell alkaline application is typically higher than with a single cell and should be minimized to reduce peak currents in the controller. The VGD inrush current can be minimized by reducing the value of the VGD capacitor. For example a 10-µF capacitor may cause a 3-A inrush where a 1-µF capacitor results in less than 1-A of inrush. Reducing the $V_{OUT}$ inrush current is more difficult since the output capacitance may need to be large to minimize output ripple. In a two cell application, a diode from $V_{IN}$ to $V_{OUT}$ (shown In Figure 8) precharges the $V_{OUT}$ capacitor and reduces inrush.

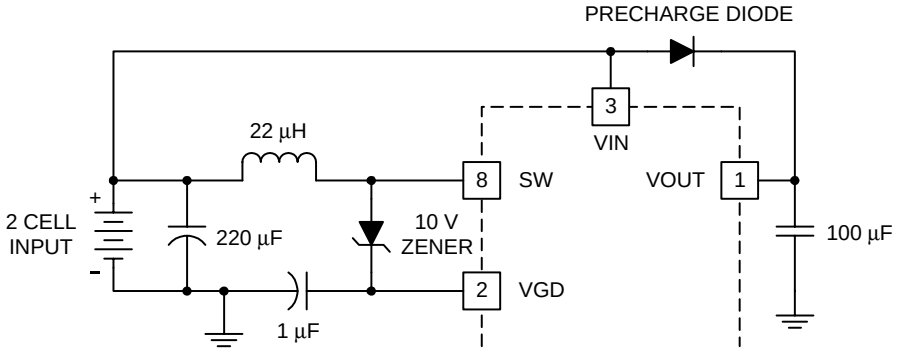



**Figure 8. Optional Precharge Diode for $V_{OUT}$ for 2-Cell Input**

### avoiding inductor saturation

Inductor selection should take into account size, on resistance, and the current capabilities of the part. Inductor ratings include both saturation current and maximum operating current for the device. The $R_{PLIM}$ resistor and inductor should be selected to guarantee the inductor does not saturate during normal operation. A saturated inductor can cause excessive peak currents and δi/δt slopes which may result in part failure. Inrush and normal operating current should be viewed with a current probe and oscilloscope to ensure the inductor current is linear and controlled.

## TYPICAL CHARACTERISTICS

EFFICIENCY
vs.
OUTPUT CURRENT

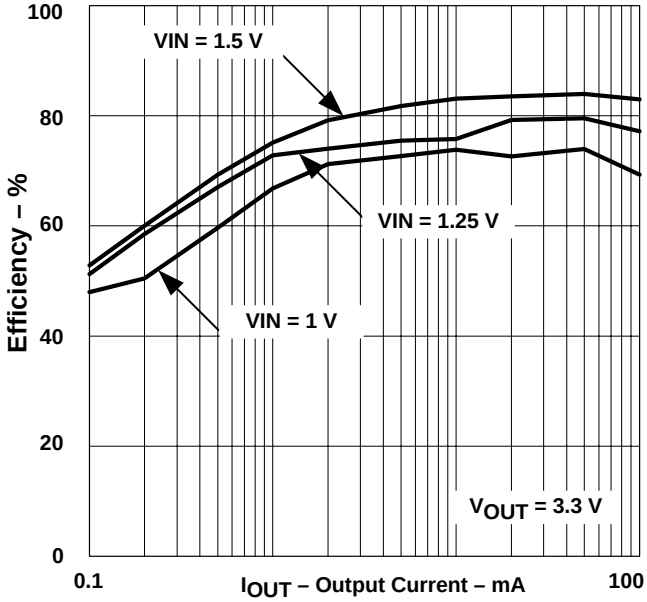



Figure 9

EFFICIENCY
vs.
OUTPUT CURRENT

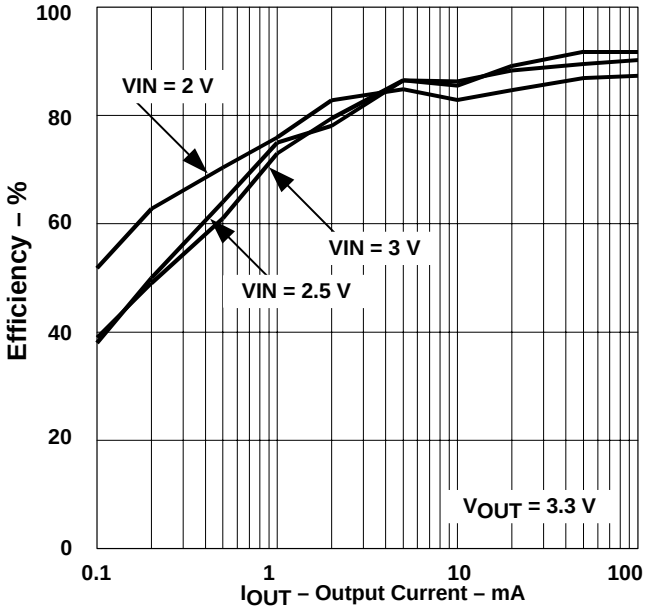



Figure 10

STARTUP CHARACTERISTICS

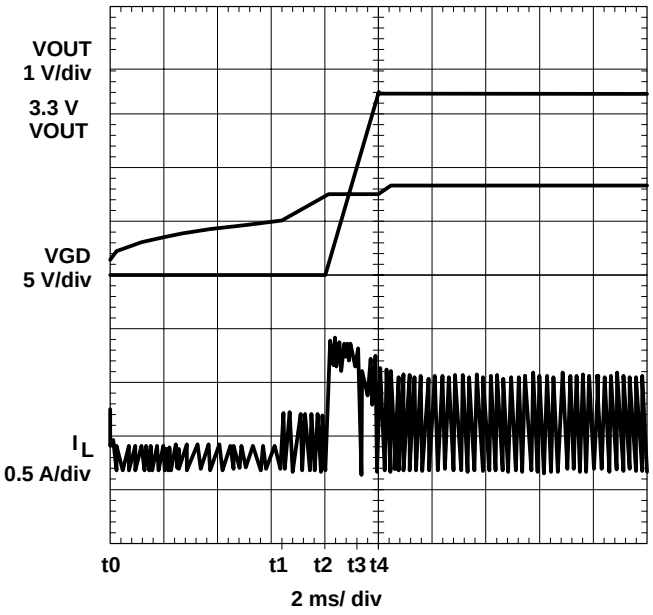



Figure 11

PSUEDO CONTINUOUS MODE OPERATION

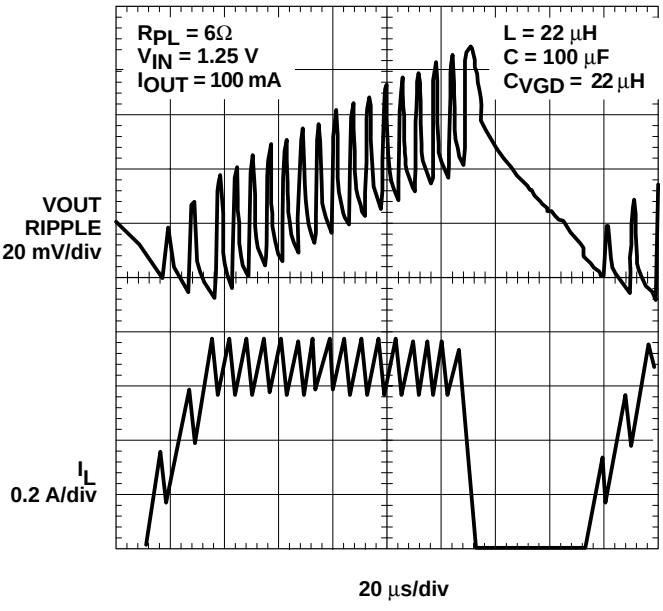



Figure 12

### startup characteristics timing sequence (for single output mode)

(see Figure 11)

- t0 the 200-kHz srartup oscillator starts VGD rising
- t1 VGD reaches sufficient voltage (5 V) to run in normal operating mode
- t2 VGD reaches sufficient voltage (7.5 V) to start VOUT
- t3 VOUT is serviced and starts up
- t4 VOUT reaches sufficient voltage and VGD is serviced until it reaches 8.5 V

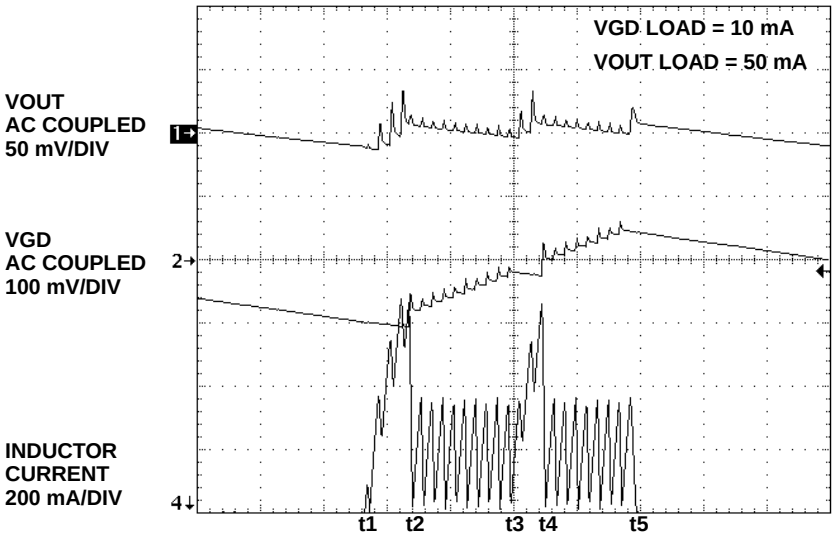



**Figure 13.**

### startup characteristics timing sequence (for dual output mode)

(see Figure 13)

- t1 VOUT is serviced and inductor current goes continuous
- t2 VGD is serviced with discontinuous operation and reaches its first threshold (7.5 V)
- t3 VOUT requires servicing and because VGD has reached its minimum threshold of 7.5 V, VOUT takes priority
- t4 VOUT is satisfied and VGD is serviced until the second threshold (8.7 V) is reached
- t5 Both outputs are satisfied

## TYPICAL CHARACTERISTICS

**UCC3941–3 DROPOUT VOLTAGE vs. OUTPUT CURRENT**

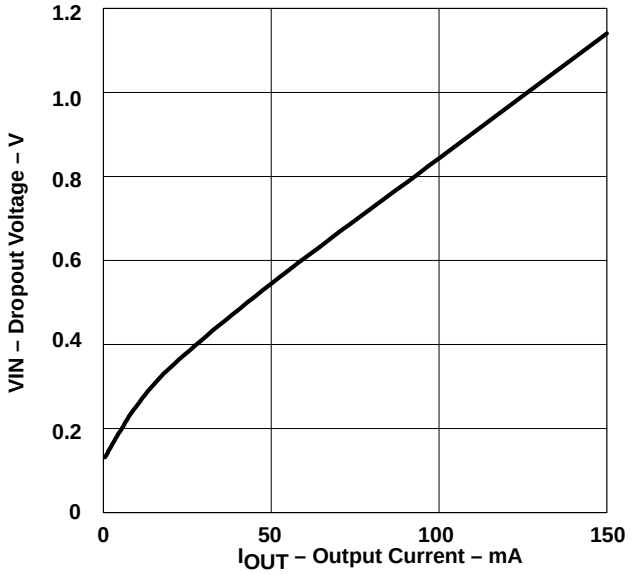



Figure 14

**MINIMUM STARTUP VOLTAGE vs. OUTPUT CURRENT**

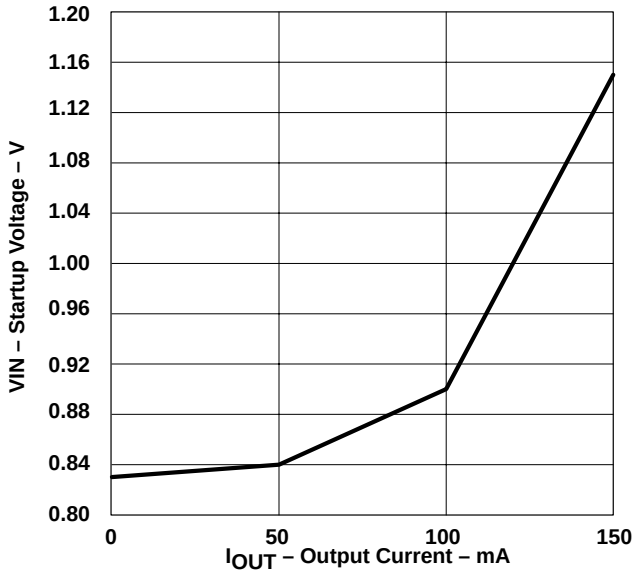
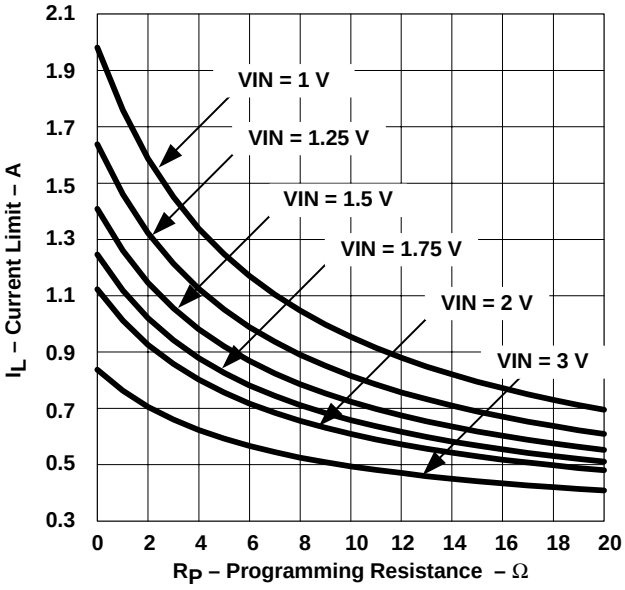



Figure 15

**UCC3941–ADJ (N and D PACKAGES) CURRENT LIMIT vs. PROGRAMMING RESISTANCE**




$$IL_{(Rp)} = \frac{11.5}{\left(\left(6.7 + R_P\right) \times V_{BAT}\right)} + 0.26$$

Figure 16

**STARTUP VOLTAGE vs. TEMPERATURE**

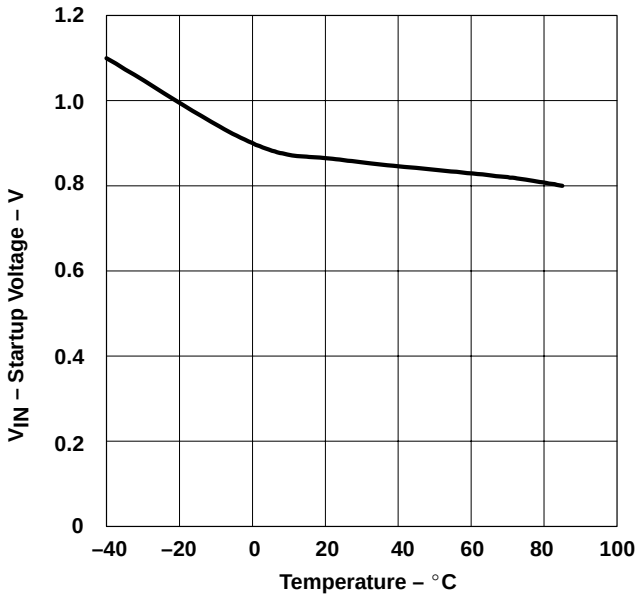



Figure 17

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