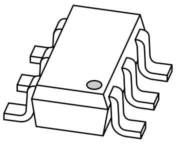


PBLS4001D

40 V PNP BISS loadswitch

Rev. 01 — 30 November 2004 **Objective data sheet**

1. Product profile

1.1 General description

Low V_{CEsat} PNP transistor and NPN resistor-equipped transistor in a SOT457 (SC-74) package.

1.2 Features

- Low V_{CEsat} (BISS) transistor and resistor-equipped transistor in one package
- Low ‘threshold’ voltage (< 1 V) compared to MOSFET
- Low drive power required
- Space-saving solution
- Reduction of component count.

1.3 Applications

- Supply line switches
- Battery charger switches
- High-side switches for LEDs, drivers and backlights
- Portable equipment.

1.4 Quick reference data

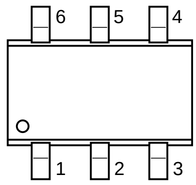
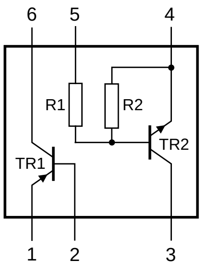
Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1; PNP: low V_{CEsat} transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	–40	V
I_C	collector current (DC)		-	-	–1	A
R_{CEsat}	equivalent on-resistance	I_C = –500 mA; I_B = –50 mA	-	240	340	mΩ
TR2; NPN: resistor-equipped transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	50	V
I_O	output current (DC)		-	-	100	mA
R1	bias resistor 1 (input)		1.54	2.2	2.86	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	

PHILIPS

2. Pinning information

Table 2: Pinning

Pin	Description	Simplified outline	Symbol
1	emitter TR1	 SOT457	 sym036
2	base TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	collector TR1		

3. Ordering information

Table 3: Ordering information

Type number	Package		
	Name	Description	Version
PBLS4001D	SC-74	plastic surface mounted package; 6 leads	SOT457

4. Marking

Table 4: Marking codes

Type number	Marking code
PBLS4001D	R1

5. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
TR1; PNP: low V_{CEsat} transistor					
V_{CBO}	collector-base voltage	open emitter	-	–40	V
V_{CEO}	collector-emitter voltage	open base	-	–40	V
V_{EBO}	emitter-base voltage	open collector	-	–5	V
I_C	collector current (DC)		-	–1	A
I_{CM}	peak collector current	$t_p \leq 300$ µs	-	–2	A
I_B	base current (DC)		-	–300	mA
I_{BM}	peak base current	$t_p \leq 300$ µs	-	–1	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C [1]	-	300	mW
TR2; NPN: resistor-equipped transistor					
V_{CBO}	collector-base voltage	open emitter	-	50	V
V_{CEO}	collector-emitter voltage	open base	-	50	V

Table 5: Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{EBO}	emitter-base voltage	open collector		-	10	V
V_I	input voltage					
	positive			-	+12	V
	negative			-	–10	V
I_O	output current (DC)			-	100	mA
I_{CM}	peak collector current			-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	300	mW
Per device						
P_{tot}	total power dissipation		[1]	-	600	mW
T_{stg}	storage temperature			–65	+150	°C
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			–65	+150	°C

[1] Device mounted on an FR4 printed-circuit board with 65 µm copper strip line, standard footprint.

6. Thermal characteristics

Table 6: Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	208	K/W

[1] Device mounted on an FR4 printed-circuit board with 65 mm copper strip line, standard footprint.

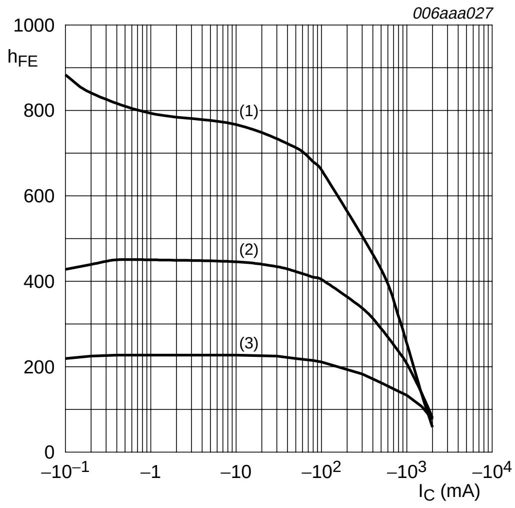
7. Characteristics

Table 7: Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1; PNP: low V_{CEsat} transistor							
I_{CBO}	collector-base cut-off current	V_{CB} = –40 V; I_E = 0 A		-	-	–100	nA
		V_{CB} = –40 V; I_E = 0 A; T_j = 150 °C		-	-	–50	μA
I_{CES}	collector-emitter cut-off current	V_{CE} = –30 V; I_B = 0 A		-	-	–100	nA
I_{EBO}	emitter-base cut-off current	V_{EB} = –5 V; I_C = 0 A		-	-	–100	nA
h_{FE}	DC current gain	V_{CE} = –5 V					
		I_C = –1 mA		300	-	-	
		I_C = –100 mA	[1]	300	-	800	
		I_C = –500 mA	[1]	250	-	-	
		I_C = –1 A	[1]	160	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = –100 mA; I_B = –1 mA		-	–80	–140	mV
		I_C = –500 mA; I_B = –50 mA	[1]	-	–120	–170	mV
		I_C = –1 A; I_B = –100 mA	[1]	-	–200	–310	mV
R_{CEsat}	equivalent on-resistance	I_C = –500 mA; I_B = –50 mA	[1]	-	240	340	mΩ
V_{BEsat}	base-emitter saturation voltage	I_C = –1 A; I_B = –50 mA	[1]	-	-	–1.1	V
$V_{BE(on)}$	base-emitter turn-on voltage	V_{CE} = –5 V; I_C = –1 A	[1]	-	-	–1	V
f_T	transition frequency	I_C = –50 mA; V_{CE} = –10 V; f = 100 MHz		150	-	-	MHz
C_c	collector capacitance	V_{CB} = –10 V; I_E = i_e = 0 A; f = 1 MHz		-	-	12	pF
TR2; NPN: resistor-equipped transistor							
I_{CBO}	collector-base cut-off current	V_{CB} = 50 V; I_E = 0 A		-	-	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 30 V; I_B = 0 A		-	-	1	μA
		V_{CE} = 30 V; I_B = 0 A; T_j = 150 °C		-	-	50	μA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0 A		-	-	2	mA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 20 mA		30	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA		-	-	150	mV
$V_{I(off)}$	off-state input voltage	V_{CE} = 5 V; I_C = 1 mA		-	1.2	0.5	V
$V_{I(on)}$	on-state input voltage	V_{CE} = 0.3 V; I_C = 20 mA		2	1.6	-	V
R1	bias resistor 1 (input)			1.54	2.2	2.86	kΩ
R2/R1	bias resistor ratio			0.8	1	1.2	
C_c	collector capacitance	V_{CB} = 10 V; I_E = i_e = 0 A; f = 1 MHz		-	-	2.5	pF

[1] Pulse test: $t_p \leq 300$ μs; $\delta \leq 0.02$.



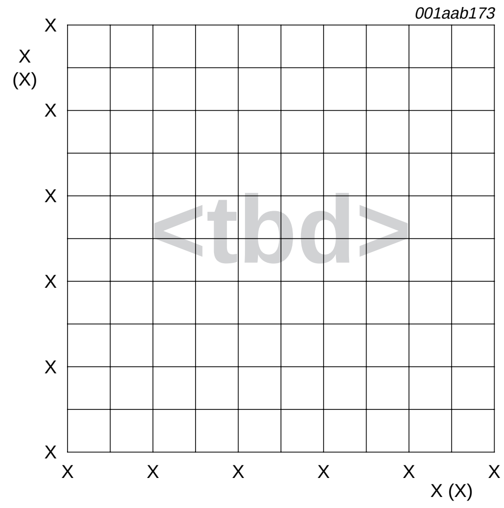
V_{CE} = −5 V.

(1) T_{amb} = 150 °C.

(2) T_{amb} = 25 °C.

(3) T_{amb} = −55 °C.

Fig 1. TR1 (PNP): DC current gain as a function of collector current; typical values



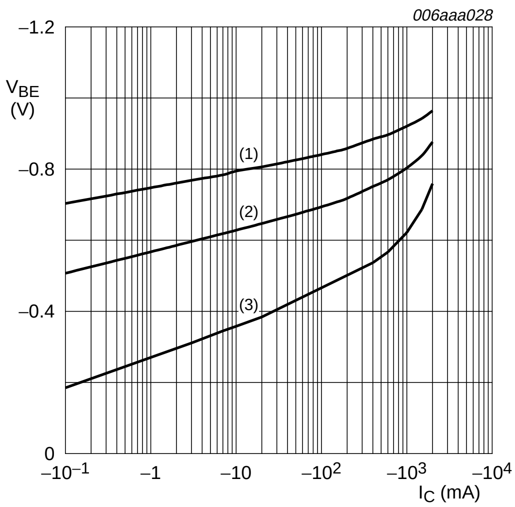
I_C/I_B = 20.

(1) T_{amb} = 150 °C.

(2) T_{amb} = 25 °C.

(3) T_{amb} = −55 °C.

Fig 2. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



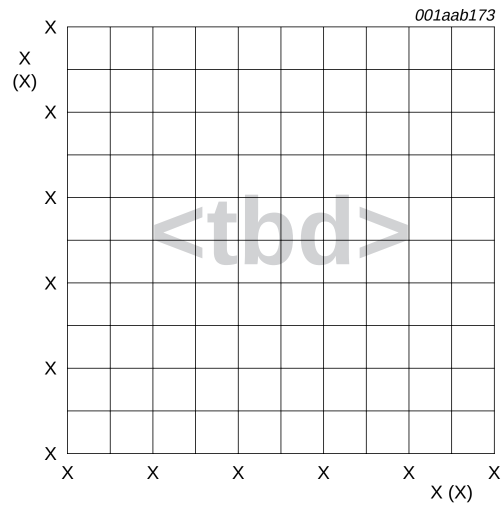
V_{CE} = −5 V.

(1) T_{amb} = −55 °C.

(2) T_{amb} = 25 °C.

(3) T_{amb} = 150 °C.

Fig 3. TR1 (PNP): Base-emitter voltage as a function of collector current; typical values



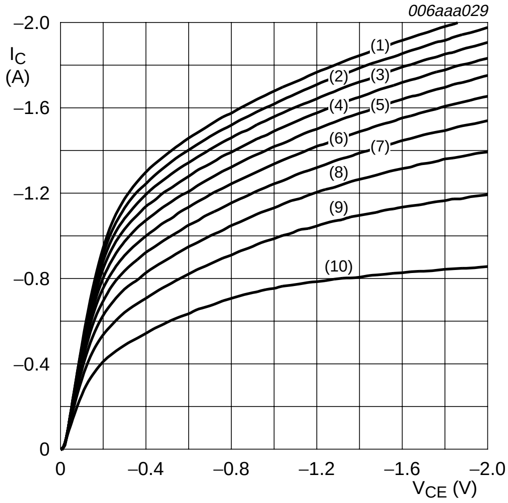
I_C/I_B = 20.

(1) T_{amb} = 150 °C.

(2) T_{amb} = 25 °C.

(3) T_{amb} = −55 °C.

Fig 4. TR1 (PNP): Base-emitter saturation voltage as a function of collector current; typical values



T_{amb} = 25 °C.

(1) I_B = −50 mA.

(2) I_B = −45 mA.

(3) I_B = −40 mA.

(4) I_B = −35 mA.

(5) I_B = −30 mA.

(6) I_B = −25 mA.

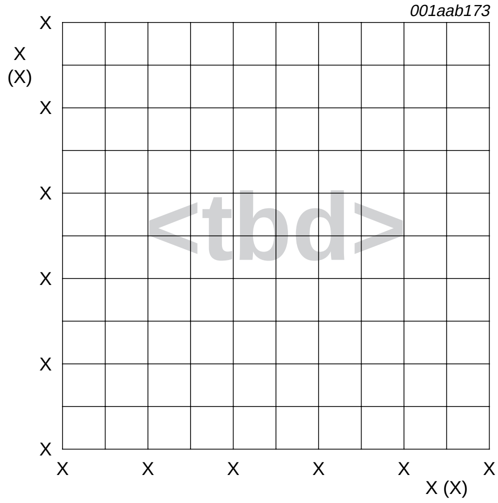
(7) I_B = −20 mA.

(8) I_B = −15 mA.

(9) I_B = −10 mA.

(10) I_B = −5 mA.

Fig 5. TR1 (PNP): Collector current as a function of collector-emitter voltage; typical values



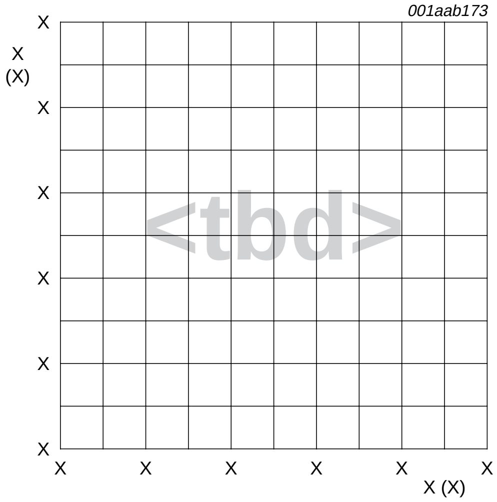
I_C/I_B = 20.

(1) T_{amb} = −55 °C.

(2) T_{amb} = 25 °C.

(3) T_{amb} = 150 °C.

Fig 6. TR1 (PNP): Equivalent on-resistance as a function of collector current; typical values



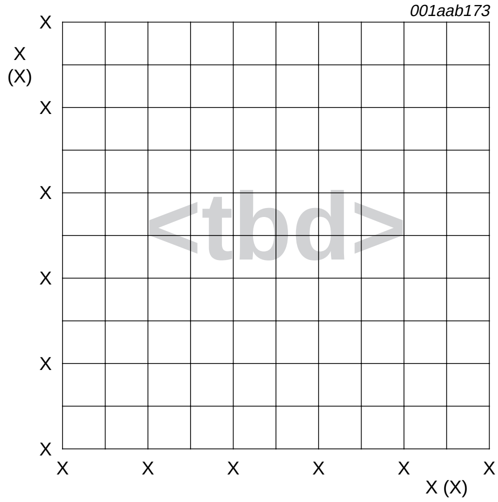
T_{amb} = 25 °C.

(1) I_C/I_B = 100.

(2) I_C/I_B = 50.

(3) I_C/I_B = 10.

Fig 7. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



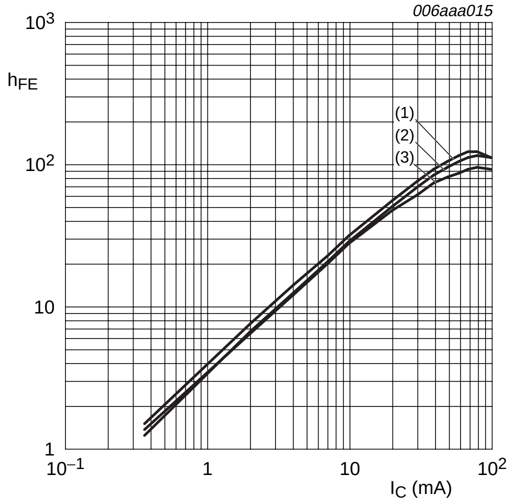
T_{amb} = 25 °C.

(1) I_C/I_B = 100.

(2) I_C/I_B = 50.

(3) I_C/I_B = 10.

Fig 8. TR1 (PNP): Equivalent on-resistance as a function of collector current; typical values



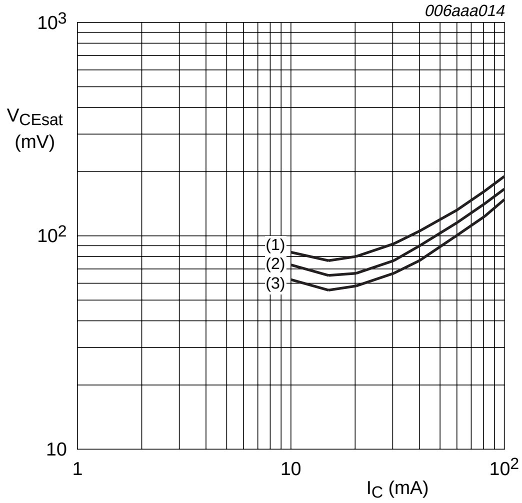
V_{CE} = 5 V.

(1) T_{amb} = 150 °C.

(2) T_{amb} = 25 °C.

(3) T_{amb} = −40 °C.

Fig 9. TR2 (NPN): DC current gain as a function of collector current; typical values



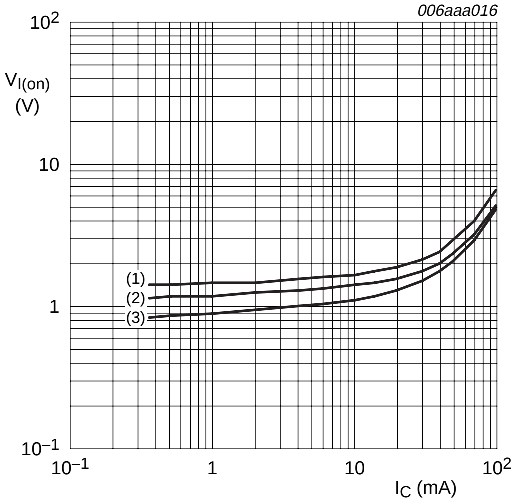
I_C/I_B = 20.

(1) T_{amb} = 100 °C.

(2) T_{amb} = 25 °C.

(3) T_{amb} = −40 °C.

Fig 10. TR2 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



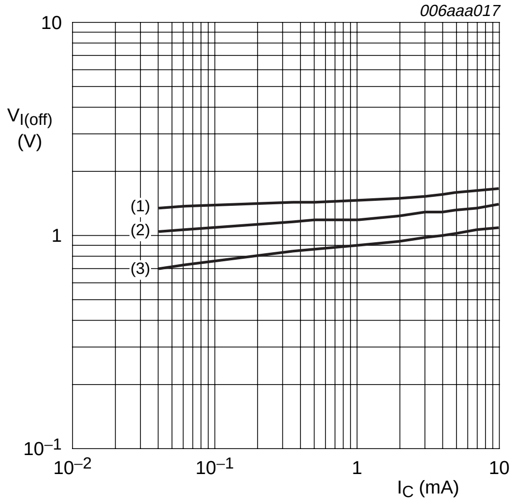
V_{CE} = 0.3 V.

(1) T_{amb} = −40 °C.

(2) T_{amb} = 25 °C.

(3) T_{amb} = 100 °C.

Fig 11. TR2 (NPN): On-state input voltage as a function of collector current; typical values



V_{CE} = 5 V.

(1) T_{amb} = −40 °C.

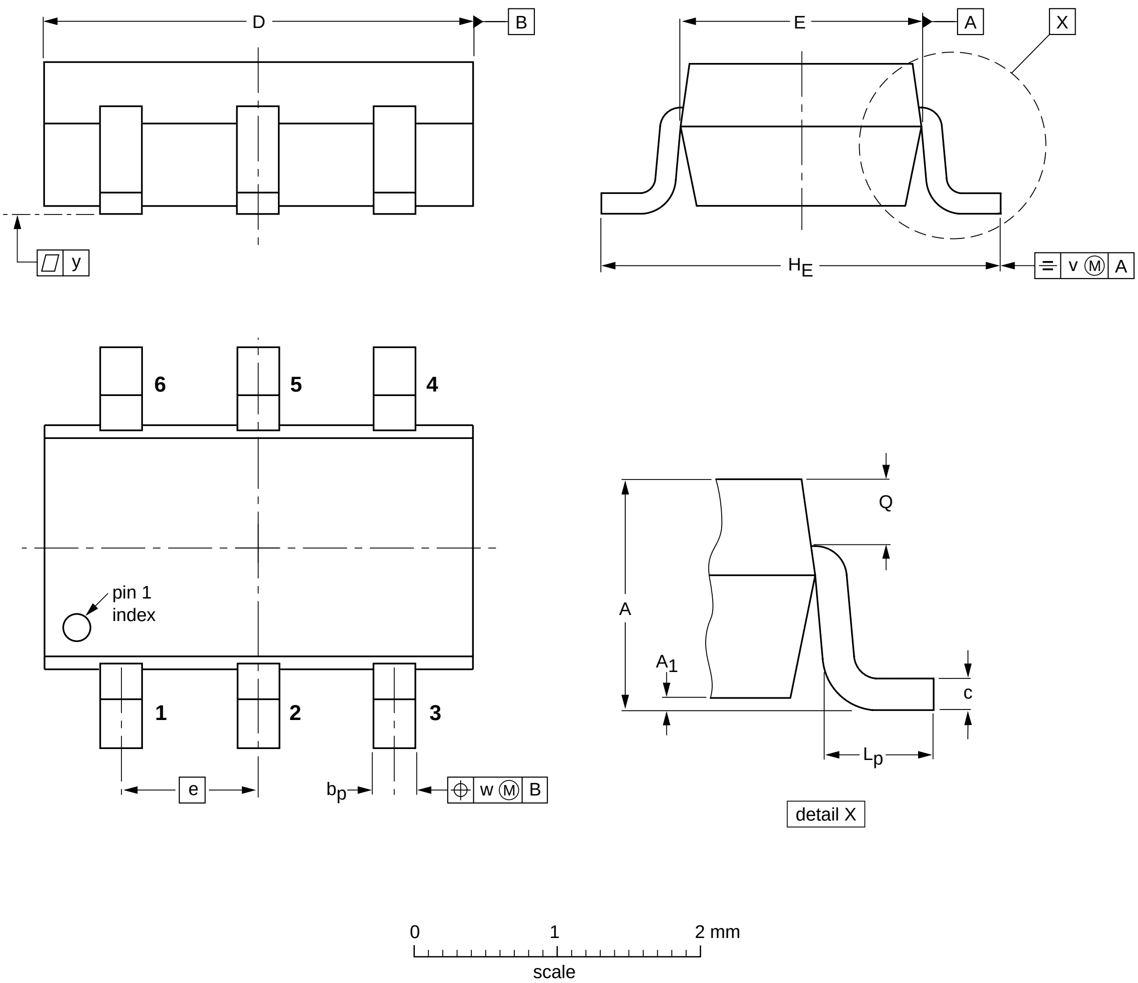
(2) T_{amb} = 25 °C.

(3) T_{amb} = 100 °C.

Fig 12. TR2 (NPN): Off-state input voltage as a function of collector current; typical values

8. Package outline

Plastic surface mounted package; 6 leads **SOT457**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT457			SC-74			~~01-05-04~~ 04-11-08

Fig 13. Package outline SOT457 (SC-74)

9. Packing information

Table 8: Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code. [1]

Type number	Package	Description		Packing quantity	
				3000	10000
PBLS4001D	SOT457	4 mm pitch, 8 mm tape and reel; T1	[2]	-115	-135
		4 mm pitch, 8 mm tape and reel; T2	[3]	-125	-165

[1] For further information and the availability of packing methods, see Section 14.

[2] T1: normal taping.

[3] T2: reverse taping.

10. Revision history

Table 9: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PBLS4001D_1	20041130	Objective data sheet	-	9397 750 13905	-

11. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

12. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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15. Contents

Date of release: 30 November 2004
Document number: 9397 750 13905

Published in The Netherlands