



## N-Channel Enhancement-Mode Vertical DMOS FETs

### Ordering Information

BV <sub>DSS</sub> / BV <sub>DGS</sub>	R <sub>DS(ON)</sub> (max)	V <sub>GS(th)</sub> (max)	I <sub>D(on)</sub> (min)	Order Number / Package		
				TO-236AB*	TO-92	TO-243AA**
250V	7.0Ω	2.0V	1.2A	TN5325K1	TN5325N3	TN5325N8

Product marking for SOT-23: N3C* where * = 2-week alpha date code
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\* Same as SOT-23. All units shipped on 3,000 piece carrier tape reels.

\*\* Shipped on 2,000 piece carrier tape and reels.

### Features

- Low threshold – 2.0V max.
- Free from secondary breakdown
- Low power drive requirement
- Low C<sub>iss</sub> and fast switching speeds
- Excellent thermal stability
- High input impedance and high gain
- Complementary N- and P-channel devices

### Applications

- Logic level interfaces – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

### Absolute Maximum Ratings

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

\* Distance of 1.6 mm from case for 10 seconds.

Product marking for TO-243AA

TN3C\*

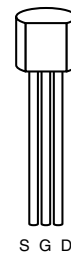
Where \* = 2-week alpha date code

### Advanced DMOS Technology

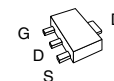
These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Package Options



TO-92



TO-243AA  
(SOT-89)



TO-236AB  
(SOT-23)

Note: See Package Outline section for dimensions.

## Thermal Characteristics

Package	$I_D$ (continuous)*	$I_D$ (pulsed)	Power Dissipation @ $T_A = 25^\circ\text{C}$	$\theta_{jc}$ $^\circ\text{C/W}$	$\theta_{ja}$ $^\circ\text{C/W}$	$I_{DR}^*$	$I_{DRM}$
TO-236AB	150mA	400mA	0.36W	200	350	150mA	400mA
TO-92	215mA	800mA	0.74W	125	170	215mA	800mA
TO-243AA	316mA	1.5A	1.6W**	15	78**	316mA	1.5A

\*  $I_D$  (continuous) is limited by max rated  $T_j$ .

\*\* Mounted on FR5 board. 25mm x 25mm x 1.57mm. Significant  $P_D$  increase possible on ceramic substrate.

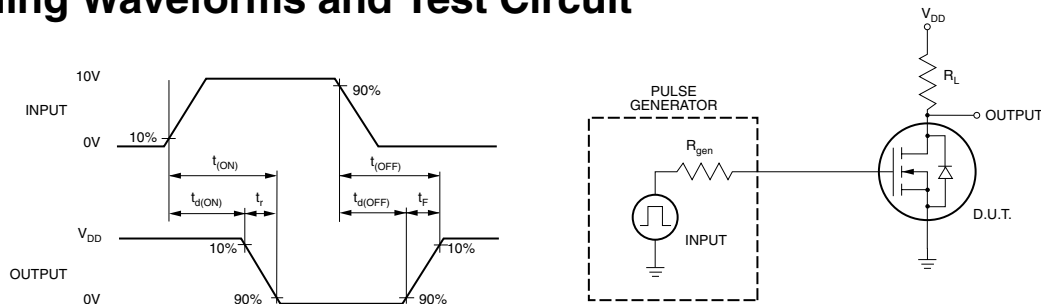
## Electrical Characteristics (@ $25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	250			V	$I_D = 100\mu\text{A}$ , $V_{GS} = 0\text{V}$
$V_{GS(th)}$	Gate Threshold Voltage	0.6		2.0	V	$V_{GS} = V_{DS}$ , $I_D = 1\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.5	mV/ $^\circ\text{C}$	$I_D = 1\text{mA}$ , $V_{GS} = V_{DS}$
$I_{GSS}$	Gate Body Leakage			100	nA	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$
$I_{DSS}$	Zero Gate Voltage Drain Current			1.0	$\mu\text{A}$	$V_{GS} = 0\text{V}$ , $V_{DS} = 100\text{V}$
				10.0	$\mu\text{A}$	$V_{GS} = 0\text{V}$ , $V_{DS} = \text{Max Rating}$
				1.0	mA	$V_{GS} = 0\text{V}$ , $V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	0.6			A	$V_{GS} = 4.5\text{V}$ , $V_{DS} = 25\text{V}$
		1.2				$V_{GS} = 10\text{V}$ , $V_{DS} = 25\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			8.0	$\Omega$	$V_{GS} = 4.5\text{V}$ , $I_D = 150\text{mA}$
				7.0	$\Omega$	$V_{GS} = 10\text{V}$ , $I_D = 1.0\text{A}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.0	%/ $^\circ\text{C}$	$V_{GS} = 4.5\text{V}$ , $I_D = 150\text{mA}$
$G_{FS}$	Forward Transconductance	150			$\text{m}^{\frac{1}{\Omega}}$	$V_{DS} = 25\text{V}$ , $I_D = 200\text{mA}$
$C_{ISS}$	Input Capacitance			110	pF	$V_{GS} = 0\text{V}$ , $V_{DS} = 25\text{V}$ , $f = 1\text{MHz}$
$C_{OSS}$	Common Source Output Capacitance			60		
$C_{RSS}$	Reverse Transfer Capacitance			23		
$t_{d(ON)}$	Turn-ON Delay Time			20	ns	$V_{DD} = 25\text{V}$ $I_D = 150\text{mA}$ $R_{GEN} = 25\Omega$
$t_r$	Rise Time			15		
$t_{d(OFF)}$	Turn-OFF Delay Time			25		
$t_f$	Fall Time			25		
$V_{SD}$	Diode Forward Voltage Drop			1.8	V	$I_{SD} = 200\text{mA}$ , $V_{GS} = 0\text{V}$
$t_{rr}$	Reverse Recovery Time		300		ns	$I_{SD} = 200\text{mA}$ , $V_{GS} = 0\text{V}$

### Notes:

1. All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test: 300 $\mu\text{s}$  pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit



11/12/01