

MOS Field Effect Power Transistors  
**2SK2723**

SWITCHING  
N-CHANNEL POWER MOS FET  
INDUSTRIAL USE

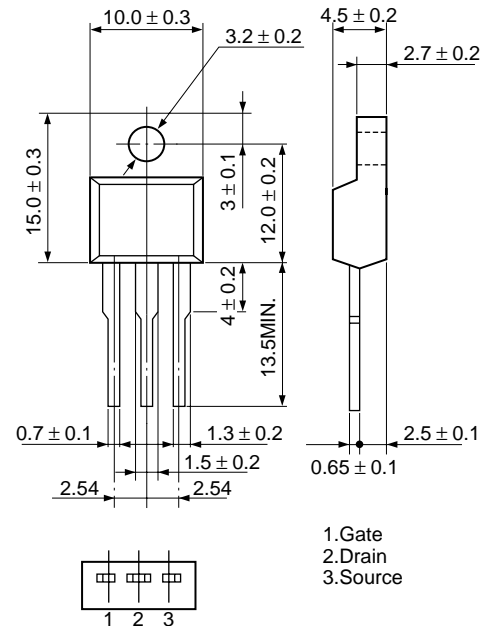
**DESCRIPTION**

This product is N-Channel MOS Field Effect Transistor designed for high current switching applications.

**FEATURES**

- Low On-Resistance  
 $R_{DS(on)1} = 40m\Omega$  Max. ( $V_{GS} = 10 V, I_D = 13 A$ )  
 $R_{DS(on)2} = 60m\Omega$  Max. ( $V_{GS} = 4 V, I_D = 13 A$ )
- Low  $C_{iss}$   $C_{iss} = 830 pF$  Typ.
- Built-in G-S Protection Diode
- Isolated TO-220 Package

**PACKAGE DIMENSIONS**  
(in millimeter)

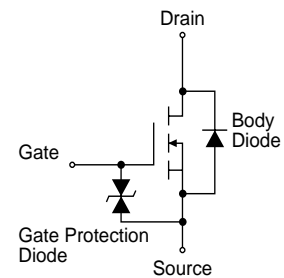


**MP-45F (ISOLATED TO-220)**

**ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$ )**

Drain to Source Voltage	$V_{DSS}$	60	V
Gate to Source Voltage	$V_{GSS}$	$\pm 20$	V
Drain Current (DC)	$I_D (DC)$	$\pm 25$	A
Drain Current (pulse)*	$I_D (pulse)$	$\pm 100$	A
Total Power Dissipation ( $T_A = 25\text{ }^\circ\text{C}$ )	$P_T$	2.0	W
Total Power Dissipation ( $T_c = 25\text{ }^\circ\text{C}$ )	$P_T$	25	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

\* $PW \leq 10 \mu s$ , Duty Cycle  $\leq 1\%$



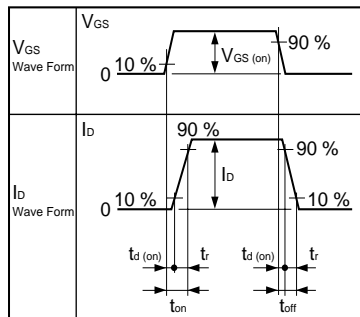
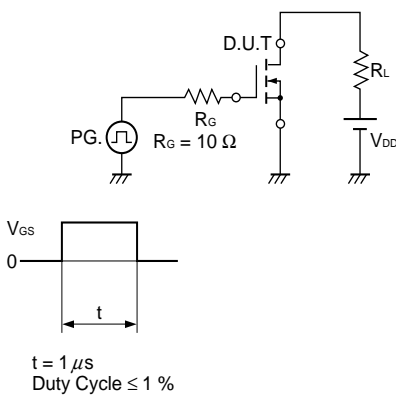
The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device acutally used, an additional protection circiut is externally required if voltage exceeding the rated voltage may be applied to this device.

The information in this document is subject to change without notice.

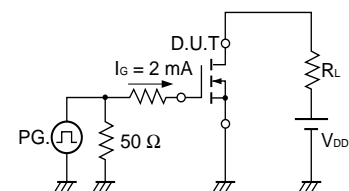
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R <sub>DS (on) 1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 13 A		28	40	mΩ
	R <sub>DS (on) 2</sub>	V <sub>GS</sub> = 4 V, I <sub>D</sub> = 13 A		45	60	mΩ
Gate to Source Cutoff Voltage	V <sub>GS (off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.0	1.6	2.0	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 13 A	8.0	18		S
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0			10	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0			±10	μA
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V V <sub>GS</sub> = 0 f = 1 MHz		830		pF
Output Capacitance	C <sub>oss</sub>			430		pF
Reverse Transfer Capacitance	C <sub>rss</sub>			185		pF
Turn-On Delay Time	t <sub>d (on)</sub>	I <sub>D</sub> = 13 A V <sub>GS (on)</sub> = 10 V		21		ns
Rise Time	t <sub>r</sub>			185		ns
Turn-Off Delay Time	t <sub>d (off)</sub>	V <sub>DD</sub> = 30 V R <sub>G</sub> = 10 Ω		100		ns
Fall Time	t <sub>f</sub>			110		ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = 25 A V <sub>DD</sub> = 48 V V <sub>GS</sub> = 10 V		35		nC
Gate to Source Charge	Q <sub>GS</sub>			2.8		nC
Gate to Drain Charge	Q <sub>GD</sub>			15		nC
Body Diode Forward Voltage	V <sub>F (S-D)</sub>	I <sub>F</sub> = 25 A, V <sub>GS</sub> = 0		1.0		V
Reverse Recovery Time	t <sub>r r</sub>	I <sub>F</sub> = 25 A, V <sub>GS</sub> = 0 di/dt = 100 A/μs		60		ns
Reverse Recovery Charge	Q <sub>r r</sub>			125		nC

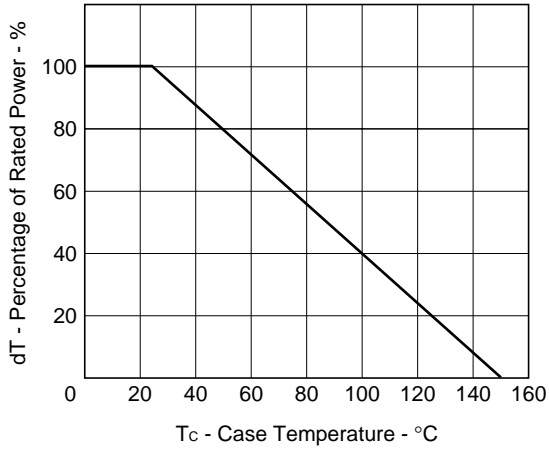
**Test Circuit 1 Switching Time**



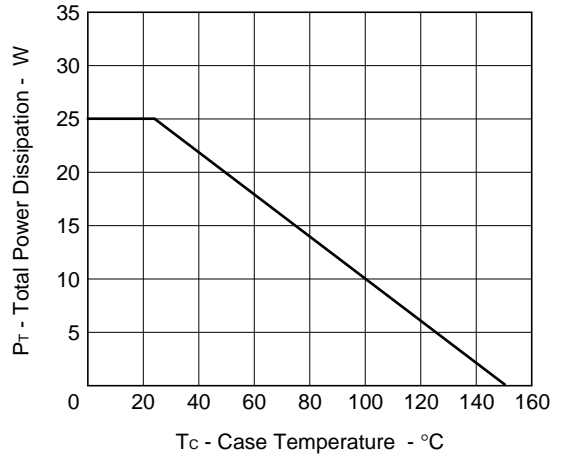
**Test Circuit 2 Gate Charge**



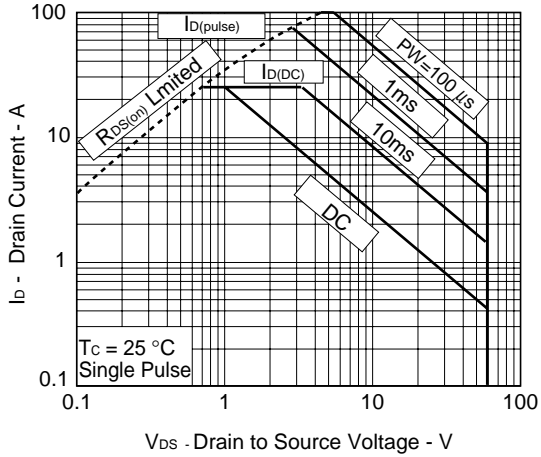
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



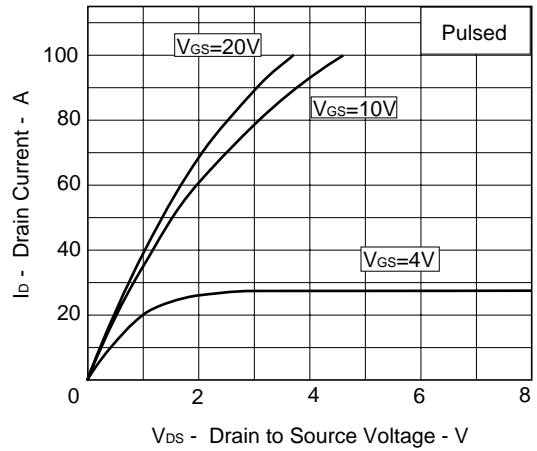
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



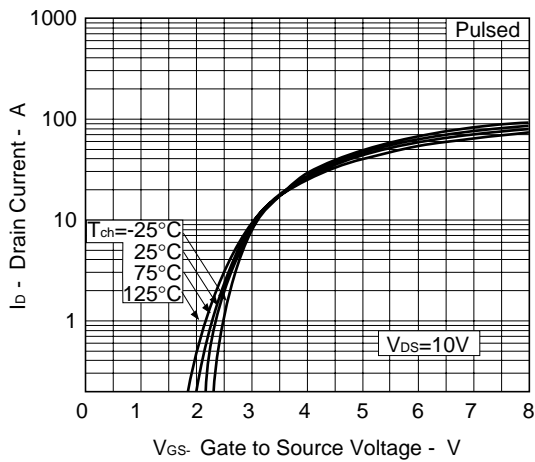
FORWARD BIAS SAFE OPERATING AREA



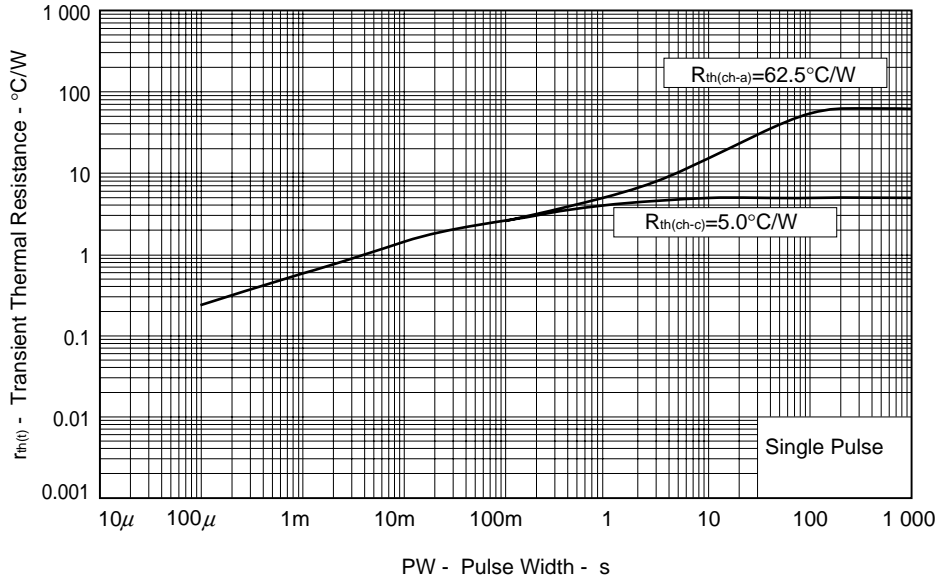
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



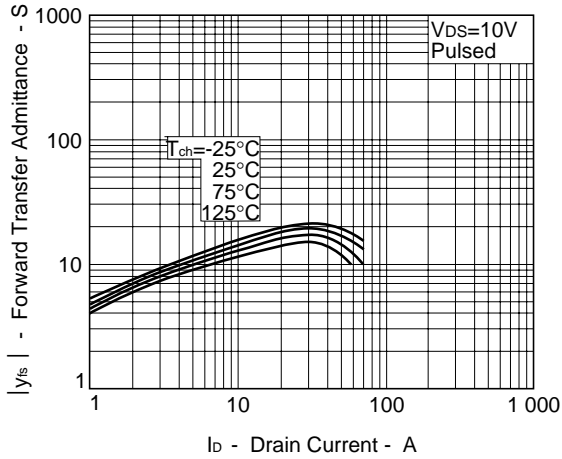
FORWARD TRANSFER CHARACTERISTICS



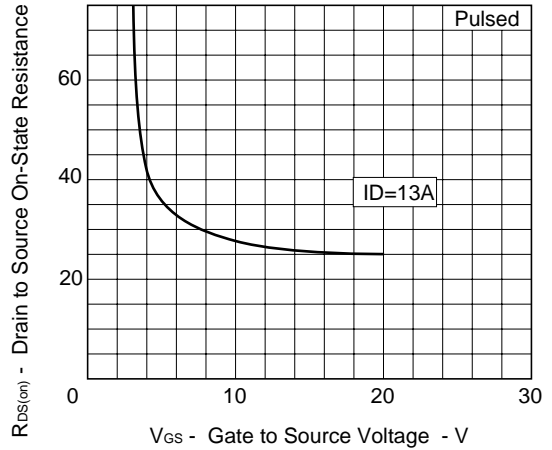
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



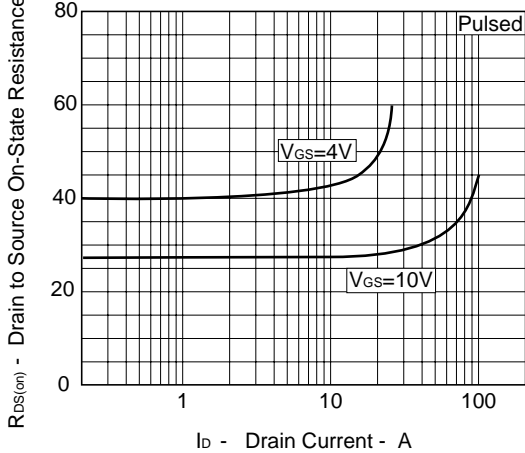
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



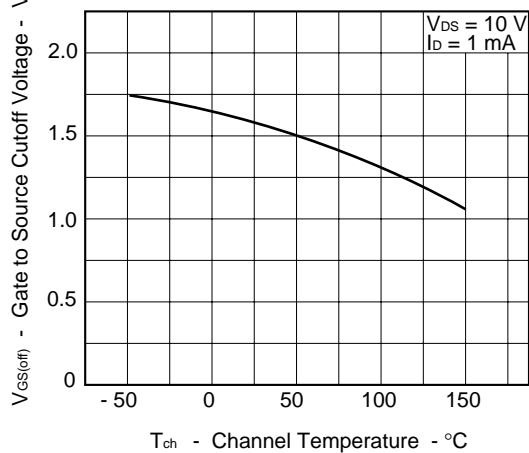
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



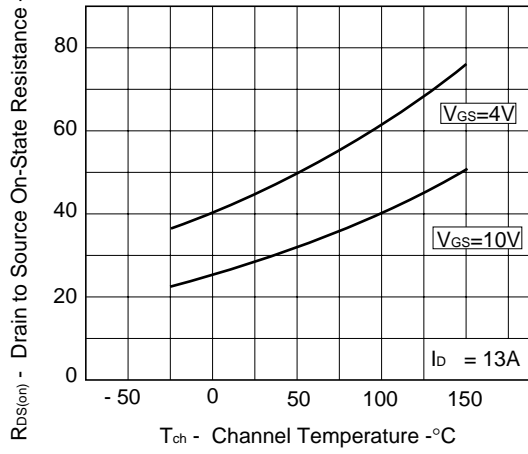
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



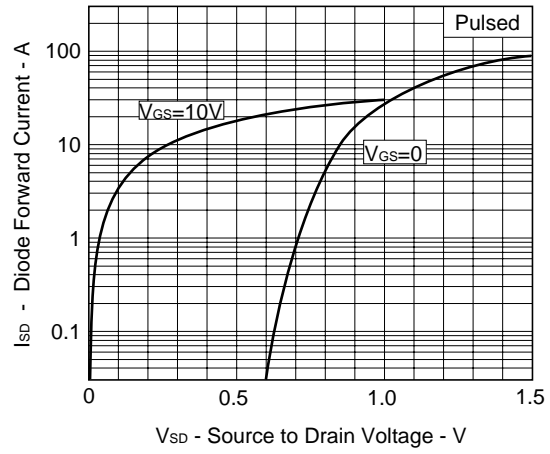
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



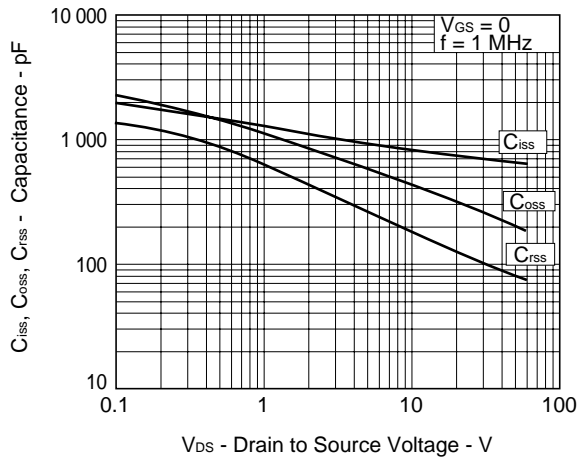
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



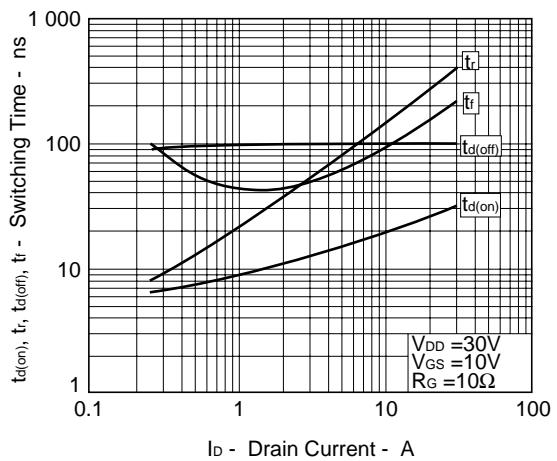
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



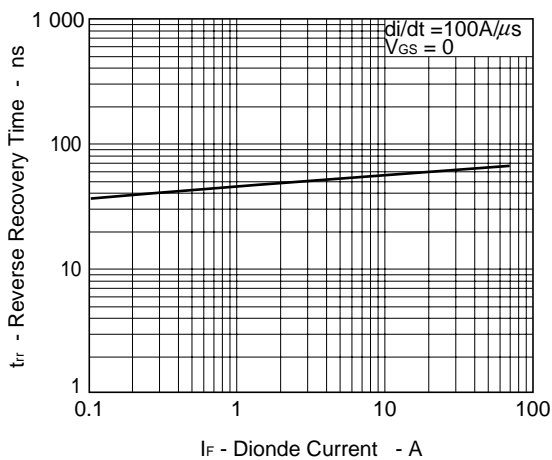
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



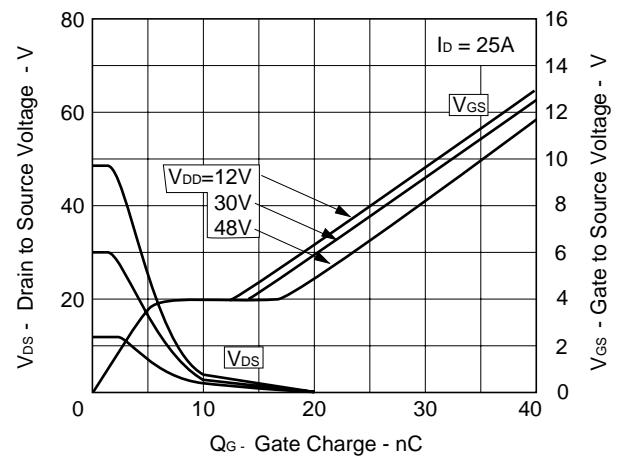
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DIODE CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



**REFERENCE**

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	C10535E
Semiconductor device package manual.	C10943X
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	X10679E
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

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Anti-radioactive design is not implemented in this product.