

## CD4034BM/CD4034BC 8-Stage TRI-STATE® Bidirectional Parallel/Serial Input/Output Bus Register

### General Description

The CD4034BM/CD4034BC is an 8-bit CMOS static shift register with two parallel bidirectional data ports (A and B) which, when combined with serial shifting operations, can be used to (1) bidirectionally transfer parallel data between two buses, (2) convert serial data to parallel form and direct them to either of two buses, (3) store (recirculate) parallel data, or (4) accept parallel data from either of two buses and convert them to serial form. These operations are controlled by five control inputs:

**A ENABLE (AE):** "A" data port is enabled only when AE is at logical "1". This allows the use of a common bus for multiple packages.

**A-BUS-TO-B-BUS/B-BUS-TO-A-BUS (A/B):** This input controls the direction of data flow. When at logical "1", data flows from port A to B (A is input, B is output). When at logical "0", the data flow direction is reversed.

**ASYNCHRONOUS/SYNCHRONOUS (A/S):** When A/S is at logical "0", data transfer occurs at positive transition of the CLOCK. When A/S is at logical "1", data transfer is independent of the CLOCK for parallel operation. In serial mode, A/S input is internally disabled such that operation is always synchronous. (Asynchronous serial operation is not possible.)

**PARALLEL/SERIAL (P/S):** A logical "1" P/S input allows data transfer into the registers via A or B port (synchronous if A/S = logical "0", asynchronous if A/S = logical "1"). A logical "0" P/S allows serial data to transfer into the register synchronously with the positive transition of the CLOCK, independent of the A/S input.

**CLOCK:** Single phase, enabled only in synchronous mode. (Either P/S = logical "1" and A/S = logical "0" or P/S = logical "0".

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave.

All inputs are protected against damage due to static discharge by diode clamps to  $V_{DD}$  and  $V_{SS}$ .

### Features

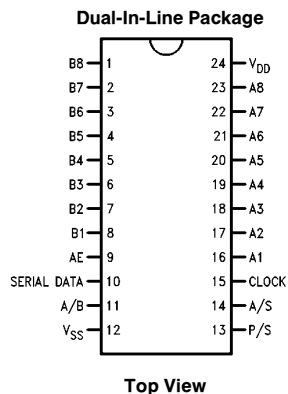
- Wide supply voltage range 3.0V to 18V
- High noise immunity 0.45  $V_{DD}$  (typ.)
- Low power TTL compatibility Fan out of 2 driving 74L or 1 driving 74LS
- RCA CD4034B second source

### Applications

- Parallel Input/Parallel Output
- Parallel Input/Serial Output
- Serial Input/Parallel Output
- Serial Input/Serial Output register
- Shift right/shift left register
- Shift right/shift left with parallel loading
- Address register
- Buffer register
- Bus system register with enable parallel lines at bus side
- Double bus register system
- Up-down Johnson or ring counter
- Pseudo-random code generators
- Sample and hold register (storage, counting, display)
- Frequency and phase comparator

CD4034BM/CD4034BC 8-Stage TRI-STATE Bidirectional Parallel/Serial Input/Output Bus Register

### Connection Diagram



Order Number CD4034B

TL/F/5963-1

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## Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage ( $V_{DD}$ )	$-0.5 V_{DC}$ to $+18 V_{DC}$
Input Voltage ( $V_{IN}$ )	$-0.5 V_{DC}$ to $V_{DD} + 0.5 V_{DC}$
Storage Temp. Range ( $T_S$ )	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Power Dissipation ( $P_D$ )	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature ( $T_L$ )	
(Soldering, 10 seconds)	$260^{\circ}\text{C}$

## Recommended Operating Conditions (Note 2)

DC Supply Voltage ( $V_{DD}$ )	$+3 V_{DC}$ to $+15 V_{DC}$
Input Voltage ( $V_{IN}$ )	$0 V_{DC}$ to $V_{DD} V_{DC}$
Operating Temperature Range ( $T_A$ )	
CD4034BM	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
CD4034BC	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

## DC Electrical Characteristics CD4034BM (Note 2)

Symbol	Parameter	Conditions	$-55^{\circ}\text{C}$		$+25^{\circ}\text{C}$			$+125^{\circ}\text{C}$		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or $V_{SS}$		5			5		150	$\mu\text{A}$
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or $V_{SS}$		10			10		300	$\mu\text{A}$
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or $V_{SS}$		20			20		600	$\mu\text{A}$
$V_{OL}$	Low Level Output Voltage	$V_{DD} = 5V$		0.05			0.05		0.05	V
		$V_{DD} = 10V$		0.05			0.05		0.05	V
		$V_{DD} = 15V$		0.05			0.05		0.05	V
$V_{OH}$	High Level Output Voltage	$V_{DD} = 5V$	4.95		4.95			4.95		V
		$V_{DD} = 10V$	9.95		9.95			9.95		V
		$V_{DD} = 15V$	14.95		14.95			14.95		V
$V_{IL}$	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$		3.0			3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V
$V_{IH}$	High Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
$I_{OL}$	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51			0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3			0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4			2.4		mA
$I_{OH}$	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	-0.64		-0.51			-0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	-1.6		-1.3			-0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	-4.2		-3.4			-2.4		mA
$I_{IN}$	Input Current	$V_{DD} = 15V, V_{IN} = 0V$	-0.1		-0.1	$-10^{-5}$		-1.0		$\mu\text{A}$
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		$10^{-5}$	0.1		1.0	$\mu\text{A}$
$I_{OZ}$	TRI-STATE Leakage Current	$V_{DD} = 15V, V_O = 0V$	-0.1		-0.1	$-10^{-5}$		-1.0		$\mu\text{A}$
		$V_{DD} = 15V, V_O = 15V$		0.1		$10^{-5}$	0.1		1.0	$\mu\text{A}$

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:**  $V_{SS} = 0V$  unless otherwise specified.

**Note 3:**  $I_{OH}$  and  $I_{OL}$  are tested one output at a time.

## DC Electrical Characteristics CD4034BC (Note 2)

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I <sub>DD</sub>	Quiescent Device Current	V <sub>DD</sub> = 5V, V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub>		20			20		150	μA
		V <sub>DD</sub> = 10V, V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub>		40			40		300	μA
		V <sub>DD</sub> = 15V, V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub>		80			80		600	μA
V <sub>OL</sub>	Low Level Output Voltage	V <sub>DD</sub> = 5V		0.05			0.05		0.05	V
		V <sub>DD</sub> = 10V		0.05			0.05		0.05	V
		V <sub>DD</sub> = 15V		0.05			0.05		0.05	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>DD</sub> = 5V	4.95		4.95			4.95		V
		V <sub>DD</sub> = 10V	9.95		9.95			9.95		V
		V <sub>DD</sub> = 15V	14.95		14.95			14.95		V
V <sub>IL</sub>	Low Level Input Voltage	V <sub>DD</sub> = 5V, V <sub>O</sub> = 0.5V or 4.5V		1.5			1.5		1.5	V
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 1.0V or 9.0V		3.0			3.0		3.0	V
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 1.5V or 13.5V		4.0			4.0		4.0	V
V <sub>IH</sub>	High Level Input Voltage	V <sub>DD</sub> = 5V, V <sub>O</sub> = 0.5V or 4.5V	3.5		3.5			3.5		V
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 1.0V or 9.0V	7.0		7.0			7.0		V
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 1.5V or 13.5V	11.0		11.0			11.0		V
I <sub>OL</sub>	Low Level Output Current (Note 3)	V <sub>DD</sub> = 5V, V <sub>O</sub> = 0.4V	0.52		0.44			0.36		mA
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 0.5V	1.3		1.1			0.9		mA
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 1.5V	3.6		3.0			2.4		mA
I <sub>OH</sub>	High Level Output Current (Note 3)	V <sub>DD</sub> = 5V, V <sub>O</sub> = 4.6V	-0.52		-0.44			-0.36		mA
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 9.5V	-1.3		-1.1			-0.9		mA
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 13.5V	-3.6		-3.0			-2.4		mA
I <sub>IN</sub>	Input Current	V <sub>DD</sub> = 15V, V <sub>IN</sub> = 0V	-0.3		-0.3	-10 <sup>-5</sup>		-1.0		μA
		V <sub>DD</sub> = 15V, V <sub>IN</sub> = 15V		0.3		10 <sup>-5</sup>	0.3	1.0		μA
I <sub>OZ</sub>	TRI-STATE Leakage Current	V <sub>DD</sub> = 15V, V <sub>O</sub> = 0V	-0.3		-0.3	-10 <sup>-5</sup>		-1.0		μA
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 15V		0.3		10 <sup>-5</sup>	0.3	1.0		μA

## AC Electrical Characteristics\*

T<sub>A</sub> = 25°C, C<sub>L</sub> = 50 pF, R<sub>L</sub> = 200k, input t<sub>r</sub> = t<sub>f</sub> = 20 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Time, A (B) Synchronous Parallel Data or Serial Data Input, B (A) Parallel Data Output	V <sub>DD</sub> = 5V		280	700	ns
		V <sub>DD</sub> = 10V		120	270	ns
		V <sub>DD</sub> = 15V		85	190	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Time, A (B) A (B) Asynchronous Parallel Data Input, B (A) Parallel Data Output	V <sub>DD</sub> = 5V		280	700	ns
		V <sub>DD</sub> = 10V		120	270	ns
		V <sub>DD</sub> = 15V		85	190	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Propagation Delay Time from A/B or AE to High Impedance State at A Outputs or from A/B to High Impedance State at B Outputs	V <sub>DD</sub> = 5V, R <sub>L</sub> = 1.0 kΩ		95	220	ns
		V <sub>DD</sub> = 10V, R <sub>L</sub> = 1.0 kΩ		60	130	ns
		V <sub>DD</sub> = 15V, R <sub>L</sub> = 1.0 kΩ		45	100	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Propagation Delay Time from A/B or AE to Logical "1" or Logical "0" State at A Outputs or from A/B to Logical "1" or Logical "0" State at B Outputs	V <sub>DD</sub> = 5V, R <sub>L</sub> = 1.0 kΩ		180	480	ns
		V <sub>DD</sub> = 10V, R <sub>L</sub> = 1.0 kΩ		75	190	ns
		V <sub>DD</sub> = 15V, R <sub>L</sub> = 1.0 kΩ		55	140	ns

## AC Electrical Characteristics\*

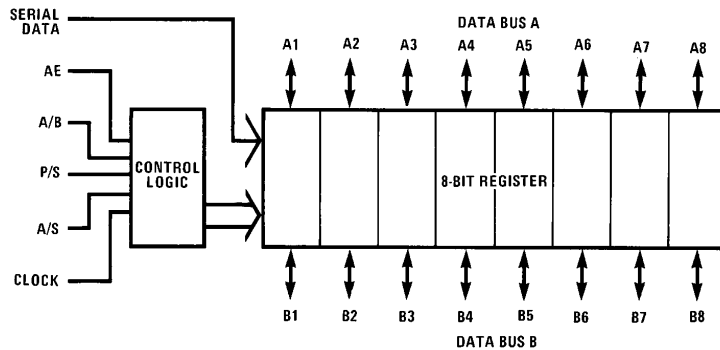
$T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}$ , input  $t_r = t_f = 20\text{ ns}$ , unless otherwise specified (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{THL}, t_{TLH}$	Output Transition Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		100 50 40	200 100 80	ns ns ns
$f_{CL}$	Maximum Clock Input Frequency	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	2 5 7	4 10 14		MHz MHz MHz
$t_{WL}, t_{WH}$	Minimum Clock Pulse Width	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		125 50 35	250 100 70	ns ns ns
$t_{RCL}, t_{FCL}$	Maximum Clock Rise & Fall Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	15 15 15			$\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$
$t_{SU}$	Parallel (A or B) and Serial Data Setup Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		25 10 7	70 30 20	ns ns ns
$t_{SU}$	Control Inputs AE, A/B, P/S, A/S Setup Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		110 35 60	280 100 60	ns ns ns
$t_{WH}$	Minimum High Level AE, A/B, P/S, A/S Pulse Width	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		160 70 40	400 160 90	ns ns ns
$C_{IN}$	Average Input Capacitance	A and B Data I/O and A/B Control Input Any Other Input		7 5	15 7.5	pF pF
$C_{PD}$	Power Dissipation Capacitance	(Note 4)		155		pF

\*AC Parameters are guaranteed by DC correlated testing.

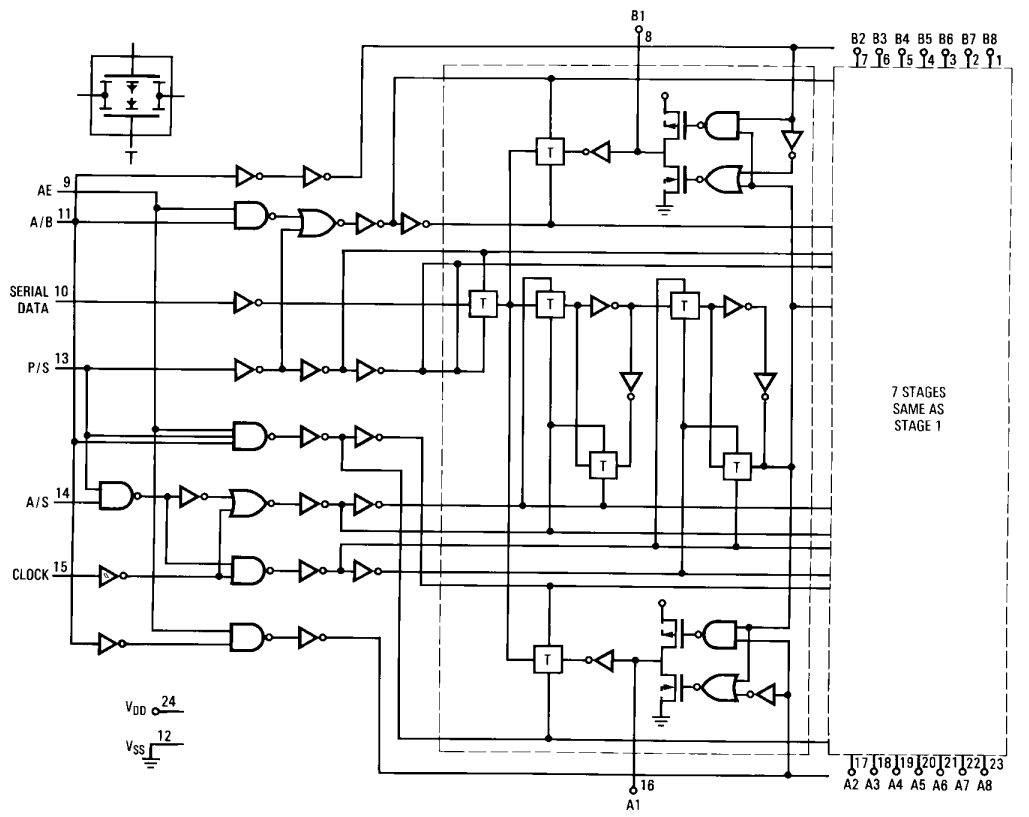
**Note 4:**  $C_{PD}$  determines the no-load power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

## Logic Diagram



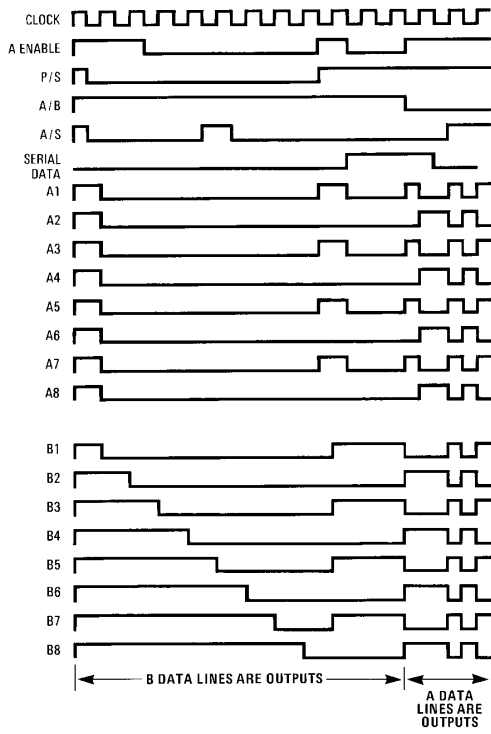
TL/F/5963-2

# Schematic Diagram

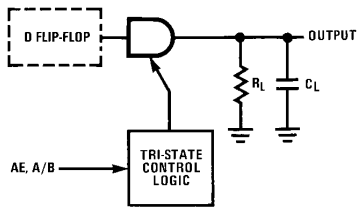


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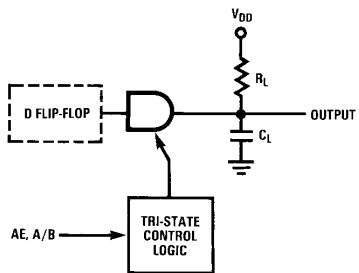
# Switching Time Waveforms and Test Circuits



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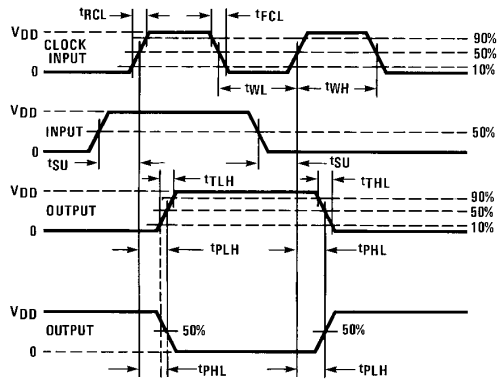


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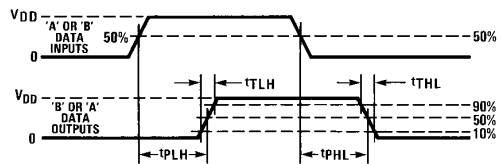
## Synchronous Operation



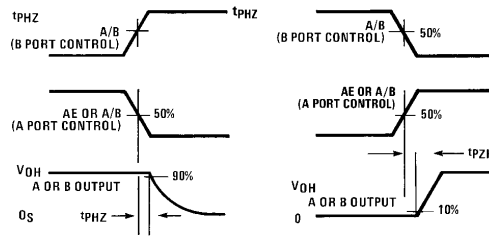
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$t_r, CL = t_f, CL = 20 \text{ ns}$

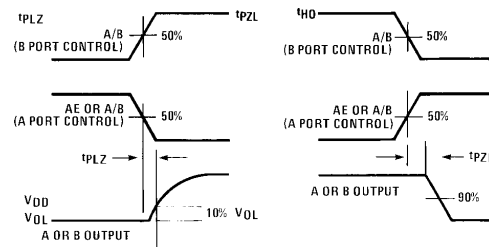
## Asynchronous Operation



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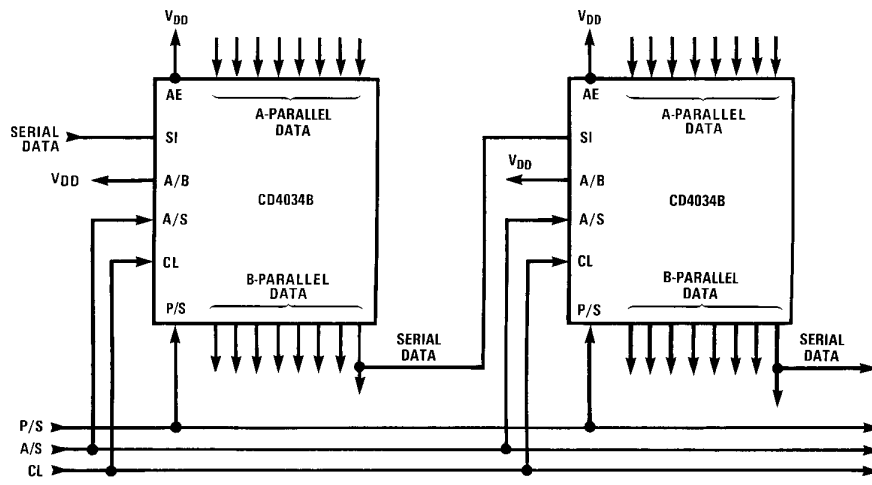
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TL/F/5963-10

## Applications

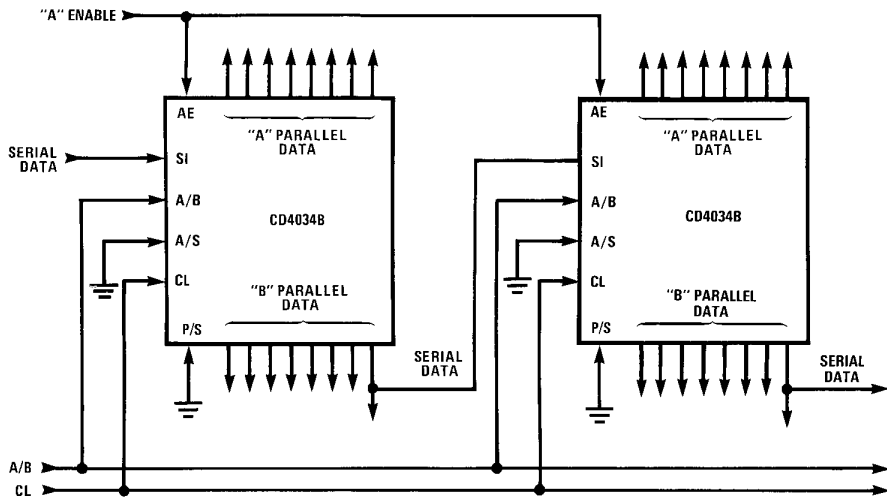
16-Bit Parallel In/Parallel Out, Parallel In/Serial Out,  
Serial In/Parallel Out, Serial In/Serial Out Register



TL/F/5963-11

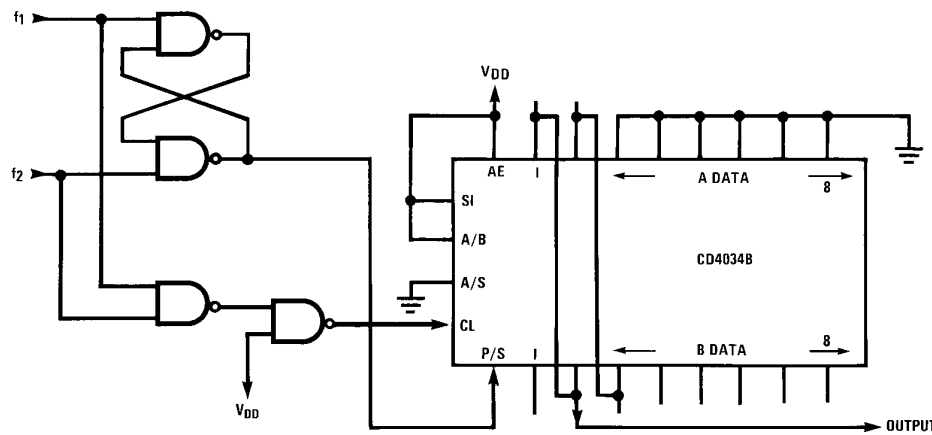
## Applications (Continued)

### 16-Bit Serial In/Gated Parallel Out Register

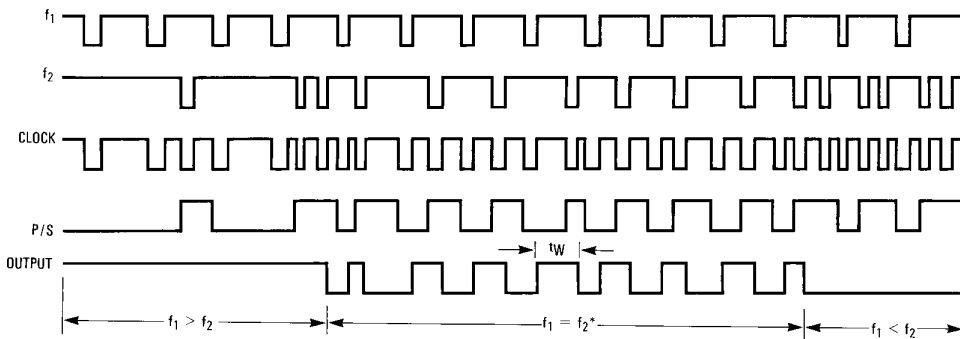


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### Frequency and Phase Comparator



TL/F/5963-13



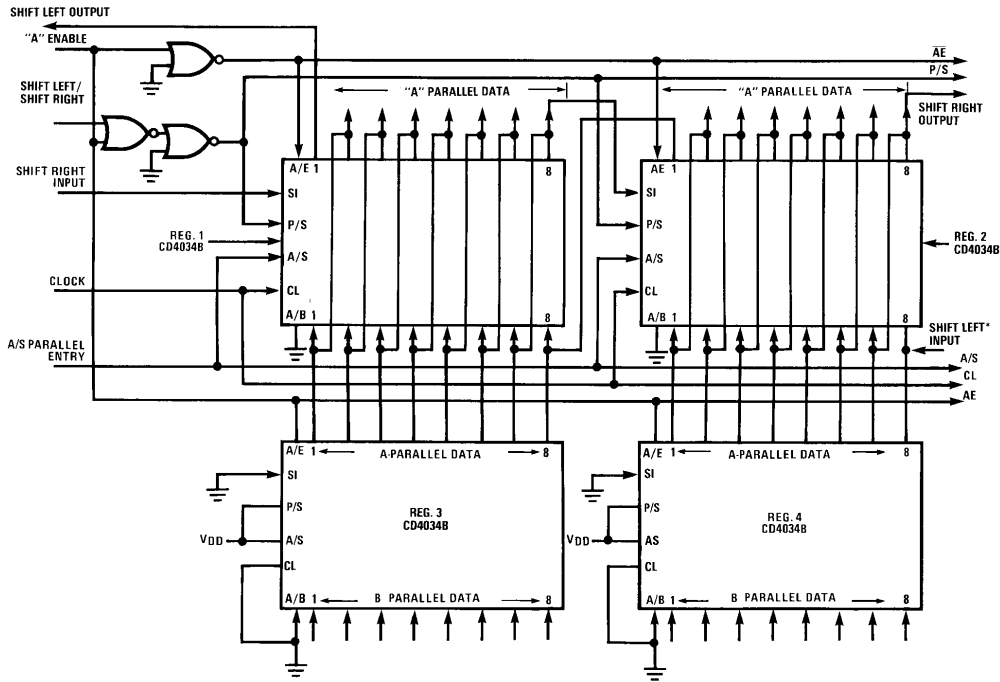
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\*When  $f_1 = f_2$ ,  $t_W$  is proportional to the phase of  $f_1$  with respect to  $f_2$ .



## Applications (Continued)

### Shift Right/Shift Left with Parallel Inputs



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Shift left input must be disabled during parallel entry.

A "High" ("Low") on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Registers 1 and 2 and enables the "A" data

lines on Registers 3 and 4 and allows parallel data into Registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Registers 3 and 4 and associated logic are not required.

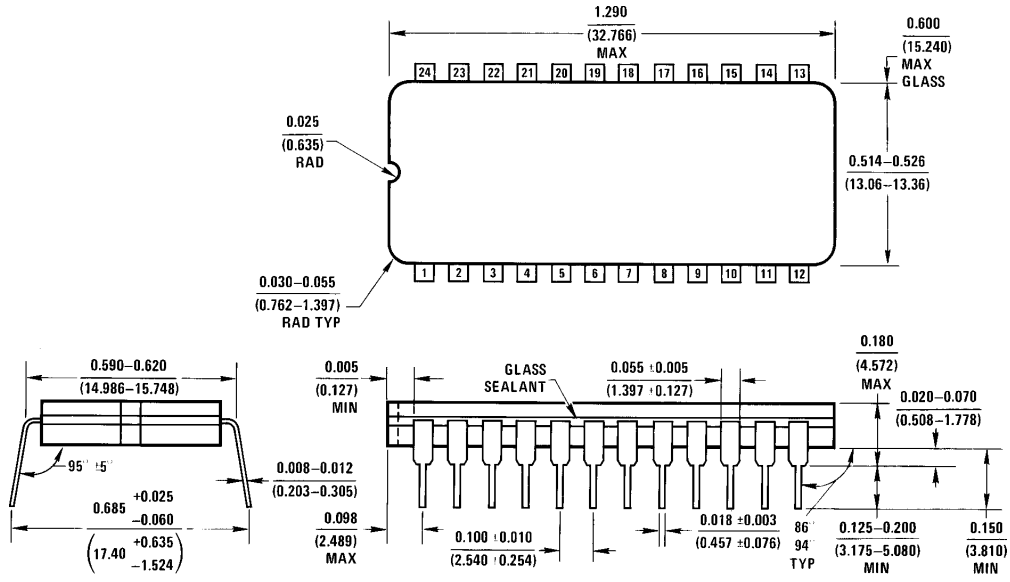
## Truth Table

"A" Enable	P/S	A/B	A/S	Mode	Operation*
0	0	0	X	Serial	Synchronous Serial data input, A- and B-Parallel data outputs disabled.
0	0	1	X	Serial	Synchronous Serial data input, B-Parallel data output.
0	1	0	0	Parallel	B Synchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	0	1	Parallel	B Asynchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	1	0	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs, synchronous data recirculation.
0	1	1	1	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs, asynchronous data recirculation.
1	0	0	X	Serial	Synchronous Serial data input, A-Parallel data output.
1	0	1	X	Serial	Synchronous Serial data input, B-Parallel data output.
1	1	0	0	Parallel	B Synchronous Parallel data input, A-Parallel data output.
1	1	0	1	Parallel	B Asynchronous Parallel data input, A-Parallel data output.
1	1	1	0	Parallel	A Synchronous Parallel data input, B-Parallel data output.
1	1	1	1	Parallel	A Asynchronous Parallel data input, B-Parallel data output.

X = Don't Care

\*For synchronous operation (serial mode or when A/S = 0 in parallel mode), outputs change state at positive transition of the clock.

**Physical Dimensions** inches (millimeters)

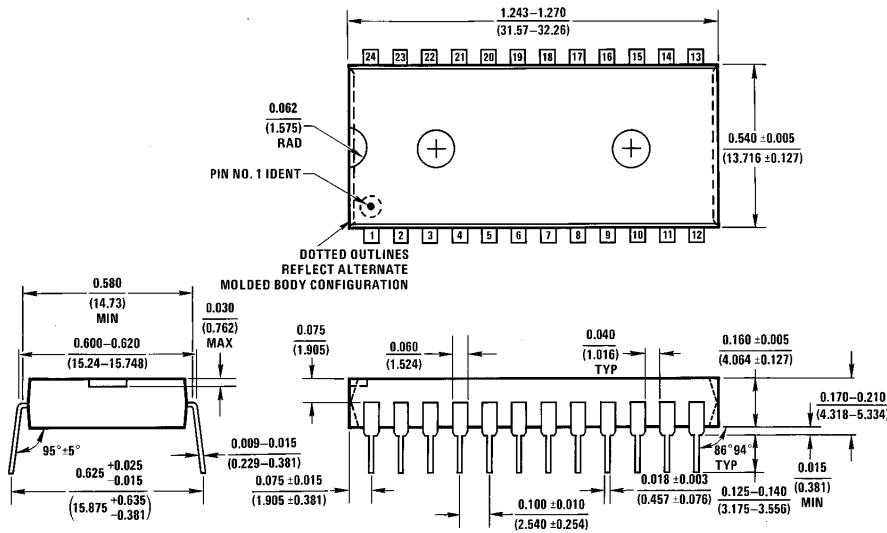


**Ceramic Dual-In-Line Package (J)**  
**Order Number CD4034BMJ or CD4034BCJ**  
**NS Package Number J24A**

J24A (REV H)

CD4034BM/CD4034BC 8-Stage TRI-STATE Bidirectional Parallel/Serial Input/Output Bus Register

**Physical Dimensions** inches (millimeters) (Continued)



**Molded Dual-In-Line Package (N)**  
**Order Number CD4034BMN or CD4034BCN**  
**NS Package Number N24A**

N24A (REV E)

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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