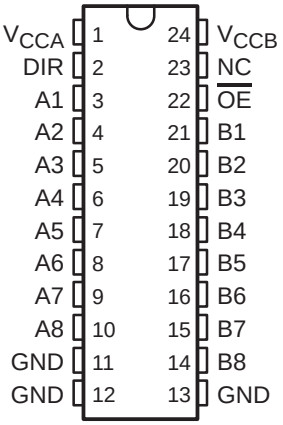
- **Bidirectional Voltage Translator**
- **2.3 V to 3.6 V on A Port and 3 V to 5.5 V on B Port**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DB, DW, NS, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails. The B port is designed to track V_{CCB}, which accepts voltages from 3 V to 5.5 V, and the A port is designed to track V_{CCA}, which operates at 2.3 V to 3.6 V. This allows for translation from a 3.3-V to a 5-V system environment and vice versa, or from a 2.5-V to a 3.3-V system environment and vice versa.

The SN74LVCC3245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

ORDERING INFORMATION

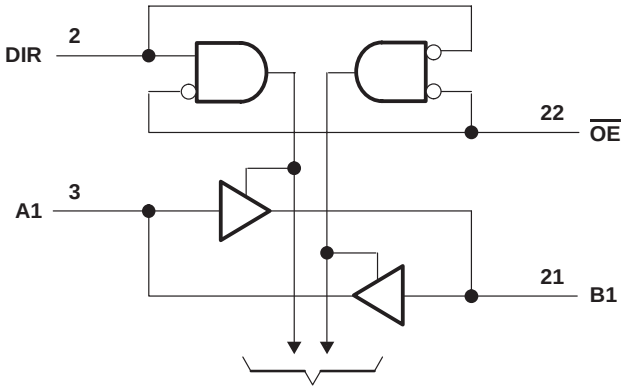
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube of 25	SN74LVCC3245ADW	LVCC3245A
		Reel of 2000	SN74LVCC3245ADWR	
	SOP – NS	Reel of 2000	SN74LVCC3245ANSR	LVCC3245A
	SSOP – DB	Reel of 2000	SN74LVCC3245ADBR	LH245A
	TSSOP – PW	Tube of 60	SN74LVCC3245APW	LH245A
		Reel of 2000	SN74LVCC3245APWR	
		Reel of 250	SN74LVCC3245APWT	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each transceiver)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CCA} and V_{CCB} . . . . . –0.5 V to 6 V
Input voltage range, V_I: All A ports (see Note 1) . . . . . –0.5 V to V_{CCA} + 0.5 V
All B ports (see Note 2) . . . . . –0.5 V to V_{CCB} + 0.5 V
Except I/O ports (see Note 1) . . . . . –0.5 V to V_{CCA} + 0.5 V
Output voltage range, V_O (see Note 2): All A ports . . . . . –0.5 V to V_{CCA} + 0.5 V
All B ports . . . . . –0.5 V to V_{CCB} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Continuous output current, I_O . . . . . ±50 mA
Continuous current through V_{CCA}, V_{CCB}, or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package . . . . . 63°C/W
DW package . . . . . 46°C/W
NS package . . . . . 65°C/W
PW package . . . . . 88°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This value is limited to 4.6 V maximum.
2. This value is limited to 6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			V_{CCA}	V_{CCB}	MIN	NOM	MAX	UNIT
V_{CCA}	Supply voltage				2.3	3.3	3.6	V
V_{CCB}	Supply voltage				3	5	5.5	V
V_{IHA}	High-level input voltage	$V_{OB} \le 0.1$ V or $V_{OB} \ge V_{CCB} - 0.1$ V	2.3 V	3 V	1.7			V
			2.7 V	3 V	2			
			3 V	3.6 V	2			
			3.6 V	5.5 V	2			
V_{IHB}	High-level input voltage	$V_{OA} \le 0.1$ V or $V_{OA} \ge V_{CCA} - 0.1$ V	2.3 V	3 V	2			V
			2.7 V	3 V	2			
			3 V	3.6 V	2			
			3.6 V	5.5 V	3.85			
V_{ILA}	Low-level input voltage	$V_{OB} \le 0.1$ V or $V_{OB} \ge V_{CCB} - 0.1$ V	2.3 V	3 V			0.7	V
			2.7 V	3 V			0.8	
			3 V	3.6 V			0.8	
			3.6 V	5.5 V			0.8	
V_{ILB}	Low-level input voltage	$V_{OA} \le 0.1$ V or $V_{OA} \ge V_{CCA} - 0.1$ V	2.3 V	3 V			0.8	V
			2.7 V	3 V			0.8	
			3 V	3.6 V			0.8	
			3.6 V	5.5 V			1.65	
V_{IH}	High-level input voltage (control pins)	$V_{OB} \le 0.1$ V or $V_{OB} \ge V_{CCB} - 0.1$ V	2.3 V	3 V	1.7			V
			2.7 V	3 V	2			
			3 V	3.6 V	2			
			3.6 V	5.5 V	2			
		$V_{OA} \le 0.1$ V or $V_{OA} \ge V_{CCA} - 0.1$ V	2.3 V	3 V	2			
			2.7 V	3 V	2			
			3 V	3.6 V	2			
			3.6 V	5.5 V	2			
V_{IL}	Low-level input voltage (control pins)	$V_{OB} \le 0.1$ V or $V_{OB} \ge V_{CCB} - 0.1$ V	2.3 V	3 V			0.7	V
			2.7 V	3 V			0.8	
			3 V	3.6 V			0.8	
			3.6 V	5.5 V			0.8	
		$V_{OA} \le 0.1$ V or $V_{OA} \ge V_{CCA} - 0.1$ V	2.3 V	3 V			0.8	
			2.7 V	3 V			0.8	
			3 V	3.6 V			0.8	
			3.6 V	5.5 V			0.8	
V_{IA}	Input voltage				0		V_{CCA}	V
V_{IB}	Input voltage				0		V_{CCB}	V
V_{OA}	Output voltage				0		V_{CCA}	V
V_{OB}	Output voltage				0		V_{CCB}	V

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions (see Note 4) (continued)

		V_{CCA}	V_{CCB}	MIN	NOM	MAX	UNIT
I_{OHA}	High-level output current	2.3 V	3 V			–8	mA
		2.7 V	3 V			–12	
		3.3 V	3 V			–24	
I_{OHB}	High-level output current	2.3 V	3.3 V			–12	mA
		2.7 V	3.3 V			–12	
		3.3 V	3 V			–24	
I_{OLA}	Low-level output current	2.3 V	3 V			8	mA
		2.7 V	3 V			12	
		3.3 V	3 V			24	
I_{OLB}	Low-level output current	2.3 V	3.3 V			12	mA
		2.7 V	3.3 V			12	
		3.3 V	3 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate					10	ns/V
T_A	Operating free-air temperature			–40		85	°C

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
V_{OHA}		I_{OH} = –100 µA	3 V	3 V	2.9	3		V
		I_{OH} = –8 mA	2.3 V	3 V	2			
		I_{OH} = –12 mA	2.7 V	3 V	2.2	2.5		
			3 V	3 V	2.4	2.8		
		I_{OH} = –24 mA	3 V	3 V	2.2	2.6		
			2.7 V	4.5 V	2	2.3		
V_{OHB}		I_{OH} = –100 µA	3 V	3 V	2.9	3		V
		I_{OH} = –12 mA	2.3 V	3 V	2.4			
			2.7 V	3 V	2.4	2.8		
		I_{OH} = –24 mA	3 V	3 V	2.2	2.6		
			2.7 V	4.5 V	3.2	4.2		
V_{OLA}		I_{OL} = 100 µA	3 V	3 V			0.1	V
		I_{OL} = 8 mA	2.3 V	3 V			0.6	
		I_{OL} = 12 mA	2.7 V	3 V		0.1	0.5	
		I_{OL} = 24 mA	3 V	3 V		0.2	0.5	
			2.7 V	4.5 V		0.2	0.5	
V_{OLB}		I_{OL} = 100 µA	3 V	3 V			0.1	V
		I_{OL} = 12 mA	2.3 V	3 V			0.4	
		I_{OL} = 24 mA	3 V	3 V		0.2	0.5	
				4.5 V		0.2	0.5	
I_I	Control inputs	$V_I = V_{CCA}$ or GND	3.6 V	3.6 V		±0.1	±1	µA
				5.5 V		±0.1	±1	
I_{OZ}†	A or B ports	$V_O = V_{CCA/B}$ or GND, $V_I = V_{IL}$ or V_{IH}	3.6 V	3.6 V		±0.5	±5	µA
I_{CCA}	B to A	A port = V_{CCA} or GND, I_O = 0	3.6 V	Open		5	50	µA
		B port = V_{CCB} or GND, I_O = 0	3.6 V	3.6 V		5	50	
				5.5 V		5	50	
I_{CCB}	A to B	A port = V_{CCA} or GND, I_O = 0	3.6 V	3.6 V		5	50	µA
				5.5 V		8	80	
ΔI_{CCA}‡	A port	$\underline{V_I} = V_{CCA}$ – 0.6 V, Other inputs at V_{CCA} or GND, $\underline{OE}$ at GND and DIR at V_{CCA}	3.6 V	3.6 V		0.35	0.5	mA
	$\overline{OE}$	$V_I = V_{CCA}$ – 0.6 V, Other inputs at V_{CCA} or GND, DIR at V_{CCA}	3.6 V	3.6 V		0.35	0.5	
	DIR	$\underline{V_I} = V_{CCA}$ – 0.6 V, Other inputs at V_{CCA} or GND, $\underline{OE}$ at GND	3.6 V	3.6 V		0.35	0.5	
ΔI_{CCB}‡	B port	$\underline{V_I} = V_{CCB}$ – 2.1 V, Other inputs at V_{CCB} or GND, $\underline{OE}$ at GND and DIR at GND	3.6 V	5.5 V		1	1.5	mA
C_i	Control inputs	$V_I = V_{CCA}$ or GND	Open	Open		4		pF
C_{io}	A or B ports	$V_O = V_{CCA/B}$ or GND	3.3 V	5 V		18.5		pF

† For I/O ports, the parameter I_{OZ} includes the input leakage current.
‡ This is the increase in supply current for each input that is at one of the specified voltage levels, rather than 0 V or the associated V_{CC}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V		V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V		V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	A	B	1	9.4	1	6	1	7.1	ns
t_{PLH}			1	9.1	1	5.3	1	7.2	
t_{PHL}	B	A	1	11.2	1	5.8	1	6.4	ns
t_{PLH}			1	9.9	1	7	1	7.6	
t_{PZL}	$\overline{OE}$	A	1	14.5	1	9.2	1	9.7	ns
t_{PZH}			1	12.9	1	9.5	1	9.5	
t_{PZL}	$\overline{OE}$	B	1	13	1	8.1	1	9.2	ns
t_{PZH}			1	12.8	1	8.4	1	9.9	
t_{PLZ}	$\overline{OE}$	A	1	7.1	1	7	1	6.6	ns
t_{PHZ}			1	6.9	1	7.8	1	6.9	
t_{PLZ}	$\overline{OE}$	B	1	8.8	1	7.3	1	7.5	ns
t_{PHZ}			1	8.9	1	7	1	7.9	

operating characteristics, V_{CCA} = 3.3 V, V_{CCB} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50, f = 10 MHz	38	pF
		Outputs disabled		4.5	

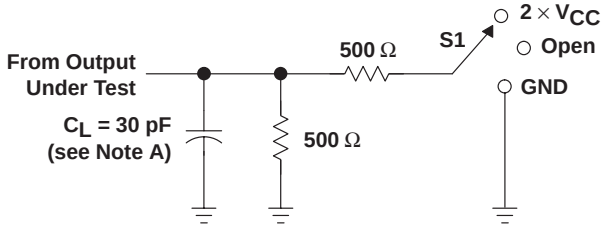
power-up considerations†

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. Take these precautions to guard against such power-up problems.

1. Connect ground before any supply voltage is applied.
2. Next, power up the control side of the device (V_{CCA} for all four of these devices).
3. Tie $\overline{OE}$ to V_{CCA} with a pullup resistor so that it ramps with V_{CCA}.
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA}. Otherwise, keep DIR low.

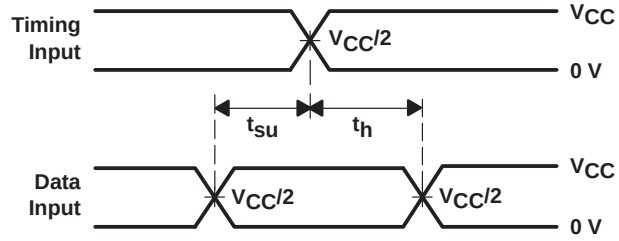
† Refer to the TI application report, *Texas Instruments Voltage-Level-Translation Devices*, literature number SCEA021.

PARAMETER MEASUREMENT INFORMATION FOR A PORT
V_{CCA} = 2.5 V ± 0.2 V AND V_{CCB} = 3.3 V ± 0.3 V

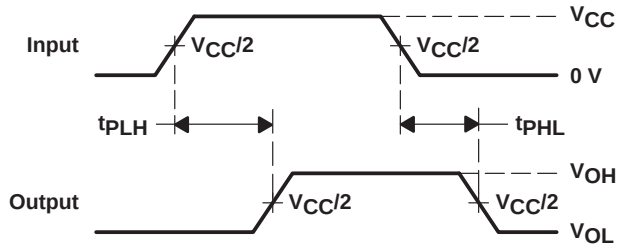


TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CC} GND

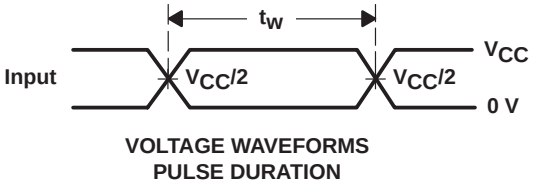
LOAD CIRCUIT



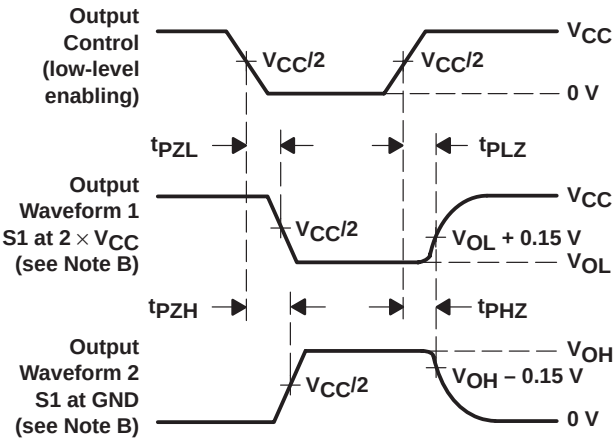
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

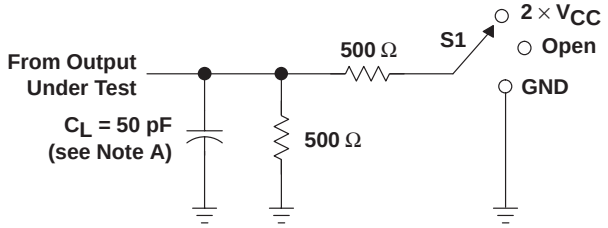


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

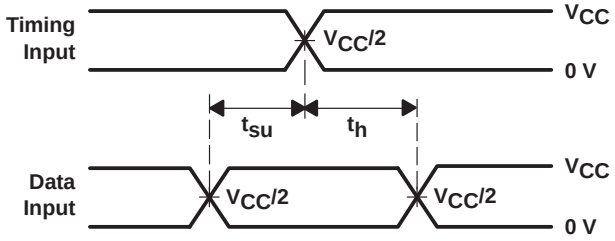
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION FOR B PORT
V_{CCA} = 2.5 V ± 0.2 V AND V_{CCB} = 3.3 V ± 0.3 V

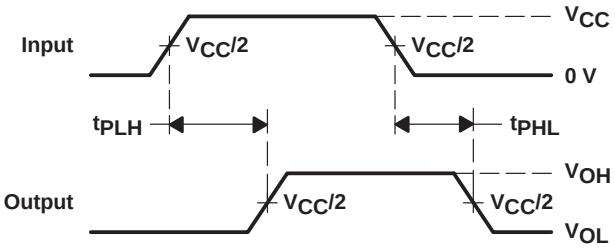


TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CC} GND

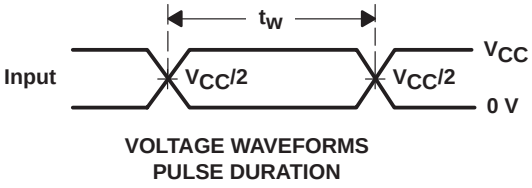
LOAD CIRCUIT



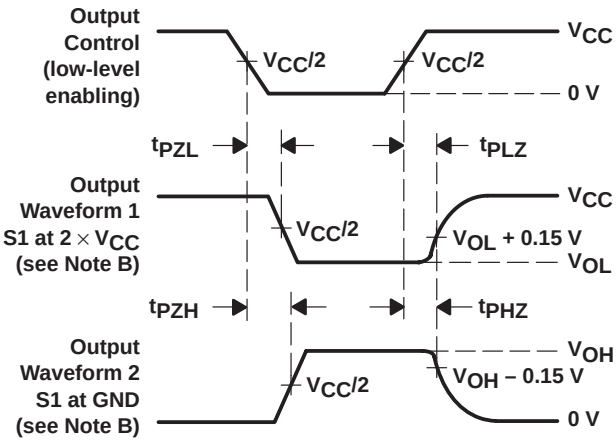
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

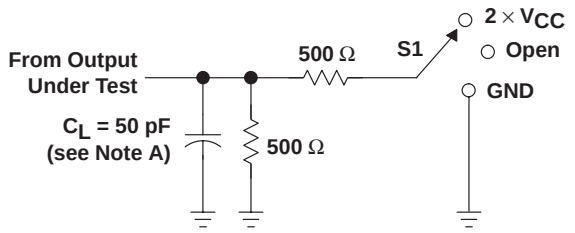


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

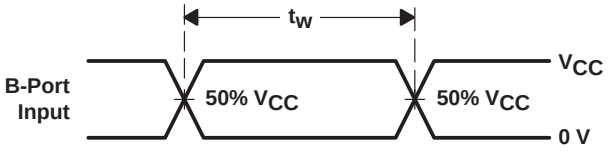
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION FOR B PORT
V_{CCA} = 3.6 V AND V_{CCB} = 5.5 V

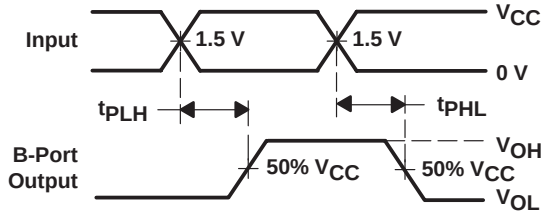


LOAD CIRCUIT

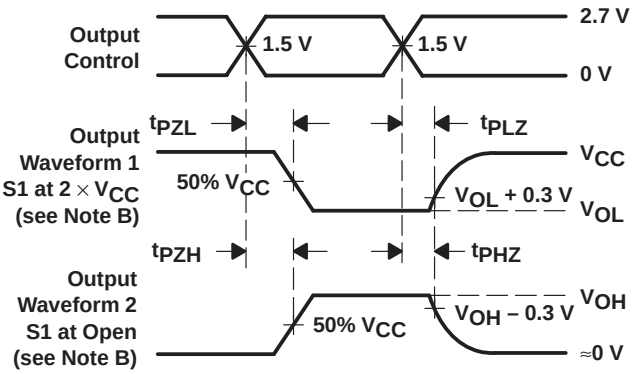
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

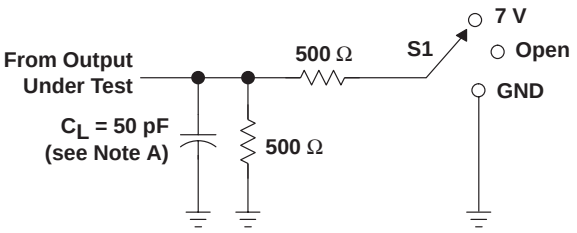


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

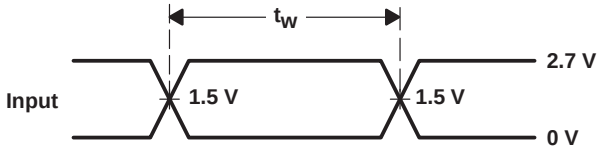
Figure 3. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION FOR A AND B PORT
V_{CCA} AND V_{CCB} = 3.6 V

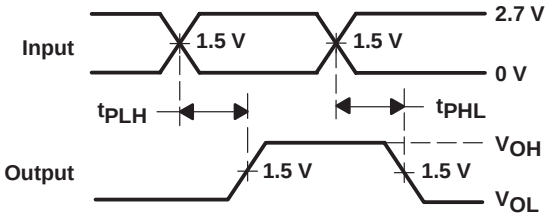


LOAD CIRCUIT

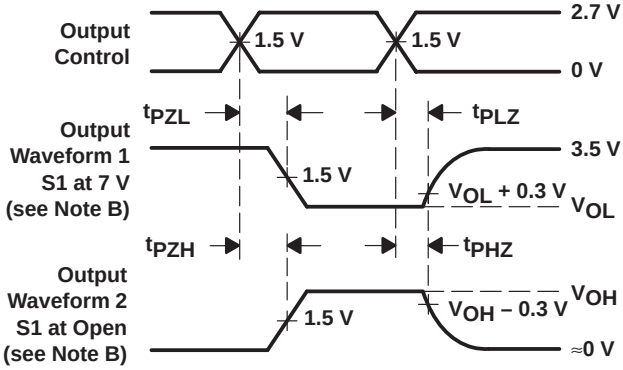
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

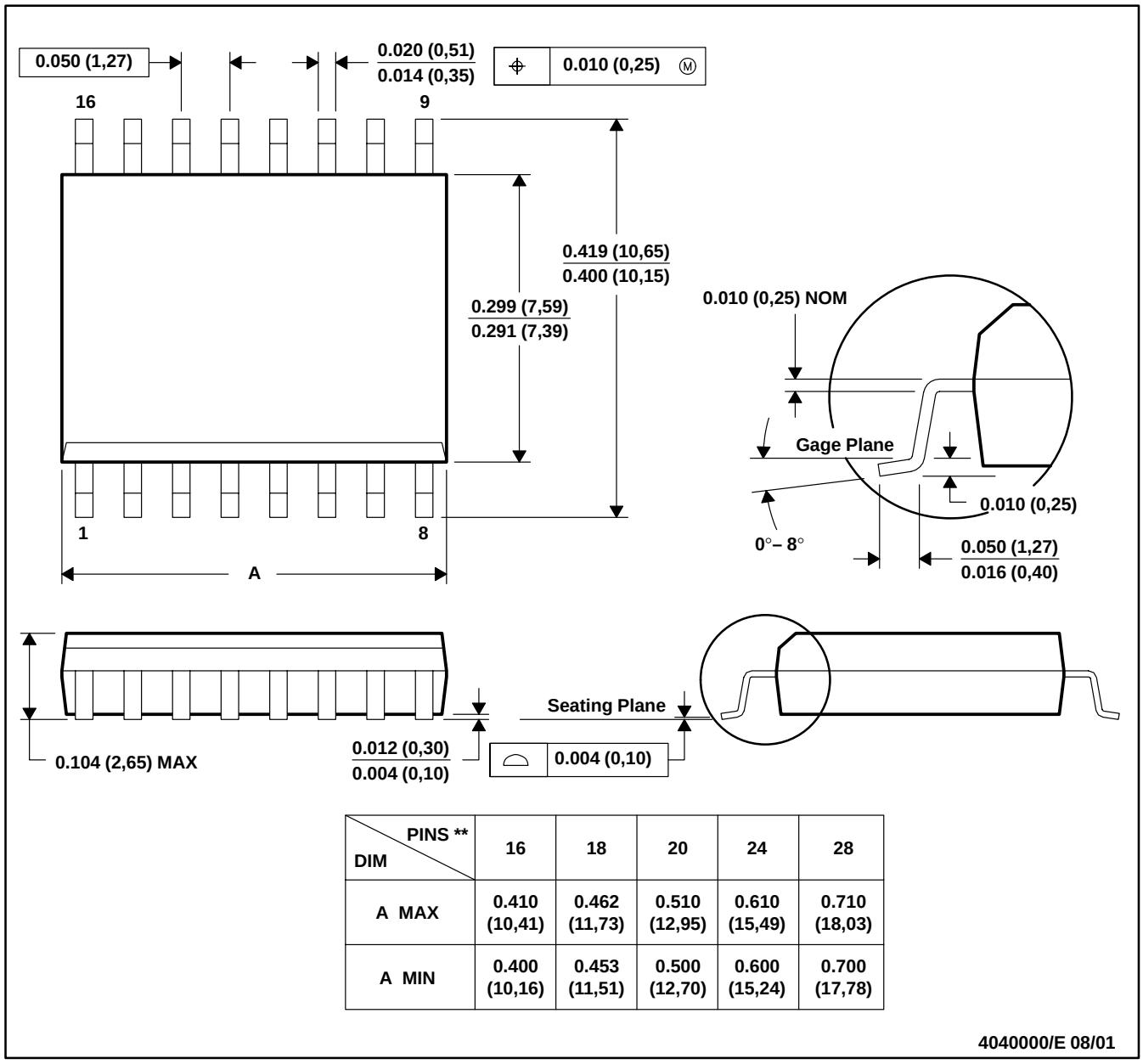
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

MSOI003E – JANUARY 1995 – REVISED SEPTEMBER 2001

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN



DIM \ PINS **	16	18	20	24	28
A MAX	0.410 (10,41)	0.462 (11,73)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.453 (11,51)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

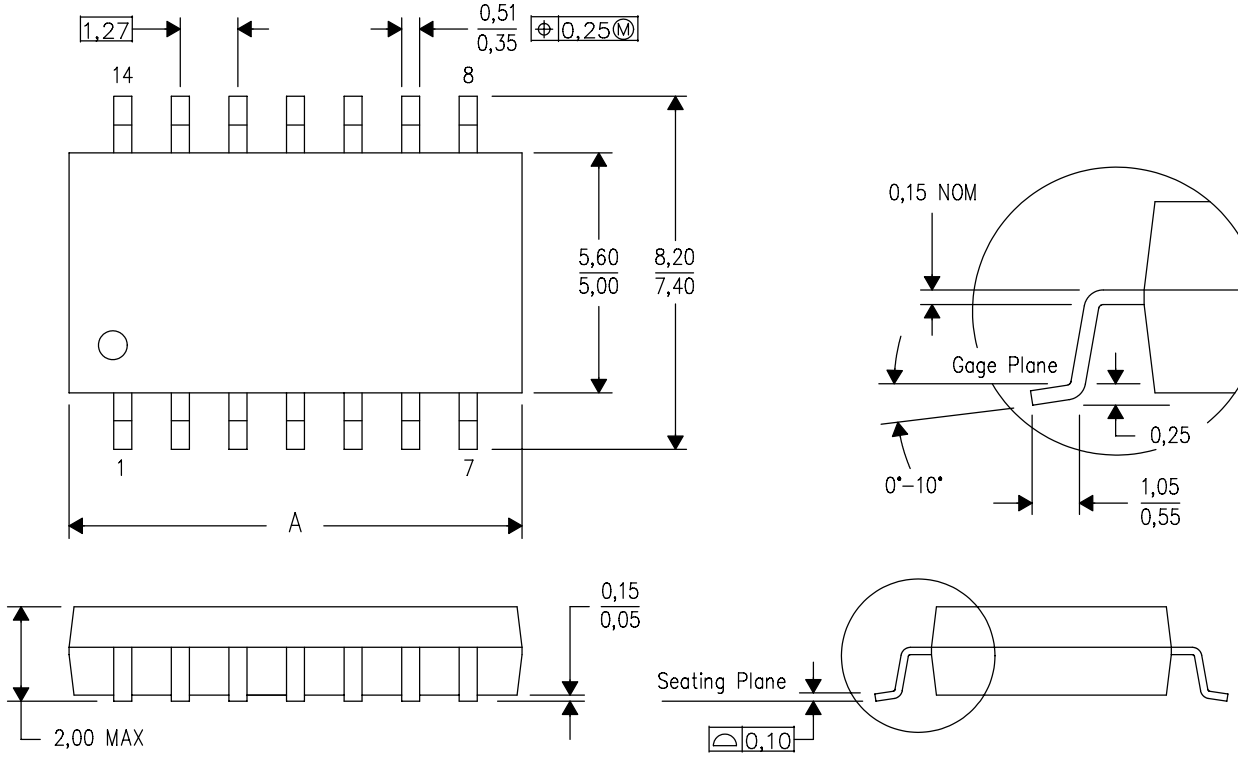
4040000/E 08/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

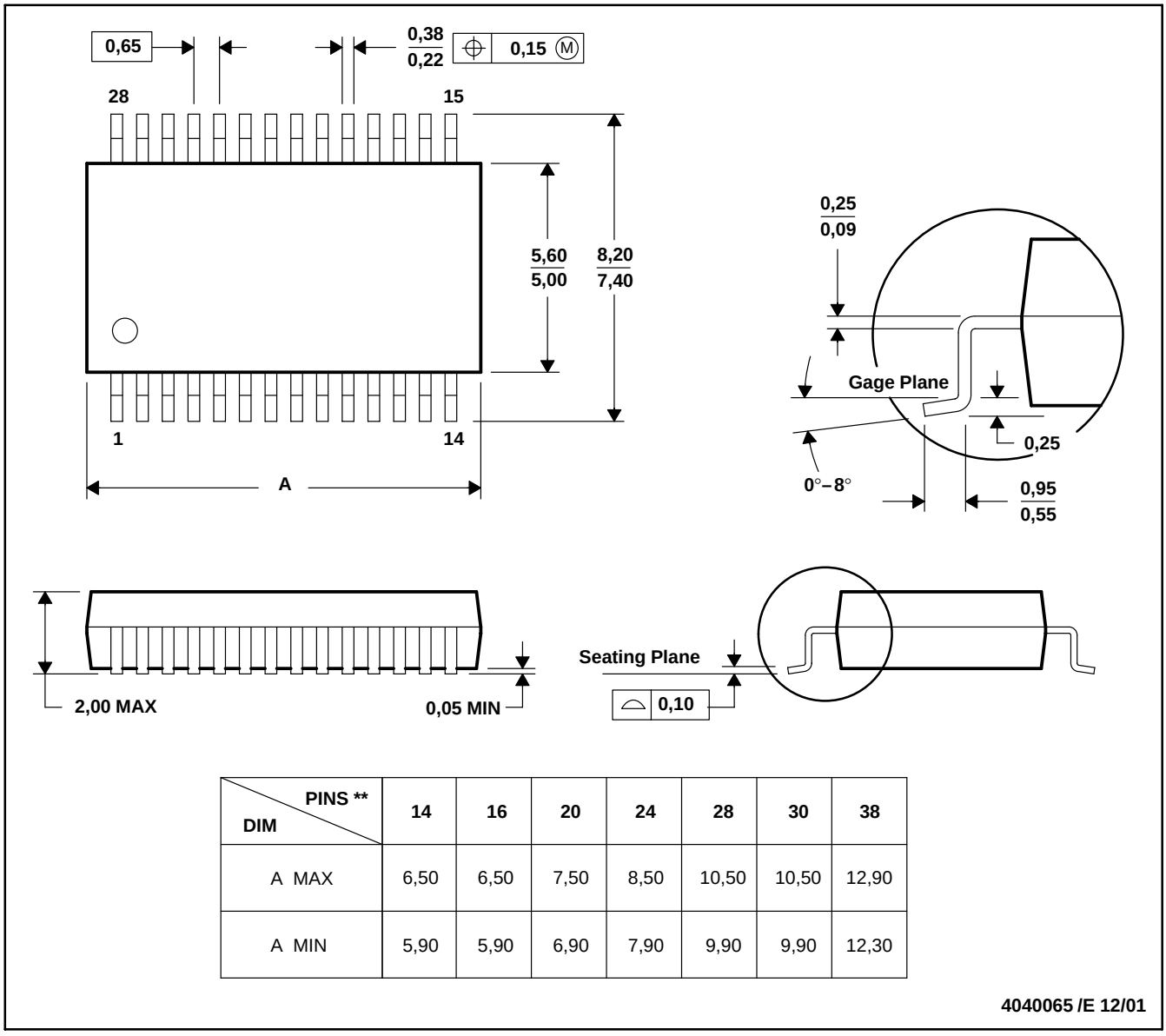
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



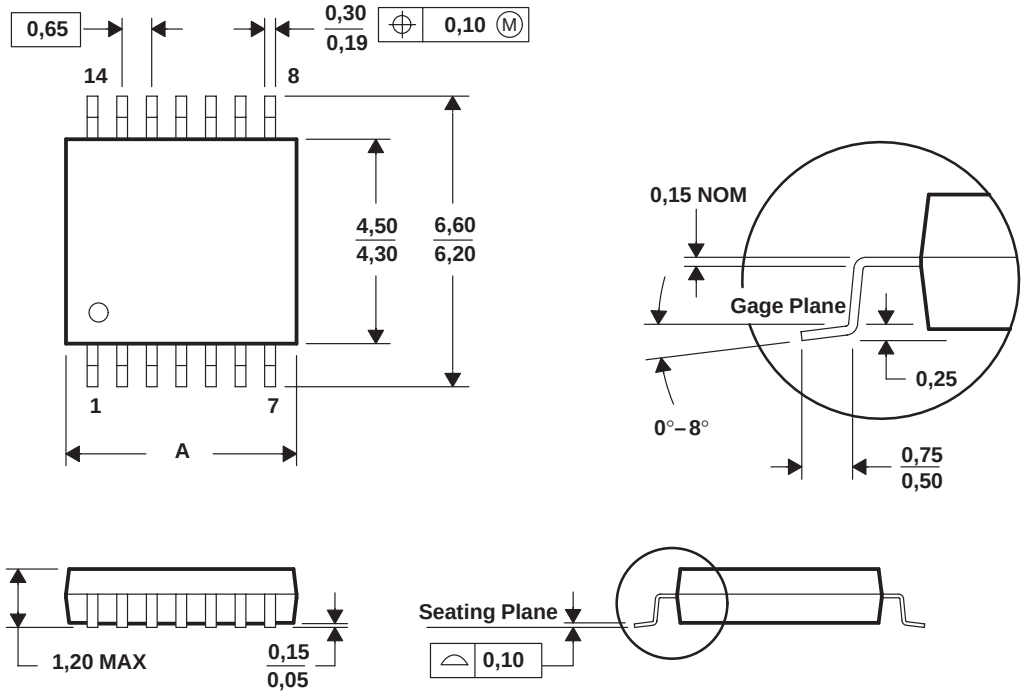
DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265