Preliminary Product Specification

Product Name	256K X 8 Bits Mask Programmable ROM		
KB Doc. No.	SF23C2000	KB Product. No.	SF23C2000

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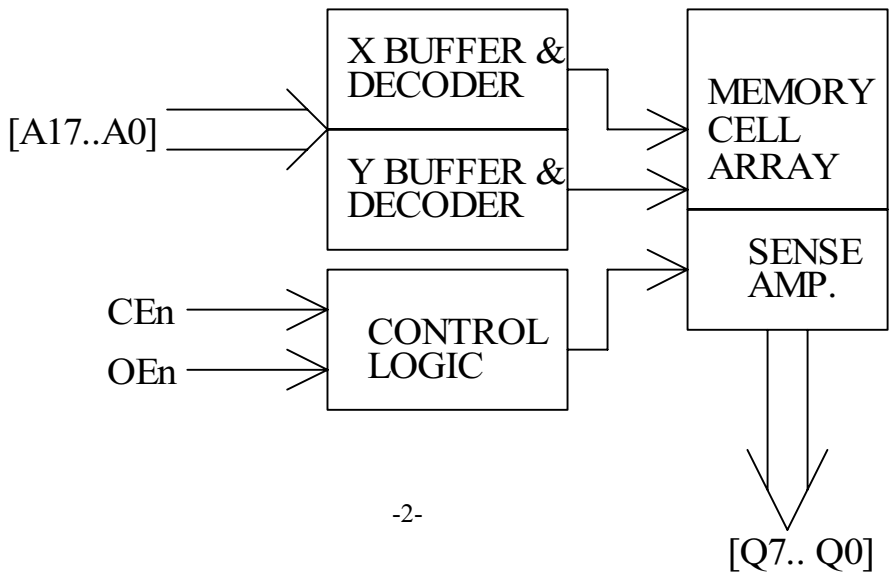
1 Function Description

The SF23C2000 is a fully static, 256K x 8 bit CMOS Mask Programmable ROM. This device operates in wide operating range. It requires no external clock for its operation and suitable for use with microprocessor program memory, and data memory (speech, graphic, etc).

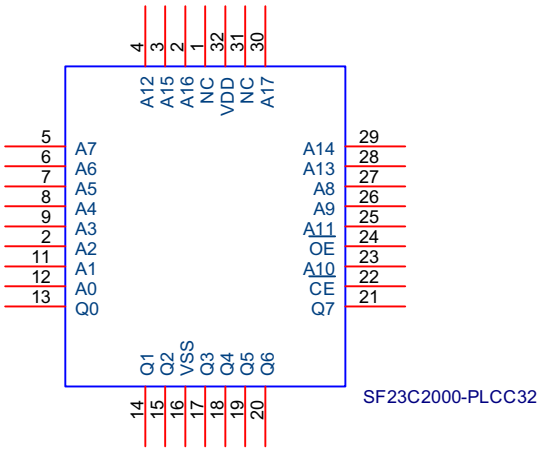
2 Features

- ✓ Voltage range: 2.4V ~ 5.5V
- ✓ Organization
  - Memory Cell Array: 256K x 8
- ✓ Low Operation Current (Typical)
  - 10μA Standby mode Current
  - 10mA Active Read Current
- ✓ Fully static operation
- ✓ Three state outputs
- ✓ Package bare chip, PLCC32

3 Functional block diagram

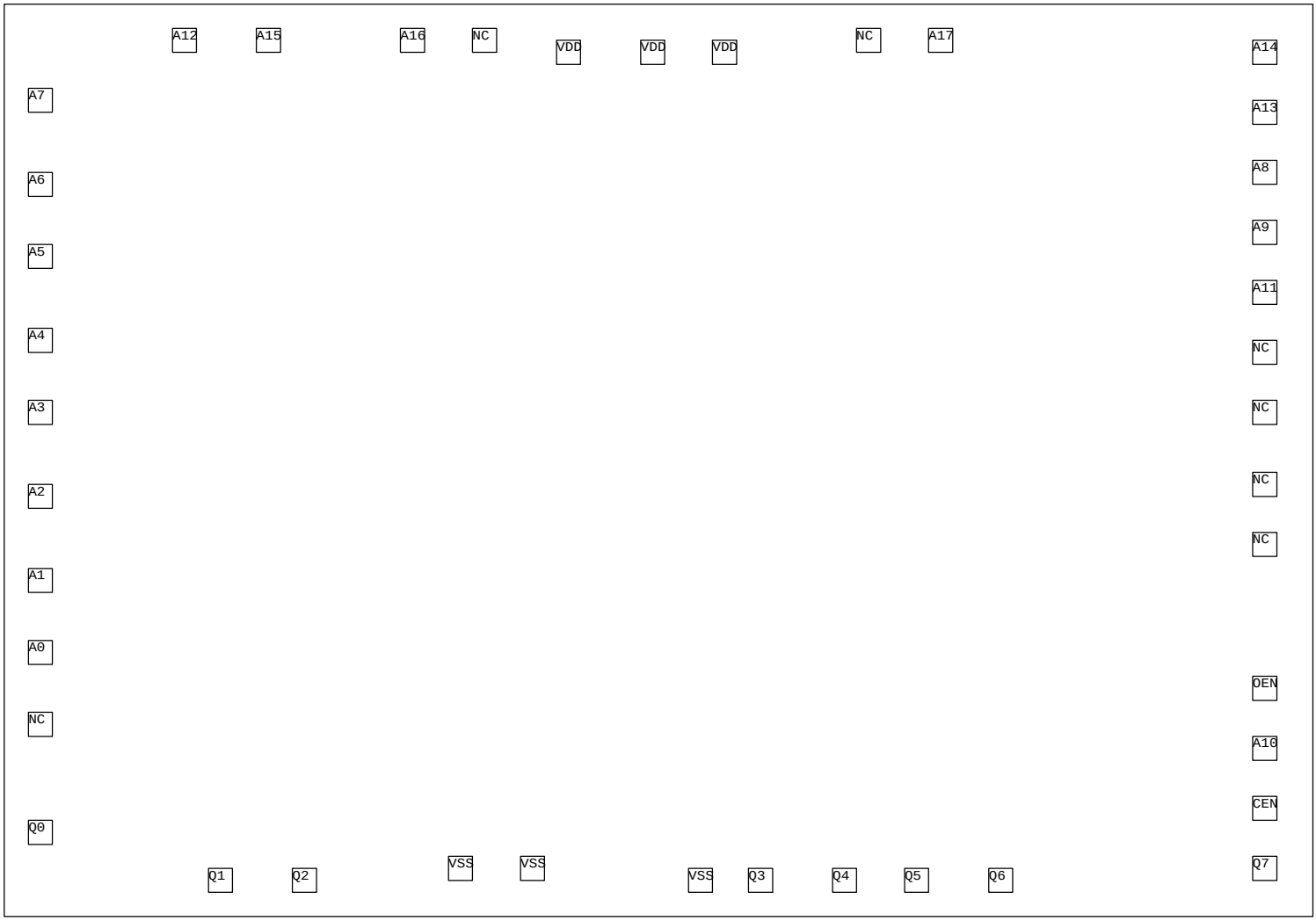


4 Pin Description



Symbol	Pin No.	I/O	Description
VDD	32	P	Positive power supply input pin.
VSS	16	P	Gound pin.
CEn	22	I	The CEn (Chip Enable) input is the device selection and power control for internal Mask ROM array. Whenever CEn goes high, the internal Mask ROM will enter standby (power saving) mode. Otherwise, it is in active mode and the contents of the ROM can be accessed.
OEn	24	I	OEn (Output Enable) is the output control which gates ROM array data onto the data output pins Q7 ~ Q0.
A17 ~ A0		I	Mask ROM Address input pins.
Q7 ~ Q0	21 ~ 17, 15 ~13	O	Mask ROM array Data outputs drive Q7 ~ Q0 pins during read operations (OEn low). The Q7 ~ Q0 pins stay in high-impedance when the chip is deselected (CEn high) or when the outputs are disabled (OEn high).

4.1 Pad Location



4.2 Pad Coordination

Pad Number	Pin Name	X Coordinate	Y Coordinate
1	A7	108.33	1931.75
2	A6	108.33	1744.31
3	A5	108.33	1557.03
4	A4	108.33	1369.59
5	A3	108.33	1182.31
6	A2	108.33	994.87
7	A1	108.33	807.59
8	A0	108.33	620.15
9	NC	108.33	432.98
10	Q0	108.33	171.72
11	Q1	525.97	101.14
12	Q2	713.13	101.14
13	VSS	1077.39	125.28
14	VSS	1267.83	125.48

15	VSS	1651.38	105.09
16	Q3	1814.02	106.14
17	Q4	2001.18	106.14
18	Q5	2188.62	106.14
19	Q6	2375.78	106.14
20	Q7	2975.87	103.39
21	CEN	2975.87	242.79
22	A10	2975.87	382.79
23	OEN	2975.87	522.79
24	NC	2978.86	875.14
25	NC	2978.86	1035.14
26	NC	2978.86	1195.14
NC	NC	2978.86	1355.14
28	A11	2978.87	1495.14
29	A9	2978.87	1635.14
30	A8	2978.87	1775.14
31	A13	2978.87	1915.14
32	A14	2978.87	2055.13
33	A17	2237.66	2066.92
34	NC	2050.22	2066.92
35	VDD	1708.76	2013.72
36	VDD	1534.34	2013.72
37	VDD	1359.92	2013.72
38	NC	1159.22	2052.30
39	A16	971.19	2052.30
40	A15	625.57	2052.30
41	A12	438.13	2052.30

5 Absolute Maximum Rating

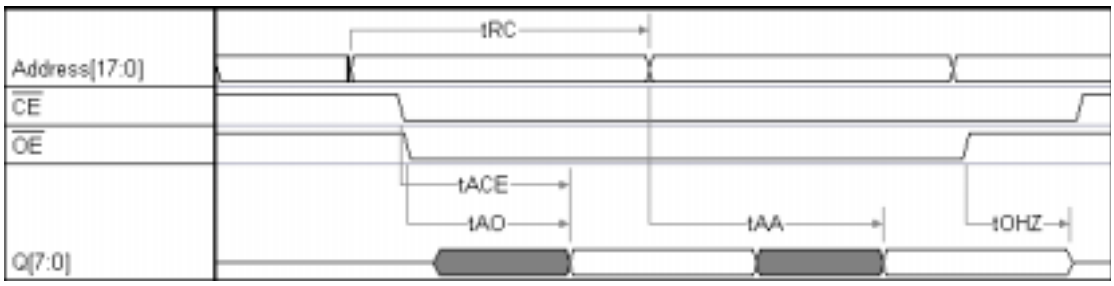
Items	Symbol	Rating	Condition
Supply Voltage	V_{DD}	-0.3 to 6 V	
Input Voltage	V_{IN}	-0.3 to Vdd+0.3 V	
Operating Temperature	T_{OPR}	-0 to 70 °C	
Storage Temperature	T_{STR}	-55 to 125 °C	

6 AC Electrical Characteristics

READ CYCLE

There are two ways of accessing the ROM data. The first one is to assert the valid address on the Address Bus, then assert CEn "low" to enable the ROM array. The access time in this mode is specified as t_{ACE}. The advantage of this access mode is that power consumption can be lowered. The second access mode keeps the CEn "low" while changes the addresses to access the contents of ROM data. The access time in this way is specified as t_{AA}. In this device, the Address Access Time decrease monotonically with increasing voltage, and it is shorter than Chip Enable Access Time when the Operation Voltage is higher then 4.5 V. Therefore in V_{op} higher than 4.5 Volts, it is more advisable to use the Address Access Mode to achieve faster access to ROM data when the power consumption is not a concern.

Item	Symbol	5.5V	5V	4.5V	3.6V	3.3V	3.0V	2.4V	Unit	Remark
Read Cycle Time	t_{RC}	290	220	170	180	190	220	290	ns	Min
Chip Enable Access Time	t_{ACE}	290	220	170	150	170	220	290	ns	Min
Address Access Time	t_{AA}	120	130	150	180	190	210	280	ns	Min



7 DC Electrical Characteristics

(V_{SS} = 0V, V_{DD} = 5.0 V, T_{OPR} = 25°C unless otherwise noted)

Parameter	Symbol	Min.	Typical	Max.	Unit	Condition
Supply Voltage	V_{DD}	2.4	-	5.5	V	
Operating Current	I_{DD}	-	10	-	mA	No load
Standby Current	I_{DD}	-	10	-	μA	No load
Input voltage	V_{IH} V_{IL}	2/3 0	- -	1 1/3	V_{DD}	V_{DD} = 4V ~ 6V

Input current leakage	I_{IL}	-	-	+/- 10	μA	
D Output High Voltage	V_{OH}	2.4	-	-	V	I_{OH} = 14 mA
D Output Low Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 3 mA