NSBA114EDXV6T1, NSBA114EDXV6T5

Preferred Devices

Dual Bias Resistor Transistors

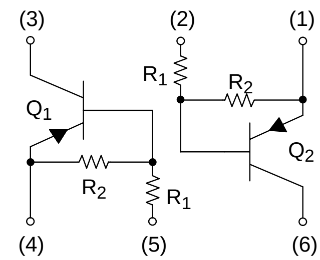
PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

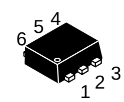
The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the NSBA114EDXV6T1 series, two BRT devices are housed in the SOT-563 package which is ideal for low-power surface mount applications where board space is at a premium.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch Tape and Reel
- Lead Free Solder Plating

ON Semiconductor®

http://onsemi.com





SOT-563
CASE 463A
PLASTIC

MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted, common for Q_1 and Q_2)

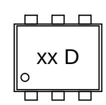
Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	- 50	Vdc
Collector-Emitter Voltage	V_{CEO}	-50	Vdc
Collector Current	I_C	-100	mAdc

THERMAL CHARACTERISTICS

Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	357 (Note 1) 2.9 (Note 1)	mW mW/°C
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	350 (Note 1)	°C/W
Characteristic (Both Junctions Heated)	**Symbol**	**Max**	**Unit**
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	500 (Note 1) 4.0 (Note 1)	mW mW/°C
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	250 (Note 1)	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to +150	°C

1. FR-4 @ Minimum Pad

MARKING DIAGRAM



xx = Specific Device Code (see table on page 2)
D = Date Code

ORDERING INFORMATION

Device	Package	Shipping
NSBA114EDXV6T1	SOT-563	4 mm pitch 4000/Tape & Reel
NSBA114EDXV6T5	SOT-563	2 mm pitch 8000/Tape & Reel

DEVICE MARKING INFORMATION

See specific marking information in the device marking table on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

DEVICE MARKING AND RESISTOR VALUES

Device	Package	Marking	R1 (kΩ)	R2 (kΩ)
NSBA114EDXV6T1 (Note 4)	SOT-563	0A	10	10
NSBA124EDXV6T1 (Note 4)	SOT-563	0B	22	22
NSBA144EDXV6T1 (Note 4)	SOT-563	0C	47	47
NSBA114YDXV6T1 (Note 4)	SOT-563	0D	10	47
NSBA114TDXV6T1 (Notes 2)	SOT-563	0E	10	∞
NSBA143TDXV6T1 (Notes 2, 4)	SOT-563	0F	4.7	∞
NSBA113EDXV6T1 (Notes 2, 4)	SOT-563	0G	1.0	1.0
NSBA123EDXV6T1 (Notes 2, 4)	SOT-563	0H	2.2	2.2
NSBA143EDXV6T1 (Notes 2, 4)	SOT-563	0J	4.7	4.7
NSBA143ZDXV6T1 (Notes 2, 4)	SOT-563	0K	4.7	47
NSBA124XDXV6T1 (Notes 2, 4)	SOT-563	0L	22	47
NSBA123JDXV6T1 (Notes 2)	SOT-563	0M	2.2	47
NSBA115EDXV6T1 (Notes 2, 4)	SOT-563	0N	100	100
NSBA114WDXV6T1 (Notes 2, 4)	SOT-563	0P	47	22

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, common for Q_1 and Q_2)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Base Cutoff Current (V_{CB} = -50 V, I_E = 0)		I_{CBO}	-	-	-100	nAdc
Collector-Emitter Cutoff Current (V_{CE} = -50 V, I_B = 0)		I_{CEO}	-	-	-500	nAdc
Emitter-Base Cutoff Current (V_{EB} = -6.0 V, I_C = 0)	NSBA114EDXV6T1	I_{EBO}	-	-	-0.5	mAdc
	NSBA124EDXV6T1		-	-	-0.2	
	NSBA144EDXV6T1		-	-	-0.1	
	NSBA114YDXV6T1		-	-	-0.2	
	NSBA114TDXV6T1		-	-	-0.9	
	NSBA143TDXV6T1		-	-	-1.9	
	NSBA113EDXV6T1		-	-	-4.3	
	NSBA123EDXV6T1		-	-	-2.3	
	NSBA143EDXV6T1		-	-	-1.5	
	NSBA143ZDXV6T1		-	-	-0.18	
	NSBA124XDXV6T1		-	-	-0.13	
	NSBA123JDXV6T1		-	-	-0.2	
	NSBA115EDXV6T1		-	-	-0.05	
	NSBA114WDXV6T1		-	-	-0.13	
Collector-Base Breakdown Voltage (I_C = -10 μA, I_E = 0)		$V_{(BR)CBO}$	-50	-	-	Vdc
Collector-Emitter Breakdown Voltage (Note 3) (I_C = -2.0 mA, I_B = 0)		$V_{(BR)CEO}$	-50	-	-	Vdc
ON CHARACTERISTICS (Note 3)						
Collector-Emitter Saturation Voltage (I_C = -10 mA, I_E = -0.3 mA) (I_C = -10 mA, I_B = -5 mA) (I_C = -10 mA, I_B = -1 mA)	 NSBA113EDXV6T1/NSBA123EDXV6T1 NSBA114TDXV6T1/NSBA143TDXV6T1 NSBA143EDXV6T1/NSBA143ZDXV6T1/NSBA124XDXV6T1	$V_{CE(sat)}$	-	-	-0.25	Vdc

2. New resistor combinations. Updated curves to follow in subsequent data sheets.
3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%
4. Available upon request.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, common for Q_1 and Q_2) (continued)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (Note 3) (continued)						
DC Current Gain	NSBA114EDXV6T1	h_{FE}	35	60	-	
(V_{CE} = -10 V, I_C = -5.0 mA)	NSBA124EDXV6T1		60	100	-	
	NSBA144EDXV6T1		80	140	-	
	NSBA114YDXV6T1		80	140	-	
	NSBA114TDXV6T1		160	250	-	
	NSBA143TDXV6T1		160	250	-	
	NSBA113EDXV6T1		3.0	5.0	-	
	NSBA123EDXV6T1		8.0	15	-	
	NSBA143EDXV6T1		15	27	-	
	NSBA143ZDXV6T1		80	140	-	
	NSBA124XDXV6T1		80	130	-	
	NSBA123JDXV6T1		80	140	-	
	NSBA115EDXV6T1		80	130	-	
	NSBA114WDXV6T1		80	140	-	
Output Voltage (on)		V_{OL}				Vdc
(V_{CC} = -5.0 V, V_B = -2.5 V, R_L = 1.0 kΩ)	NSBA114EDXV6T1		-	-	-0.2	
	NSBA124EDXV6T1		-	-	-0.2	
	NSBA114YDXV6T1		-	-	-0.2	
	NSBA114TDXV6T1		-	-	-0.2	
	NSBA143TDXV6T1		-	-	-0.2	
	NSBA113EDXV6T1		-	-	-0.2	
	NSBA123EDXV6T1		-	-	-0.2	
	NSBA143EDXV6T1		-	-	-0.2	
	NSBA143ZDXV6T1		-	-	-0.2	
	NSBA124XDXV6T1		-	-	-0.2	
	NSBA123JDXV6T1		-	-	-0.2	
(V_{CC} = -5.0 V, V_B = -3.5 V, R_L = 1.0 kΩ)	NSBA144EDXV6T1		-	-	-0.2	
(V_{CC} = -5.0 V, V_B = -5.5 V, R_L = 1.0 kΩ)	NSBA115EDXV6T1		-	-	-0.2	
(V_{CC} = -5.0 V, V_B = -4.0 V, R_L = 1.0 kΩ)	NSBA114WDXV6T1		-	-	-0.2	
Output Voltage (off) (V_{CC} = -5.0 V, V_B = -0.5 V, R_L = 1.0 kΩ)		V_{OH}	-4.9	-	-	Vdc
(V_{CC} = -5.0 V, V_B = -0.05 V, R_L = 1.0 kΩ)	NSBA113EDXV6T1					
(V_{CC} = -5.0 V, V_B = -0.25 V, R_L = 1.0 kΩ)	NSBA114TDXV6T1					
	NSBA143TDXV6T1					
	NSBA123EDXV6T1					
	NSBA143ZDXV6T1					
Input Resistor	NSBA114EDXV6T1	R_1	7.0	10	13	k Ω
	NSBA124EDXV6T1		15.4	22	28.6	
	NSBA144EDXV6T1		32.9	47	61.1	
	NSBA114YDXV6T1		7.0	10	13	
	NSBA114TDXV6T1		7.0	10	13	
	NSBA143TDXV6T1		3.3	4.7	6.1	
	NSBA113EDXV6T1		0.7	1.0	1.3	
	NSBA123EDXV6T1		1.5	2.2	2.9	
	NSBA143EDXV6T1		3.3	4.7	6.1	
	NSBA143ZDXV6T1		3.3	4.7	6.1	
	NSBA124XDXV6T1		15.4	22	28.6	
	NSBA123JDXV6T1		1.54	2.2	2.86	
	NSBA115EDXV6T1		70	100	130	
	NSBA114WDXV6T1		32.9	47	61.1	
Resistor Ratio	NSBA114EDXV6T1/NSBA124EDXV6T1/ NSBA144EDXV6T1/NSBA115EDXV6T1	R_1/R_2	0.8	1.0	1.2	
	NSBA114YDXV6T1		0.17	0.21	0.25	
	NSBA114TDXV6T1/NSBA143TDXV6T1		-	-	-	
	NSBA113EDXV6T1/NSBA123EDXV6T1/NSBA143EDXV6T1		0.8	1.0	1.2	
	NSBA143ZDXV6T1		0.055	0.1	0.185	
	NSBA124XDXV6T1		0.38	0.47	0.56	
	NSBA123JDXV6T1		0.038	0.047	0.056	
	NSBA114WDXV6T1		1.7	2.1	2.6	

2. New resistor combinations. Updated curves to follow in subsequent data sheets.
3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%
4. Available upon request.

ALL NSBA114EDXV6T1 SERIES DEVICES

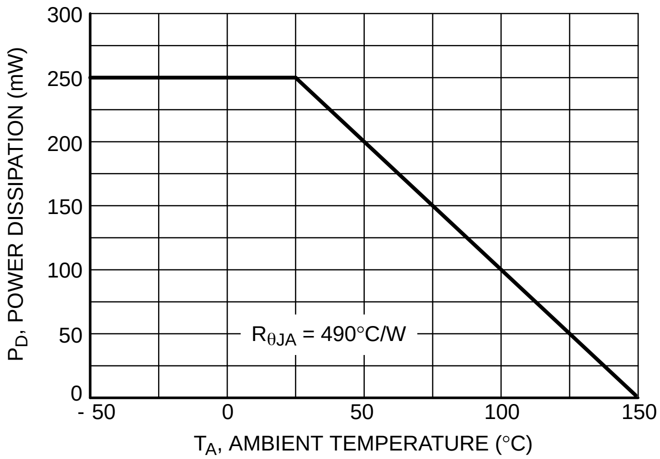


Figure 1. Derating Curve - ALL DEVICES

TYPICAL ELECTRICAL CHARACTERISTICS — NSBA114EDXV6T1

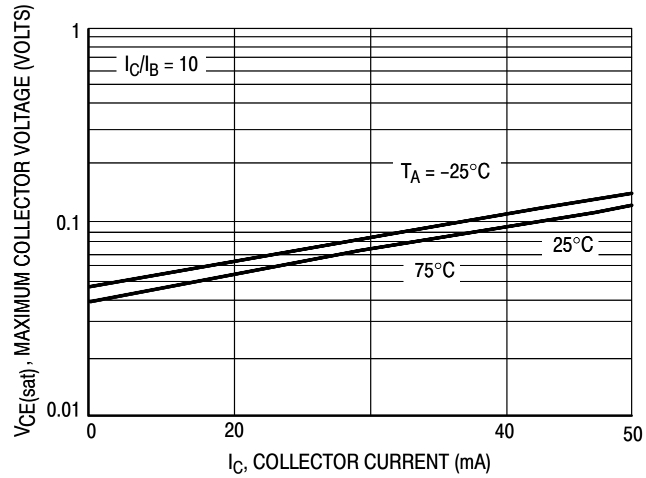


Figure 2. $V_{CE(sat)}$ versus I_C

TYPICAL ELECTRICAL CHARACTERISTICS — NSBA114EDXV6T1

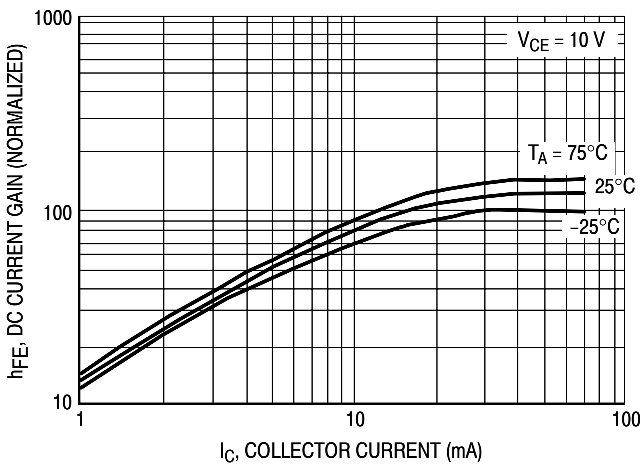


Figure 3. DC Current Gain

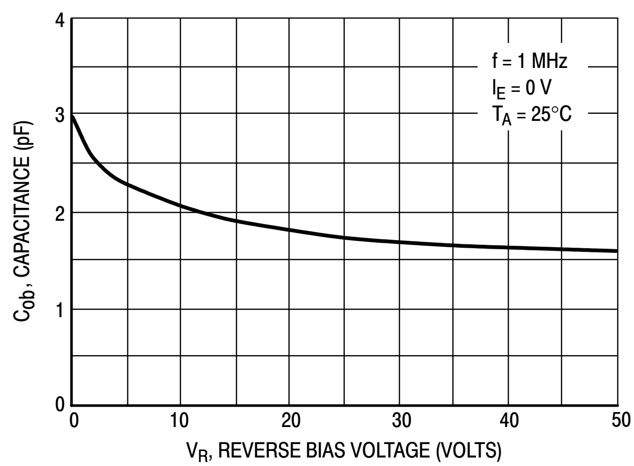


Figure 4. Output Capacitance

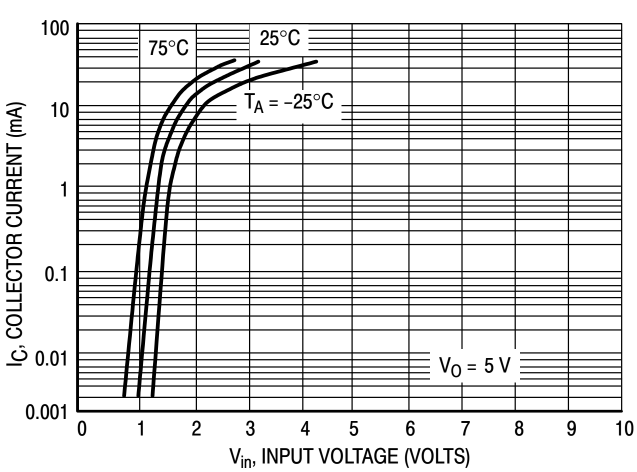


Figure 5. Output Current versus Input Voltage

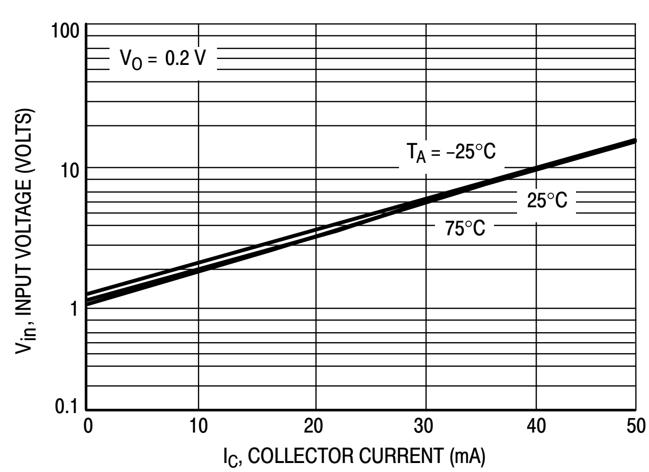


Figure 6. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS — NSBA124EDXV6T1

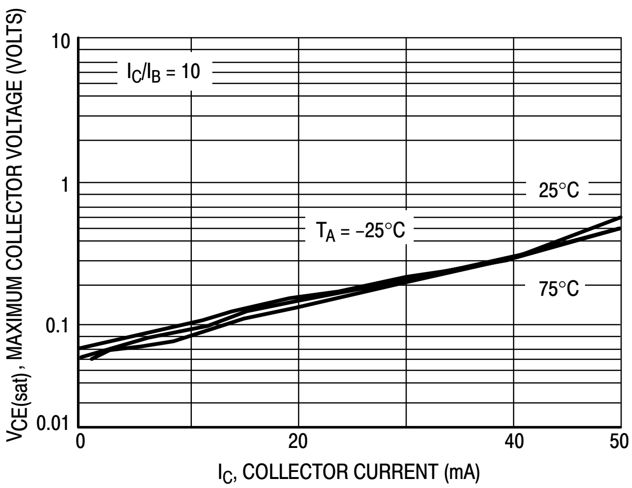


Figure 7. $V_{CE(sat)}$ versus I_C

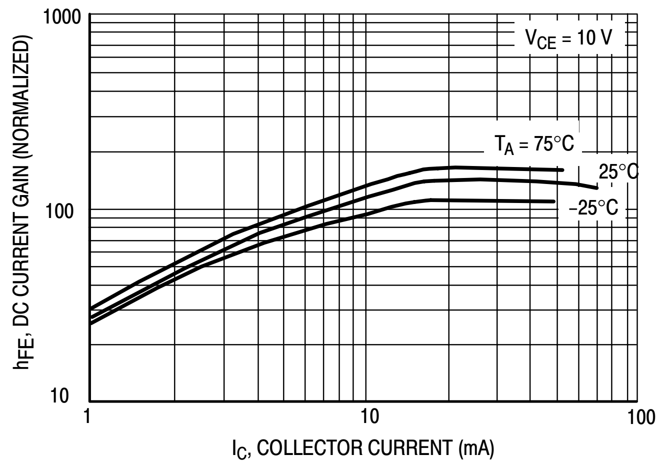


Figure 8. DC Current Gain

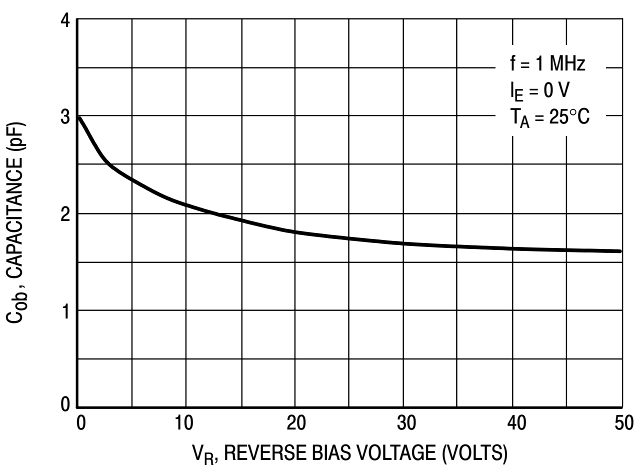


Figure 9. Output Capacitance

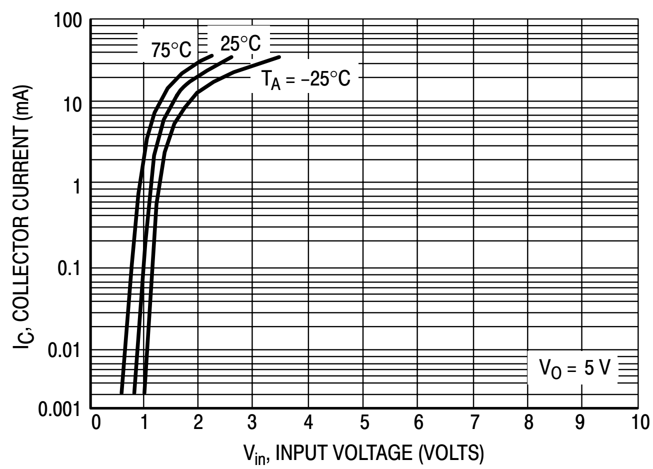


Figure 10. Output Current versus Input Voltage

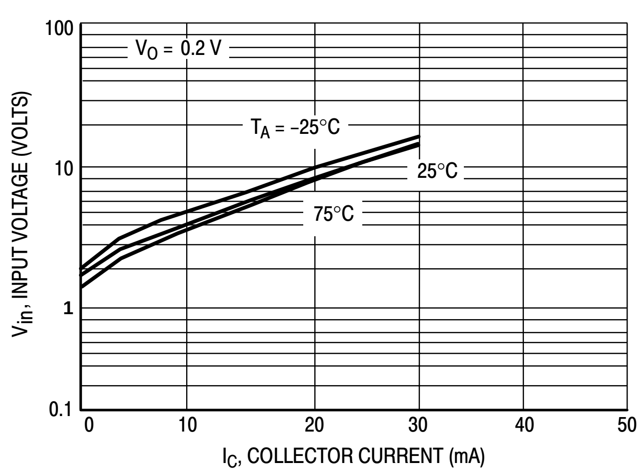


Figure 11. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS — NSBA144EDXV6T1

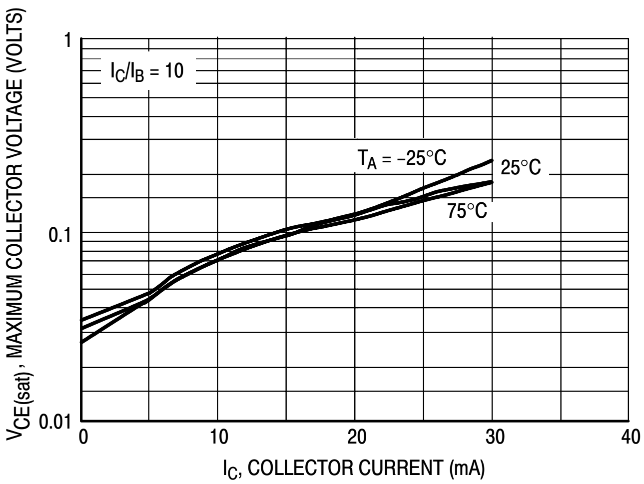


Figure 12. $V_{CE(sat)}$ versus I_C

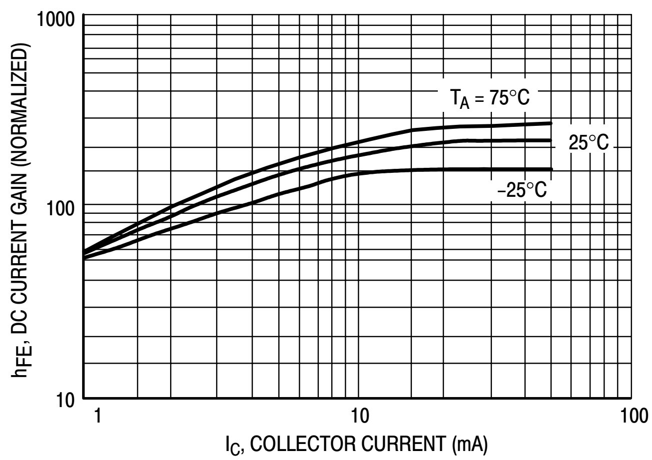


Figure 13. DC Current Gain

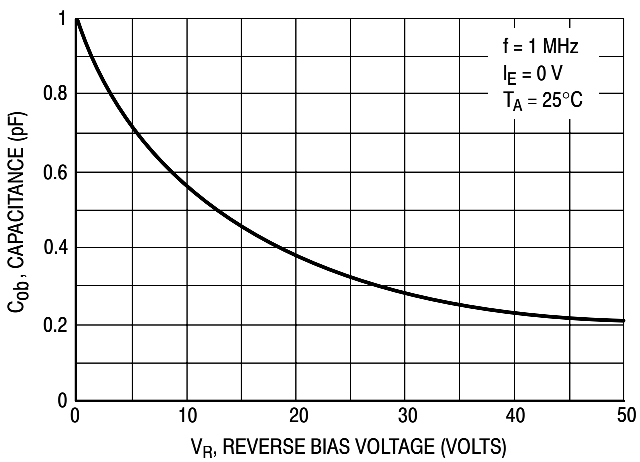


Figure 14. Output Capacitance

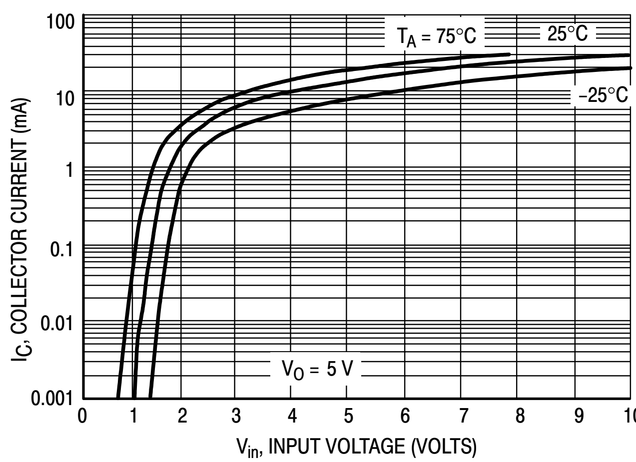


Figure 15. Output Current versus Input Voltage

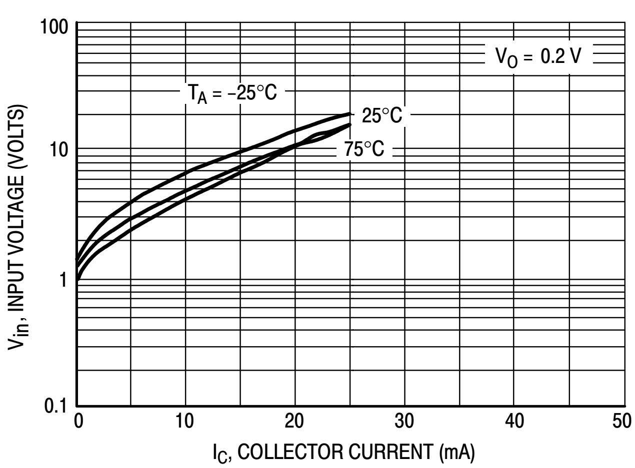


Figure 16. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS — NSBA114YDXV6T1

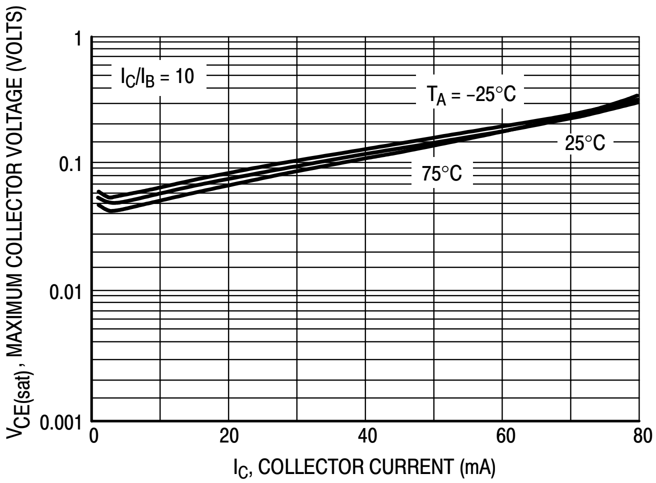


Figure 17. $V_{CE(sat)}$ versus I_C

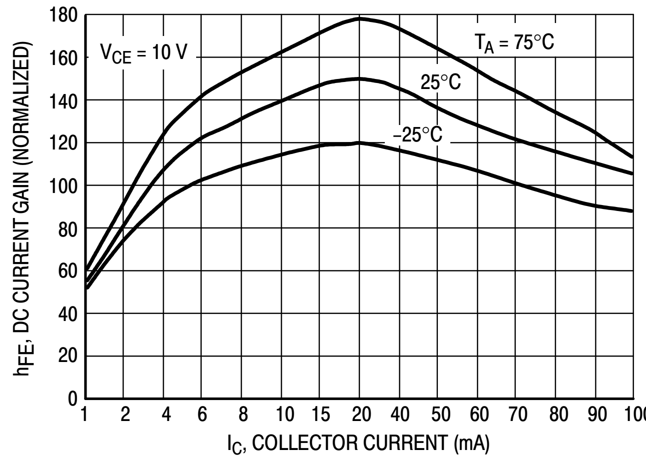


Figure 18. DC Current Gain

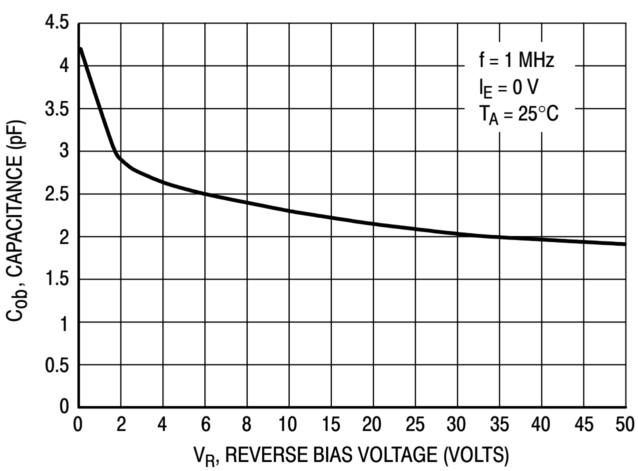


Figure 19. Output Capacitance

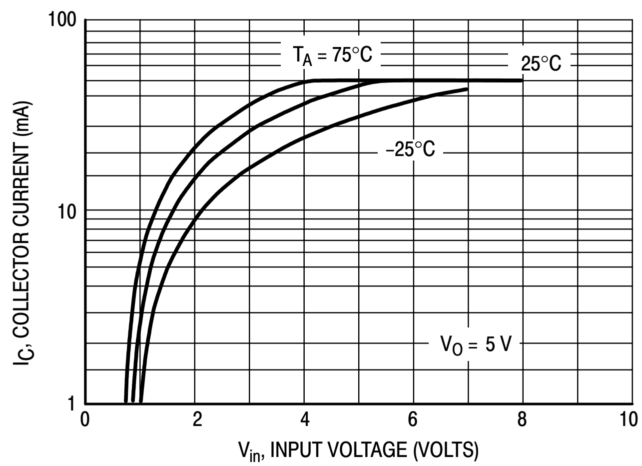


Figure 20. Output Current versus Input Voltage

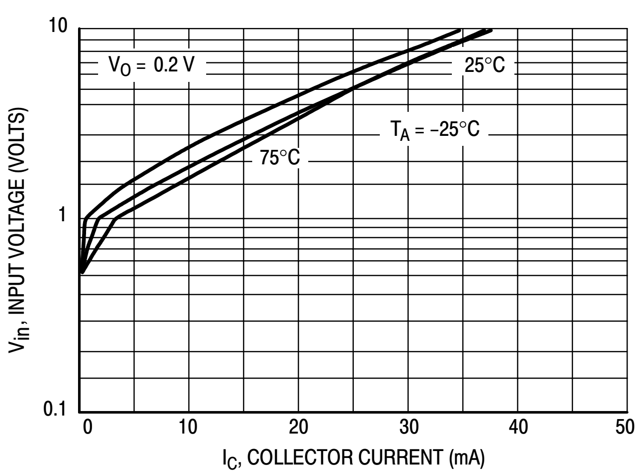


Figure 21. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS — NSBA114TDXV6T1

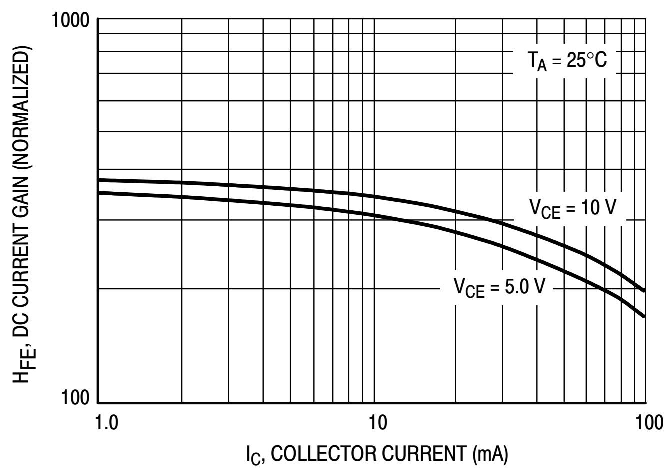


Figure 22. DC Current Gain

TYPICAL ELECTRICAL CHARACTERISTICS — NSBA143TDXV6T1

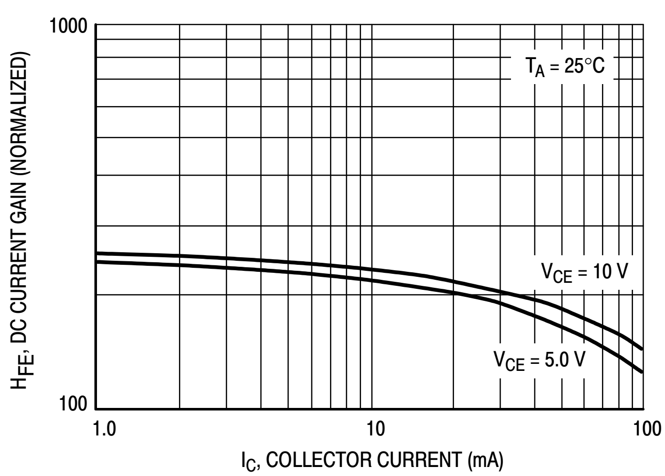


Figure 23. DC Current Gain

TYPICAL ELECTRICAL CHARACTERISTICS — NSBA115EDXV6T1

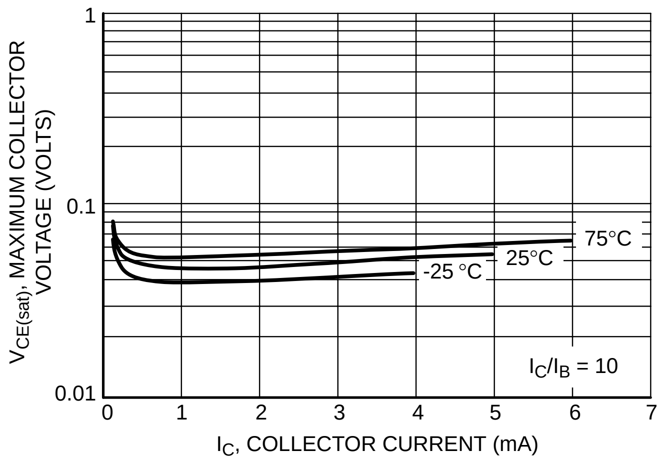


Figure 24. Maximum Collector Voltage versus Collector Current

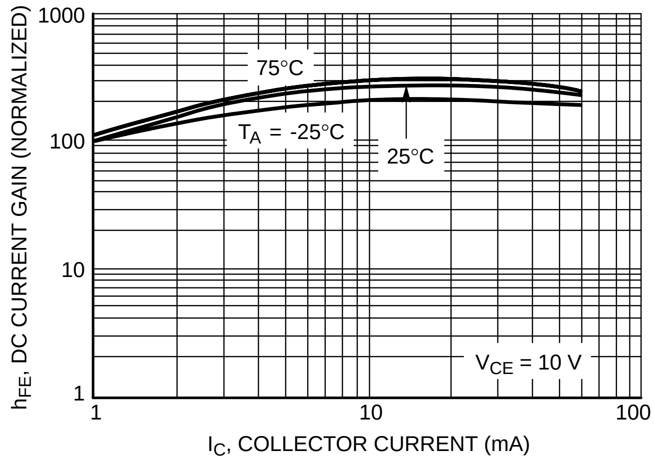


Figure 25. DC Current Gain

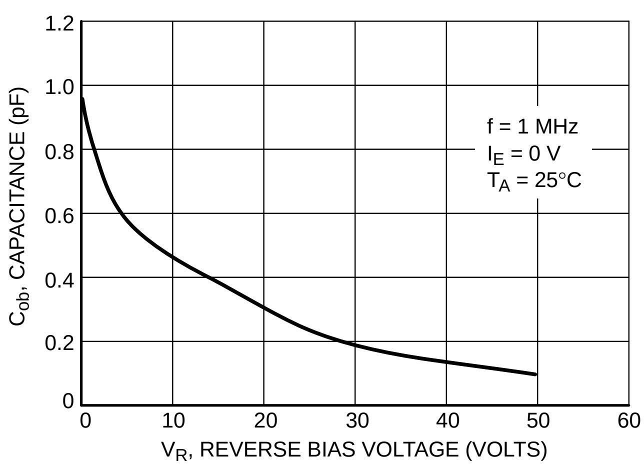


Figure 26. Output Capacitance

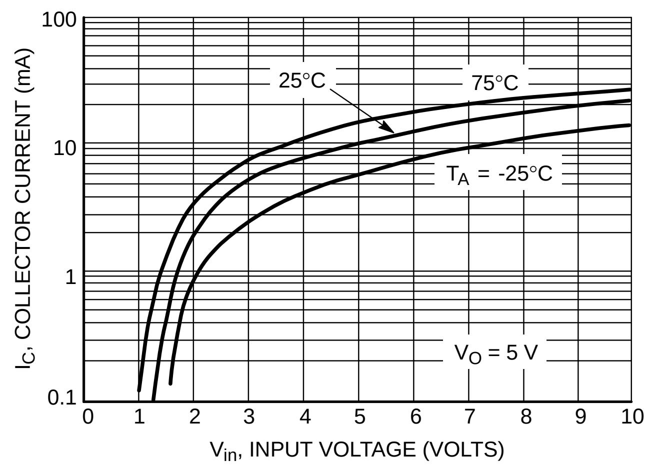


Figure 27. Output Current versus Input Voltage

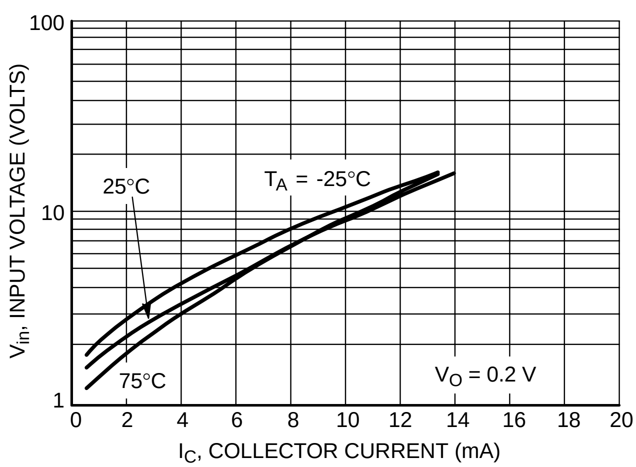


Figure 28. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS — NSBA114WDXV6T1

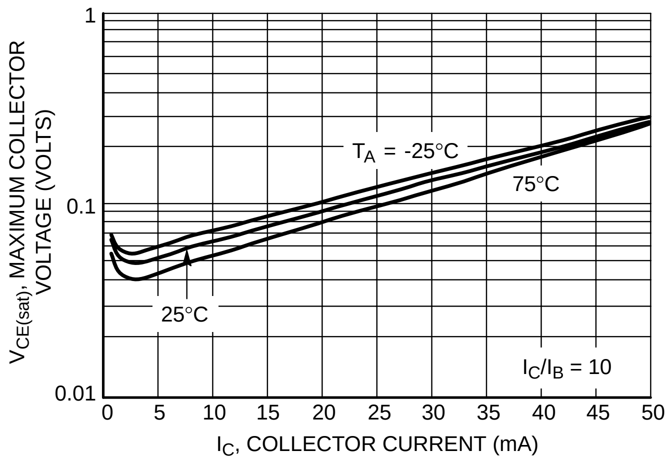


Figure 29. Maximum Collector Voltage versus Collector Current

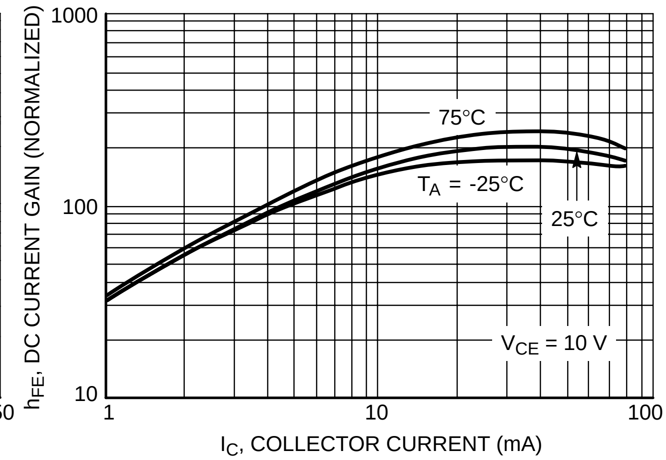


Figure 30. DC Current Gain

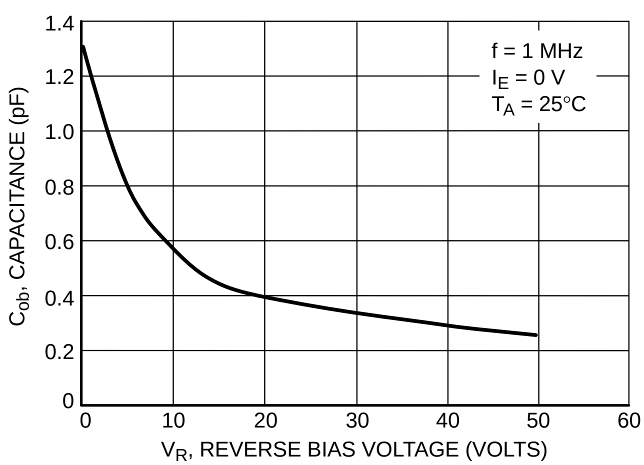


Figure 31. Output Capacitance

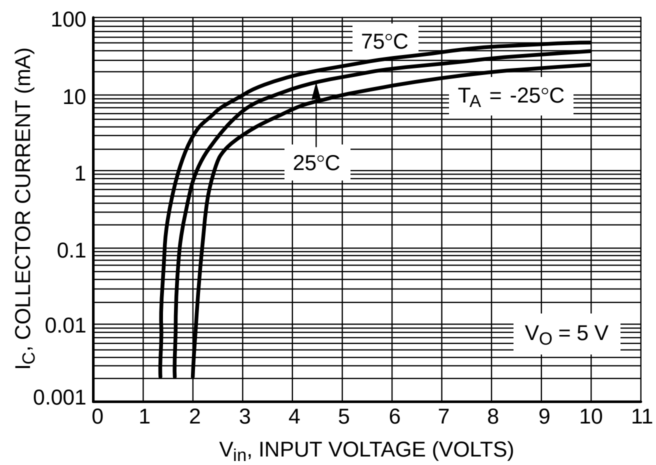


Figure 32. Output Current versus Input Voltage

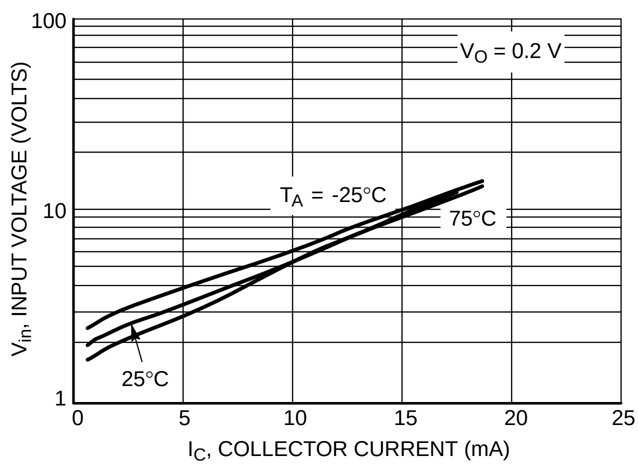
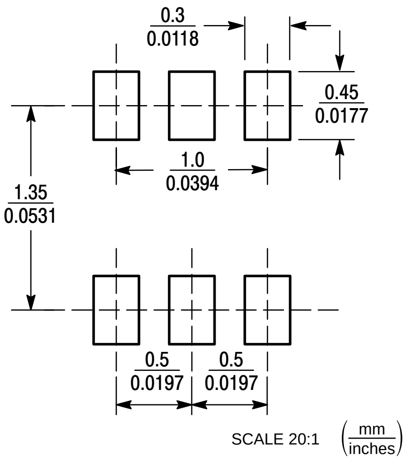


Figure 33. Input Voltage versus Output Current

INFORMATION FOR USING THE SOT-563 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT-563

SOT-563 POWER DISSIPATION

The power dissipation of the SOT-563 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT-563 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 150 milliwatts.

$$P_D = \frac{150°C - 25°C}{833°C/W} = 150 \text{ milliwatts}$$

The 833°C/W for the SOT-563 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 150 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT-563 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad®. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

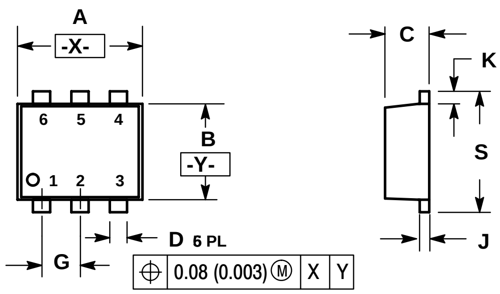
The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS

SOT-563, 6 LEAD
CASE 463A-01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.50	1.70	0.059	0.067
B	1.10	1.30	0.043	0.051
C	0.50	0.60	0.020	0.024
D	0.17	0.27	0.007	0.011
G	0.50 BSC		0.020 BSC	
J	0.08	0.18	0.003	0.007
K	0.10	0.30	0.004	0.012
S	1.50	1.70	0.059	0.067

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

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