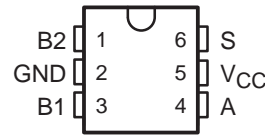


# SN74LVC1G3157 SINGLE-POLE, DOUBLE-THROW ANALOG SWITCH

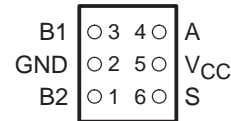
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- 1.65-V to 5.5-V  $V_{CC}$  Operation
- Useful for Both Analog and Digital Applications
- Specified Break-Before-Make Switching
- Rail-to-Rail Signal Handling
- High Degree of Linearity
- High Speed, Typically 0.5 ns ( $V_{CC} = 3\text{ V}$ ,  $C_L = 50\text{ pF}$ )
- Low On-State Resistance, Typically  $\approx 6\ \Omega$  ( $V_{CC} = 4.5\text{ V}$ )
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DBV OR DCK PACKAGE  
(TOP VIEW)



YEP OR YZP PACKAGE  
(BOTTOM VIEW)



## description/ordering information

This single-pole, double-throw (SPDT) analog switch is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC1G3157 can handle both analog and digital signals. The device permits signals with amplitudes of up to  $V_{CC}$  (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Tape and reel	SN74LVC1G3157YEPR	---C5_
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74LVC1G3157YZPR	
	SOT (SOT-23) – DBV	Tape and reel	SN74LVC1G3157DBVR	CC5_
	SOT (SC-70) – DCK	Tape and reel	SN74LVC1G3157DCKR	C5_

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.

YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# SN74LVC1G3157

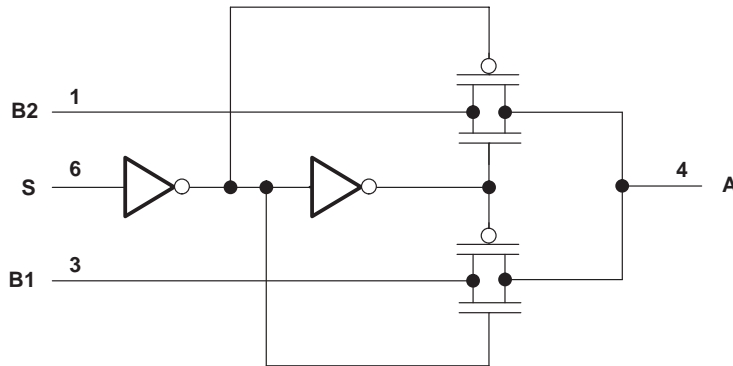
## SINGLE-POLE, DOUBLE-THROW ANALOG SWITCH

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FUNCTION TABLE

CONTROL INPUT S	ON CHANNEL
L	B1
H	B2

### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ (see Note 1)	-0.5 V to 6.5 V
Control input voltage range, $V_{IN}$ (see Notes 1 and 2)	-0.5 V to 6.5 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, 3, and 4)	-0.5 V to $V_{CC} + 0.5$ V
Control input clamp current, $I_{IK}$ ( $V_{IN} < 0$ )	-50 mA
I/O port diode current, $I_{I/O}$ ( $V_{I/O} < 0$ or $V_{I/O} > V_{CC}$ )	$\pm 50$ mA
On-state switch current, $I_{I/O}$ ( $V_{I/O} = 0$ to $V_{CC}$ ) (see Note 5)	$\pm 128$ mA
Continuous current through $V_{CC}$ or GND	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 6):	
DBV package	165°C/W
DCK package	259°C/W
YEP/YZP package	123°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- All voltages are with respect to ground unless otherwise specified.
  - The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  - This value is limited to 5.5 V maximum.
  - $V_I$ ,  $V_O$ ,  $V_A$ , and  $V_{Bn}$  are used to denote specific conditions for  $V_{I/O}$ .
  - $I_I$ ,  $I_O$ ,  $I_A$ , and  $I_{Bn}$  are used to denote specific conditions for  $I_{I/O}$ .
  - The package thermal impedance is calculated in accordance with JESD 51-7.

# SN74LVC1G3157

## SINGLE-POLE, DOUBLE-THROW ANALOG SWITCH

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### recommended operating conditions (see Note 7)

		MIN	MAX	UNIT
V <sub>CC</sub>		1.65	5.5	V
V <sub>I/O</sub>		0	V <sub>CC</sub>	V
V <sub>IN</sub>		0	5.5	V
V <sub>IH</sub>	High-level input voltage, control input	V <sub>CC</sub> = 1.65 V to 1.95 V	V <sub>CC</sub> × 0.75	V
		V <sub>CC</sub> = 2.3 V to 5.5 V	V <sub>CC</sub> × 0.7	
V <sub>IL</sub>	Low-level input voltage, control input	V <sub>CC</sub> = 1.65 V to 1.95 V	V <sub>CC</sub> × 0.25	V
		V <sub>CC</sub> = 2.3 V to 5.5 V	V <sub>CC</sub> × 0.3	
Δt/Δv	Input transition rise/fall time	V <sub>CC</sub> = 1.65 V to 1.95 V	20	ns/V
		V <sub>CC</sub> = 2.3 V to 2.7 V	20	
		V <sub>CC</sub> = 3 V to 3.6 V	10	
		V <sub>CC</sub> = 4.5 V to 5.5 V	10	
T <sub>A</sub>		-40	85	°C

NOTE 7: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74LVC1G3157

## SINGLE-POLE, DOUBLE-THROW ANALOG SWITCH

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
r <sub>on</sub>	On-state switch resistance‡	See Figures 1 and 2	V <sub>I</sub> = 0 V	I <sub>O</sub> = 4 mA	1.65 V	11	20	Ω
			V <sub>I</sub> = 1.65 V	I <sub>O</sub> = -4 mA		15	50	
			V <sub>I</sub> = 0 V	I <sub>O</sub> = 8 mA	2.3 V	8	12	
			V <sub>I</sub> = 2.3 V	I <sub>O</sub> = -8 mA		11	30	
			V <sub>I</sub> = 0 V	I <sub>O</sub> = 24 mA	3 V	7	9	
			V <sub>I</sub> = 3 V	I <sub>O</sub> = -24 mA		9	20	
			V <sub>I</sub> = 0 V	I <sub>O</sub> = 30 mA	4.5 V	6	7	
			V <sub>I</sub> = 2.4 V	I <sub>O</sub> = -30 mA		7	12	
V <sub>I</sub> = 4.5 V	I <sub>O</sub> = -30 mA		7	15				
r <sub>range</sub>	On-state switch resistance over signal range‡§	0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub> (see Figures 1 and 2)	I <sub>A</sub> = -4 mA	1.65 V			140	Ω
			I <sub>A</sub> = -8 mA	2.3 V			45	
			I <sub>A</sub> = -24 mA	3 V			18	
			I <sub>A</sub> = -30 mA	4.5 V			10	
Δr <sub>on</sub>	Difference of on-state resistance between switches†¶#	See Figure 1	V <sub>Bn</sub> = 1.15 V	I <sub>A</sub> = -4 mA	1.65 V		0.5	Ω
			V <sub>Bn</sub> = 1.6 V	I <sub>A</sub> = -8 mA	2.3 V		0.1	
			V <sub>Bn</sub> = 2.1 V	I <sub>A</sub> = -24 mA	3 V		0.1	
			V <sub>Bn</sub> = 3.15 V	I <sub>A</sub> = -30 mA	4.5 V		0.1	
r <sub>on(flat)</sub>	ON resistance flatness†¶	0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	I <sub>A</sub> = -4 mA	1.65 V			110	Ω
			I <sub>A</sub> = -8 mA	2.3 V			26	
			I <sub>A</sub> = -24 mA	3 V			9	
			I <sub>A</sub> = -30 mA	4.5 V			4	
I <sub>off</sub> *†	Off-state switch leakage current	0 ≤ V <sub>I</sub> , V <sub>O</sub> ≤ V <sub>CC</sub> . (see Figure 3)		1.65 V to 5.5 V			±1 ±0.05	μA
I <sub>S(on)</sub>	On-state switch leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>O</sub> = Open (see Figure 4)		5.5 V			±1 ±0.1†	μA
I <sub>IN</sub>	Control input current	0 ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>		0 V to 5.5 V			±1 ±0.05	μA
I <sub>CC</sub>	Supply current	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5 V		1	10	μA
ΔI <sub>CC</sub>	Supply-current change	V <sub>IN</sub> = V <sub>CC</sub> - 0.6 V		5.5 V			500	μA
C <sub>in</sub>	Control input capacitance	S		5 V		2.7		pF
C <sub>io(off)</sub>	Switch input/output capacitance	Bn		5 V		5.2		pF
C <sub>io(on)</sub>	Switch input/output capacitance	Bn		5 V		17.3		pF
		A			17.3			

† T<sub>A</sub> = 25°C

‡ Measured by the voltage drop between I/O pins at the indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A or B) ports.

§ Specified by design

¶ Δr<sub>on</sub> = r<sub>on(max)</sub> - r<sub>on(min)</sub> measured at identical V<sub>CC</sub>, temperature, and voltage levels.

# This parameter is characterized, but not tested in production.

|| Flatness is defined as the difference between the maximum and minimum values of ON resistance over the specified range of conditions.

\* I<sub>off</sub> is the same as I<sub>S(off)</sub> (off-state switch leakage current).



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## SINGLE-POLE, DOUBLE-THROW ANALOG SWITCH

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### analog switch characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V <sub>CC</sub>	TYP	UNIT
Frequency response (switch on) <sup>†</sup>	A or Bn	Bn or A	R <sub>L</sub> = 50 Ω, f <sub>in</sub> = sine wave (see Figure 6)	1.65 V	300	MHz
				2.3 V	300	
				3 V	300	
				4.5 V	300	
Crosstalk (between switches) <sup>‡</sup>	B1 or B2	B2 or B1	R <sub>L</sub> = 50 Ω, f <sub>in</sub> = 10 MHz (sine wave) (see Figure 7)	1.65 V	-54	dB
				2.3 V	-54	
				3 V	-54	
				4.5 V	-54	
Feed-through attenuation (switch off) <sup>‡</sup>	A or Bn	Bn or A	C <sub>L</sub> = 5 pF, R <sub>L</sub> = 50 Ω, f <sub>in</sub> = 10 MHz (sine wave) (see Figure 8)	1.65 V	-57	dB
				2.3 V	-57	
				3 V	-57	
				4.5 V	-57	
Charge injection <sup>§</sup>	S	A	C <sub>L</sub> = 0.1 nF, R <sub>L</sub> = 1 MΩ, (see Figure 9)	3.3 V	3	pC
				5 V	7	
Total harmonic distortion	A or Bn	Bn or A	V <sub>I</sub> = 0.5 V p-p, R <sub>L</sub> = 600 Ω, f <sub>in</sub> = 600 Hz to 20 kHz (sine wave) (see Figure 10)	1.65 V	0.1	%
				2.3 V	0.025	
				3 V	0.015	
				4.5 V	0.01	

<sup>†</sup> Adjust f<sub>in</sub> voltage to obtain 0 dBm at output. Increase f<sub>in</sub> frequency until dB meter reads -3 dB.

<sup>‡</sup> Adjust f<sub>in</sub> voltage to obtain 0 dBm at input.

<sup>§</sup> Specified by design

### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 5 and 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub> <sup>¶</sup>	A or Bn	Bn or A	2		1.2		0.8		0.3		ns
t <sub>en</sub> <sup>#</sup>	S	Bn	7	24	3.5	14	2.5	7.6	1.7	5.7	ns
t <sub>dis</sub> <sup>  </sup>			3	13	2	7.5	1.5	5.3	0.8	3.8	
t <sub>B-M</sub> <sup>*</sup>			0.5		0.5		0.5		0.5		ns

<sup>¶</sup> t<sub>pd</sub> is the slower of t<sub>PLH</sub> or t<sub>PHL</sub>. The propagation delay is calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

<sup>#</sup> t<sub>en</sub> is the slower of t<sub>PZL</sub> or t<sub>PZH</sub>.

<sup>||</sup> t<sub>dis</sub> is the slower of t<sub>PLZ</sub> or t<sub>PHZ</sub>.

<sup>\*</sup> Specified by design

# SN74LVC1G3157 SINGLE-POLE, DOUBLE-THROW ANALOG SWITCH

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## PARAMETER MEASUREMENT INFORMATION

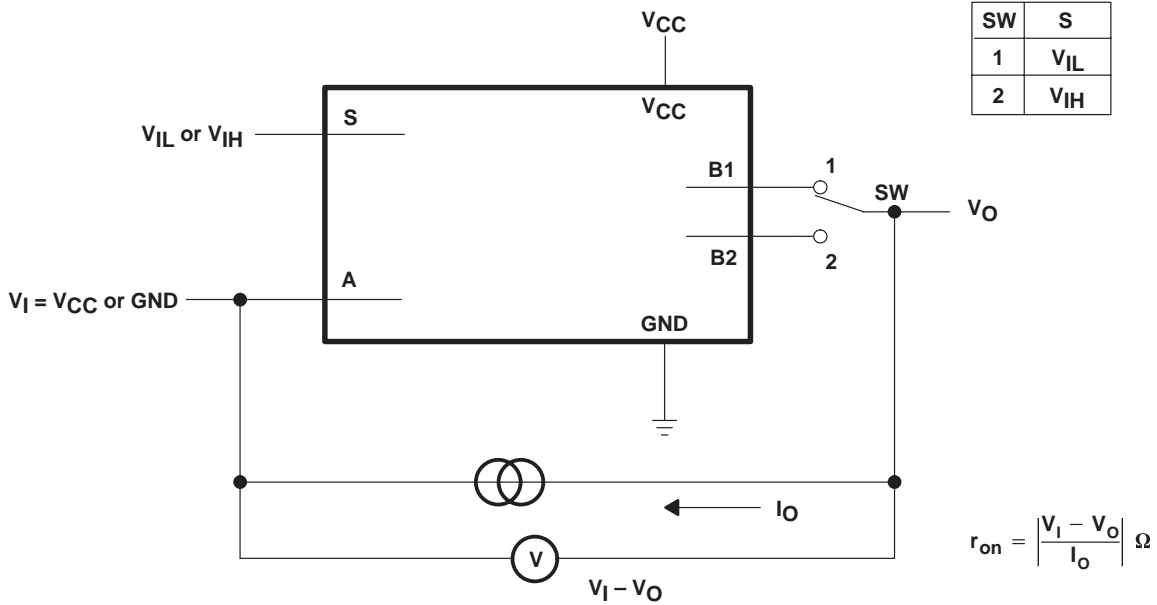


Figure 1. On-State Resistance Test Circuit

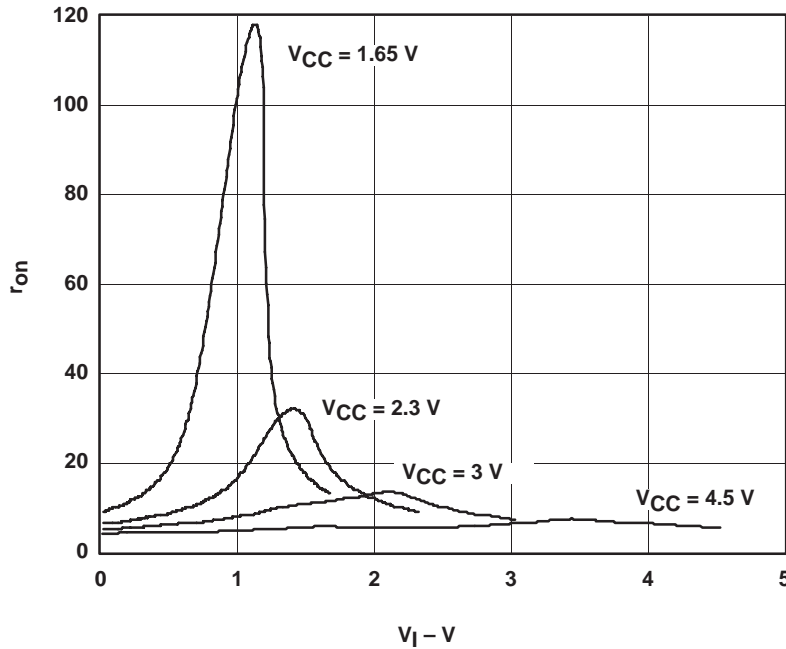


Figure 2. Typical  $r_{on}$  as a Function of Input Voltage ( $V_I$ ) for  $V_I = 0$  to  $V_{CC}$

PARAMETER MEASUREMENT INFORMATION

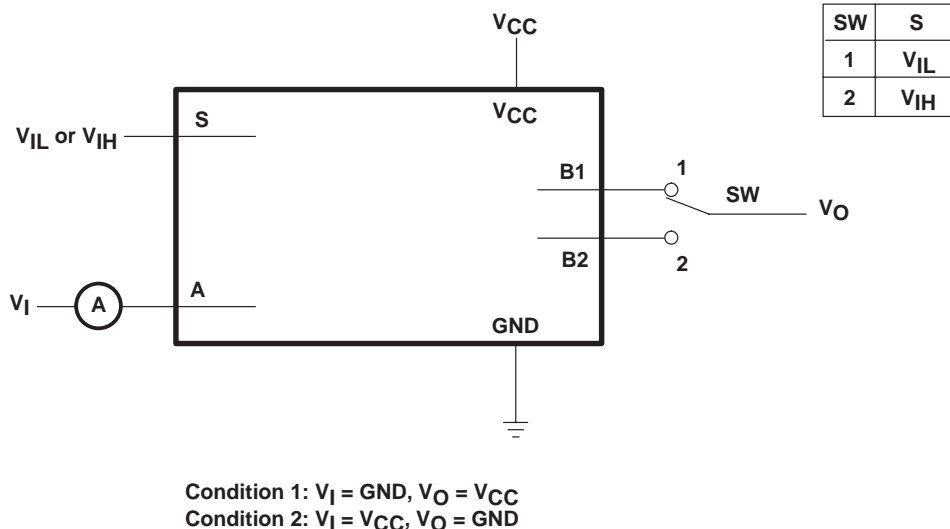


Figure 3. Off-State Switch Leakage-Current Test Circuit

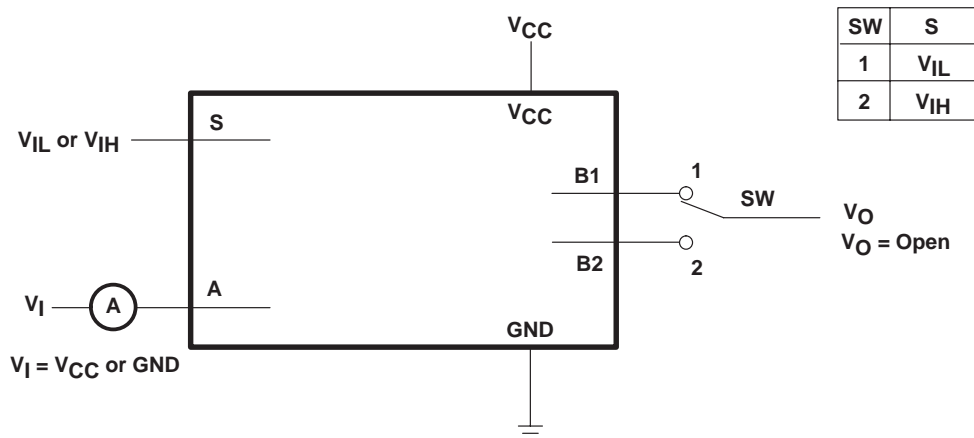


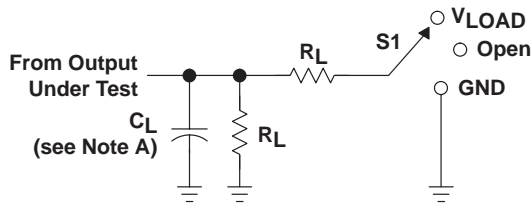
Figure 4. On-State Switch Leakage-Current Test Circuit

# SN74LVC1G3157

## SINGLE-POLE, DOUBLE-THROW ANALOG SWITCH

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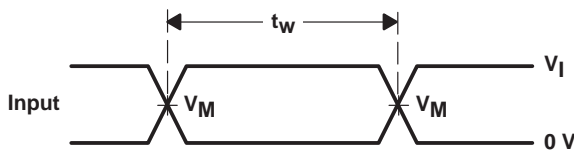
### PARAMETER MEASUREMENT INFORMATION



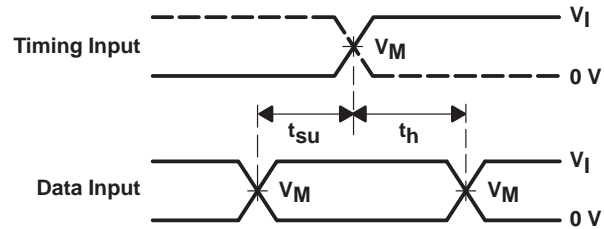
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

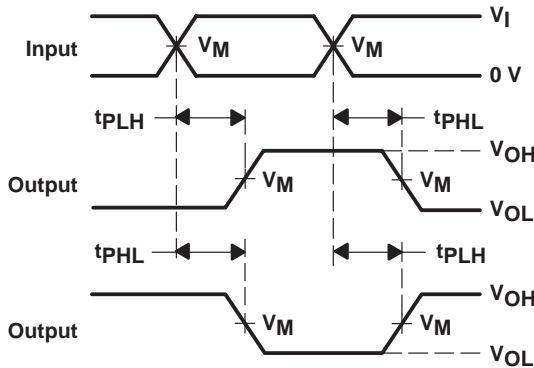
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V



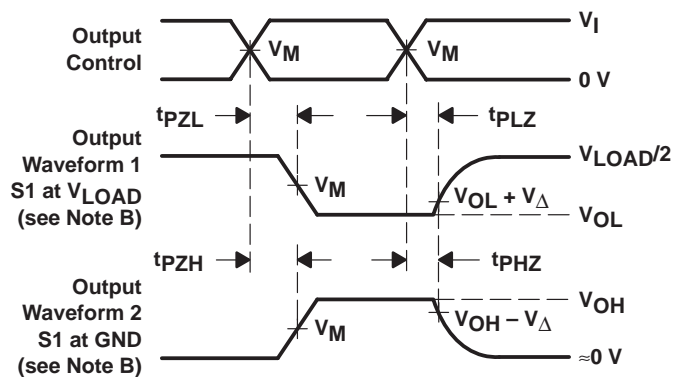
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

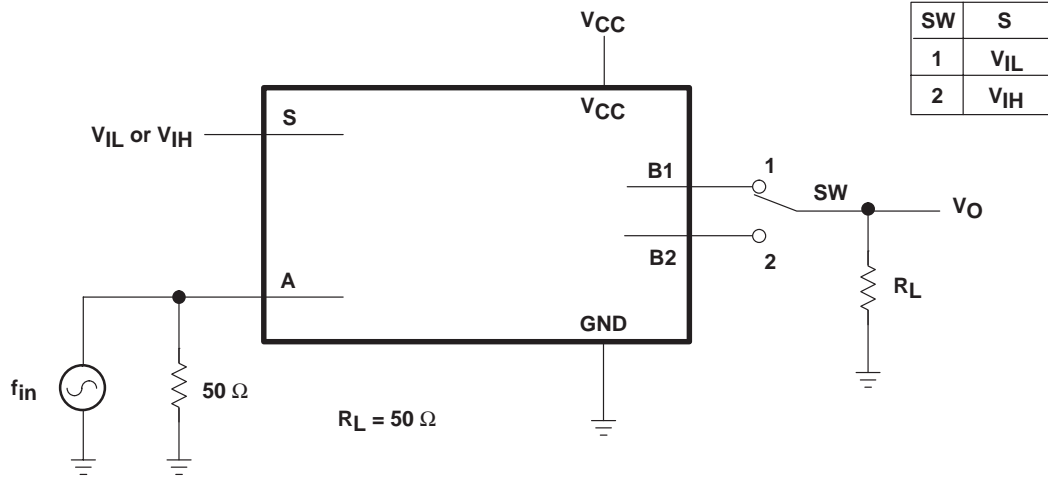
Figure 5. Load Circuit and Voltage Waveforms



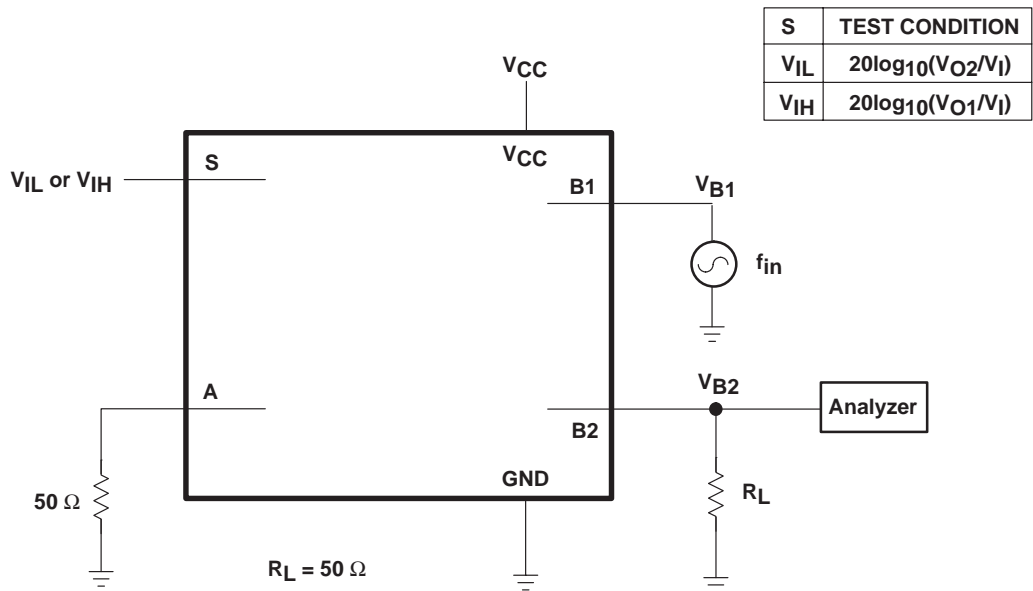
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**PARAMETER MEASUREMENT INFORMATION**



**Figure 6. Frequency Response (Switch On)**



**Figure 7. Crosstalk (Between Switches)**

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## PARAMETER MEASUREMENT INFORMATION

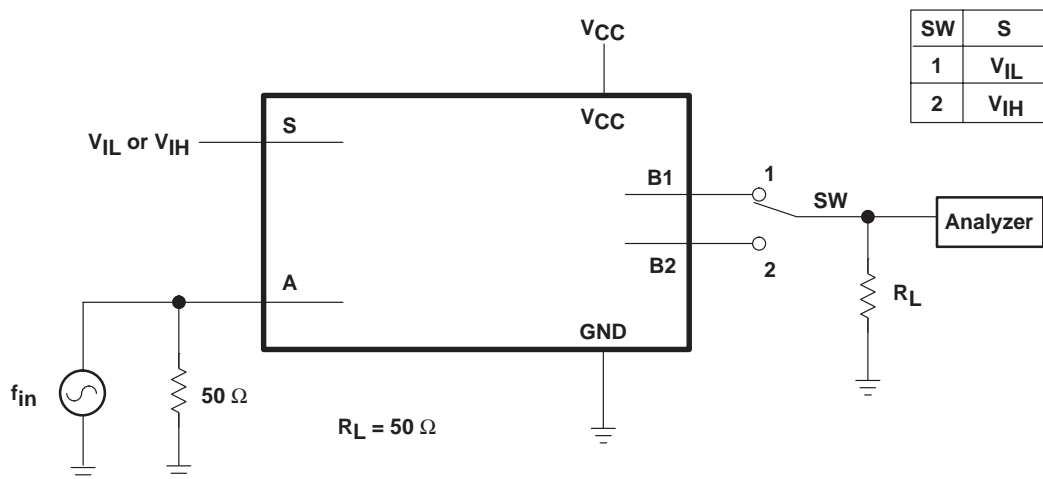


Figure 8. Feed Through

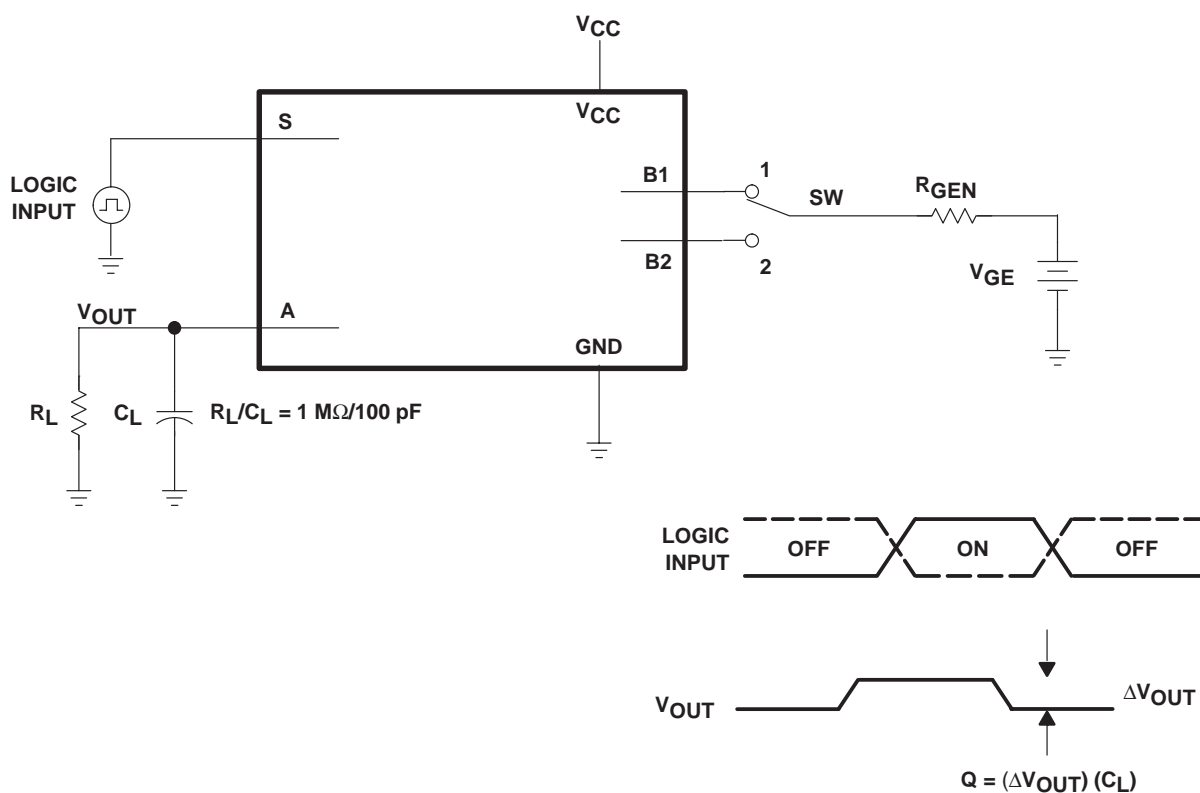


Figure 9. Charge-Injection Test

PARAMETER MEASUREMENT INFORMATION

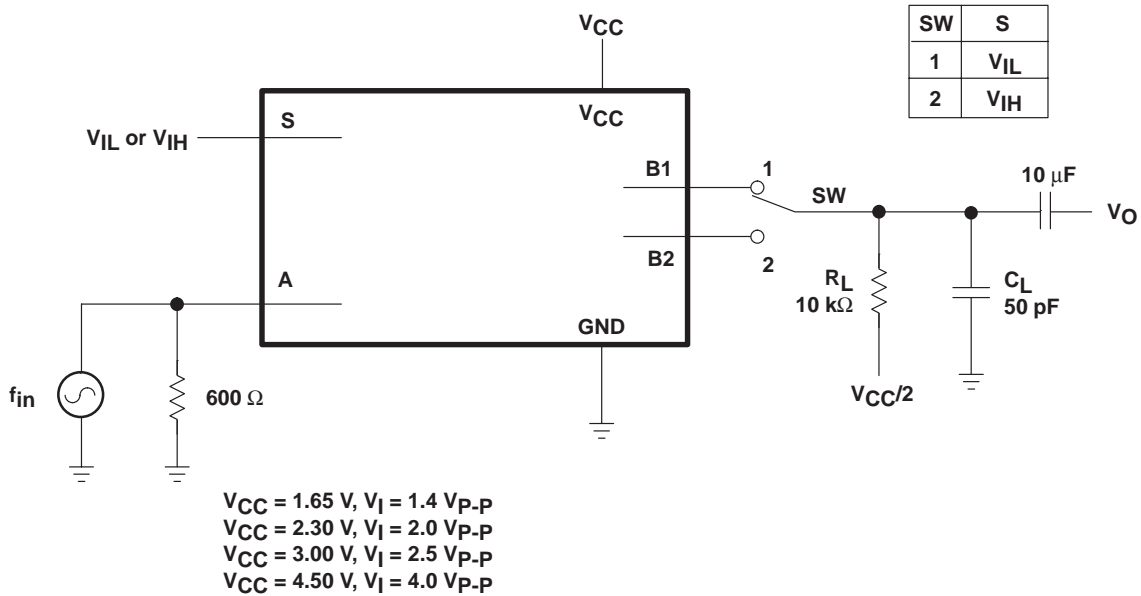


Figure 10. Total Harmonic Distortion

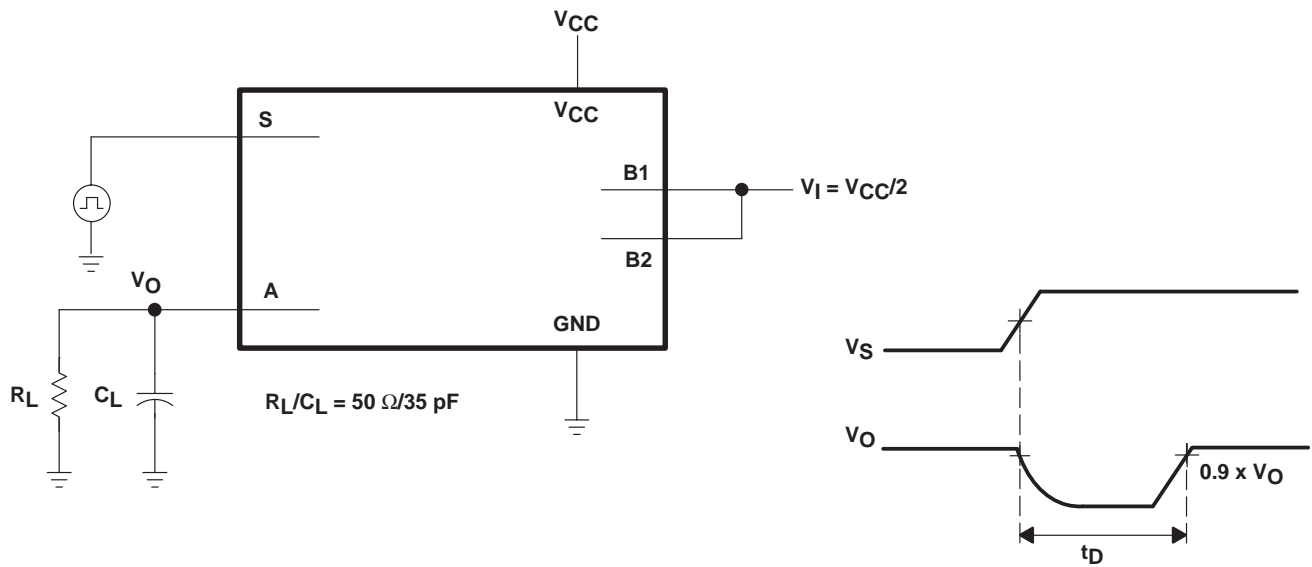
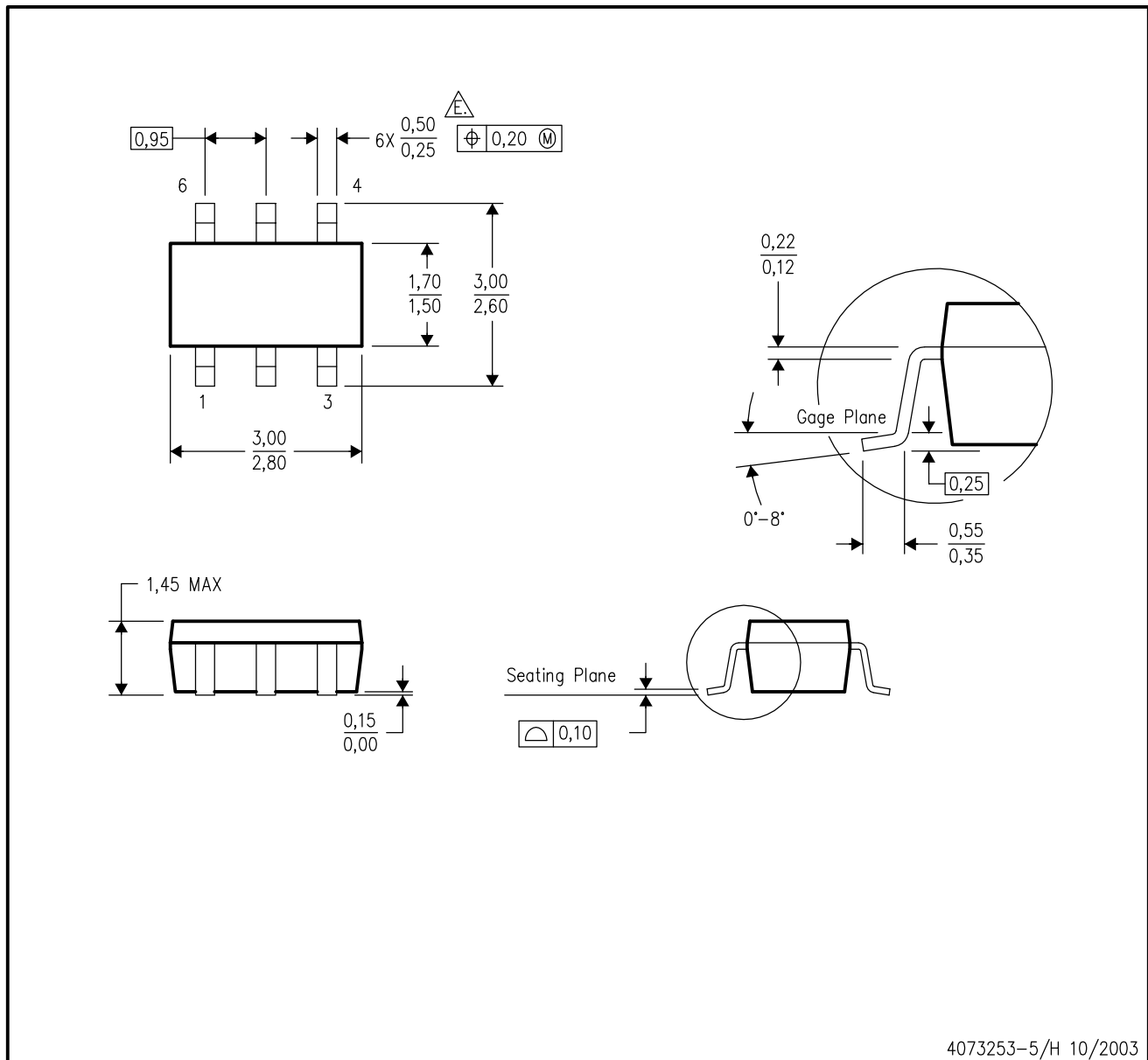


Figure 11. Break-Before-Make Internal Timing

DBV (R-PDSO-G6)

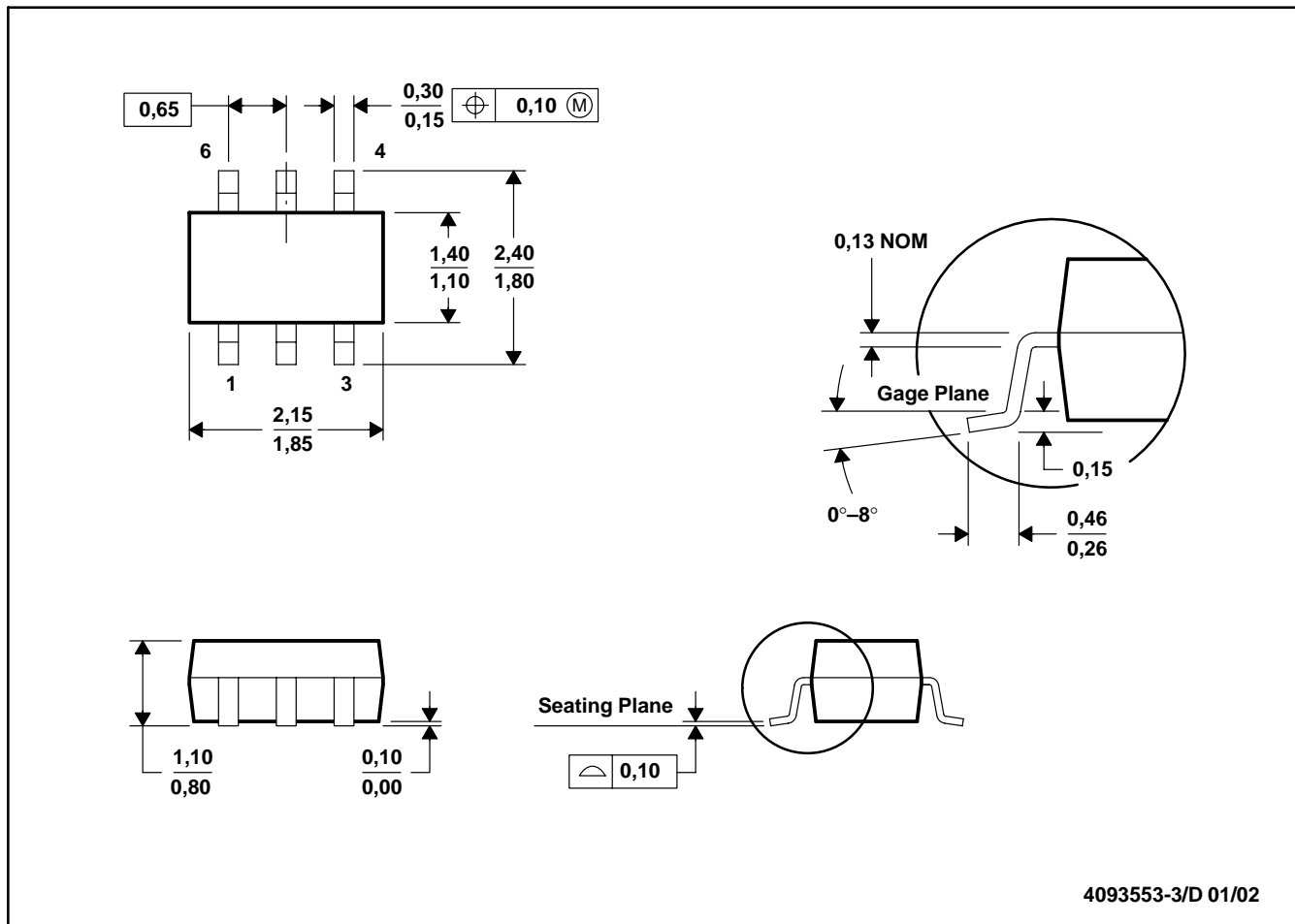
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
  - $\triangle$  Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DCK (R-PDSO-G6)

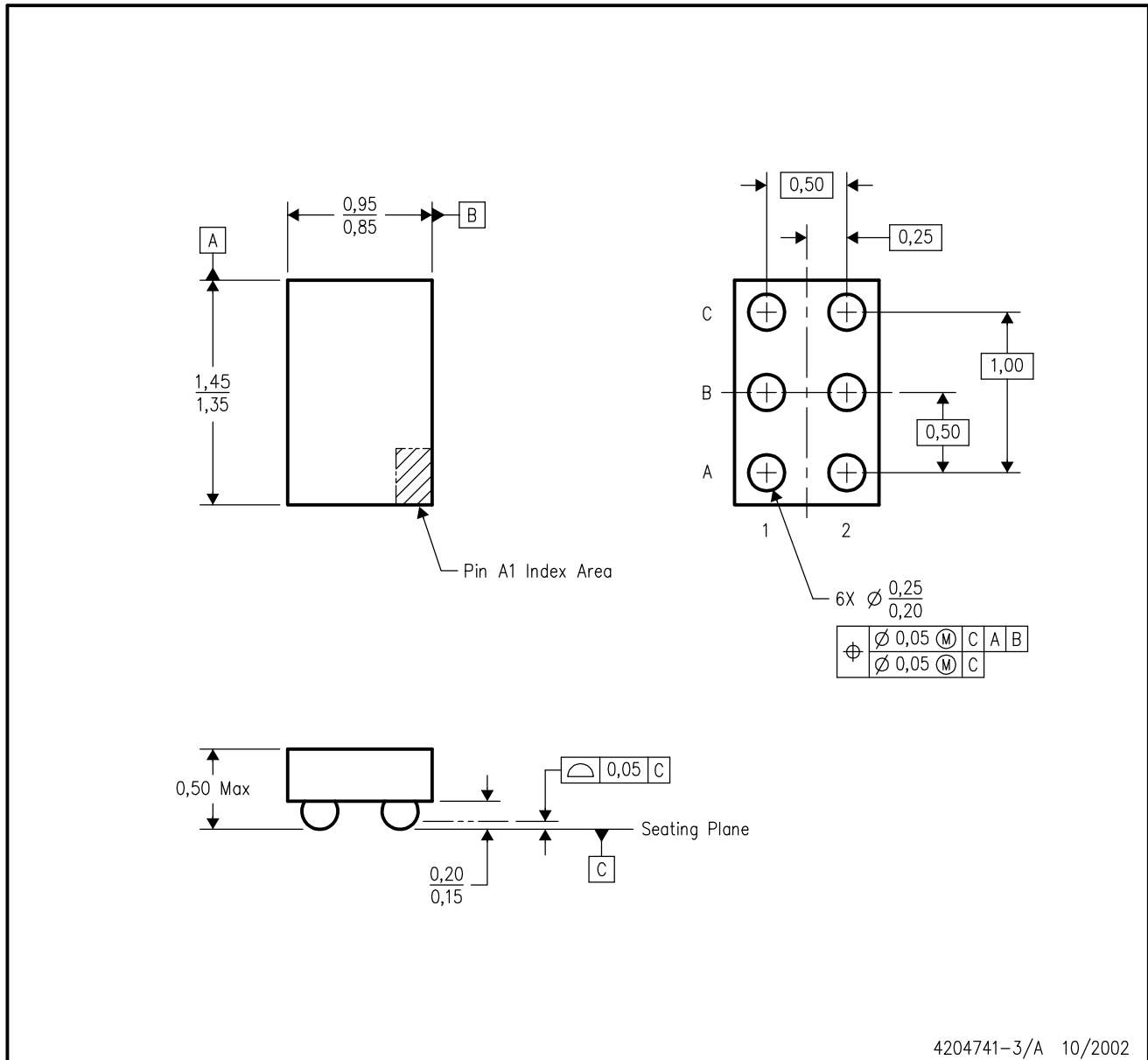
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion.  
 D. Falls within JEDEC MO-203

YZP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY

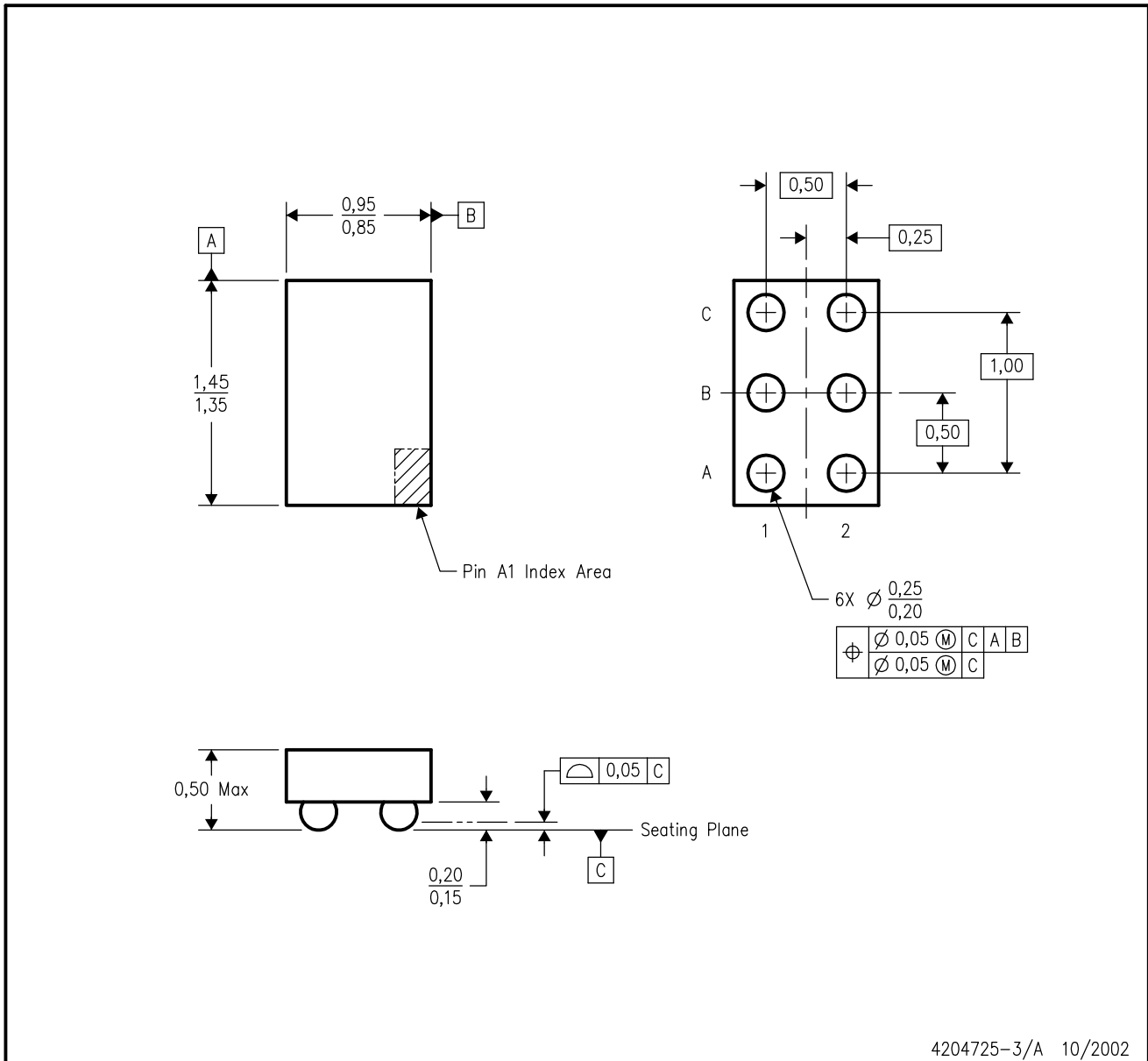


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.
  - D. This package is lead-free. Refer to the 6 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YEP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. NanoStar™ package configuration.
  - D. This package is tin-lead (SnPb). Refer to the 6 YZP package (drawing 4204741) for lead-free.

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