

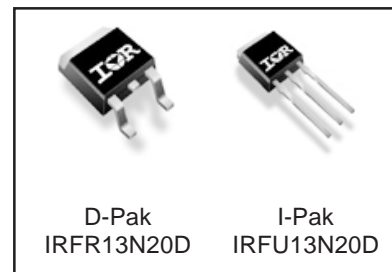
Applications

- High frequency DC-DC converters

V_{DSS}	R_{DS(on)} max	I_D
200V	0.235Ω	13A

Benefits

- Low Gate to Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	13	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	9.2	
I _{DM}	Pulsed Drain Current ①	52	
P _D @ T _C = 25°C	Power Dissipation	110	W
	Linear Derating Factor	0.71	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	2.2	V/ns
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Typical SMPS Topologies

- Telecom 48V input Forward Converters

Notes ① through ⑥ are on page 10
 www.irf.com

IRFR13N20D/IRFU13N20D

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Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	200	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.25	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.235	Ω	V _{GS} = 10V, I _D = 8.0A ④
V _{GS(th)}	Gate Threshold Voltage	3.0	—	5.5	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 200V, V _{GS} = 0V
		—	—	250		V _{DS} = 160V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	6.2	—	—	S	V _{DS} = 50V, I _D = 7.8A
Q _g	Total Gate Charge	—	25	38	nC	I _D = 7.8A
Q _{gs}	Gate-to-Source Charge	—	7.3	11		V _{DS} = 160V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	12	18		V _{GS} = 10V, ④
t _{d(on)}	Turn-On Delay Time	—	11	—	ns	V _{DD} = 100V
t _r	Rise Time	—	27	—		I _D = 7.8A
t _{d(off)}	Turn-Off Delay Time	—	17	—		R _G = 6.8Ω
t _f	Fall Time	—	10	—		V _{GS} = 10V ④
C _{iss}	Input Capacitance	—	830	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	140	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	35	—		f = 1.0MHz
C _{oss}	Output Capacitance	—	990	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	57	—		V _{GS} = 0V, V _{DS} = 160V, f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance	—	59	—		V _{GS} = 0V, V _{DS} = 0V to 160V ⑤

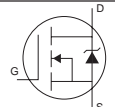
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy②	—	130	mJ
I _{AR}	Avalanche Current①	—	7.8	A
E _{AR}	Repetitive Avalanche Energy①	—	11	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	1.4	°C/W
R _{θJA}	Junction-to-Ambient (PCB mount)*	—	50	
R _{θJA}	Junction-to-Ambient	—	110	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	13	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	52		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 7.8A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	140	210	ns	T _J = 25°C, I _F = 7.8A
Q _{rr}	Reverse Recovery Charge	—	750	1120	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

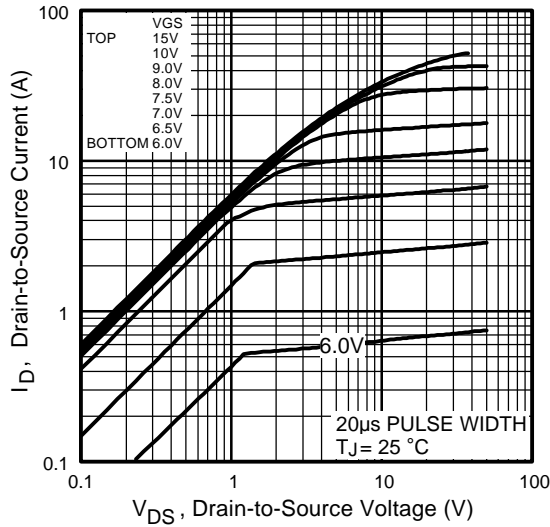


Fig 1. Typical Output Characteristics

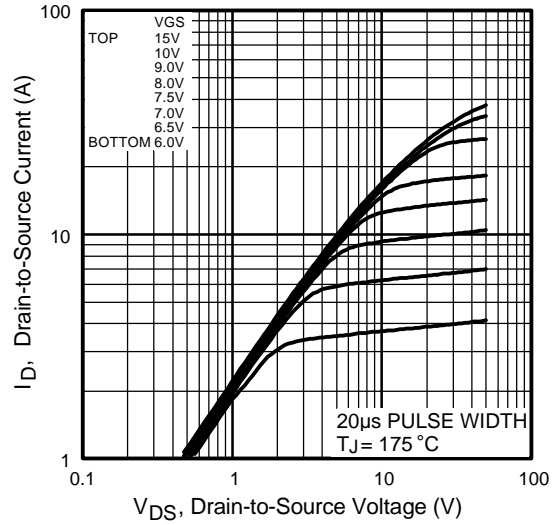


Fig 2. Typical Output Characteristics

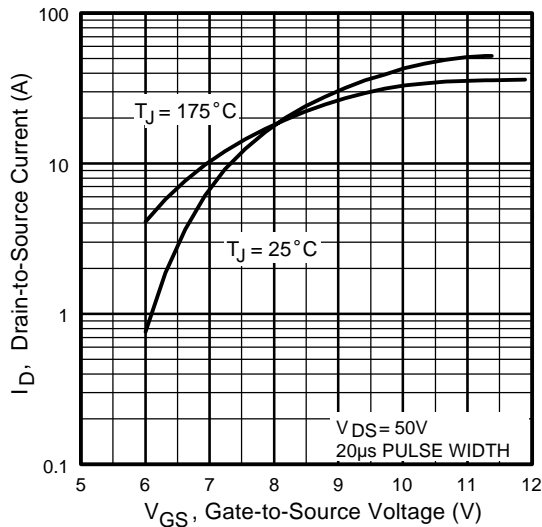


Fig 3. Typical Transfer Characteristics

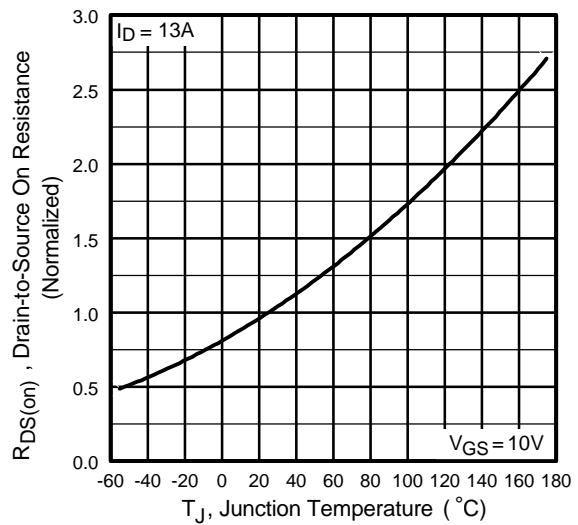


Fig 4. Normalized On-Resistance Vs. Temperature

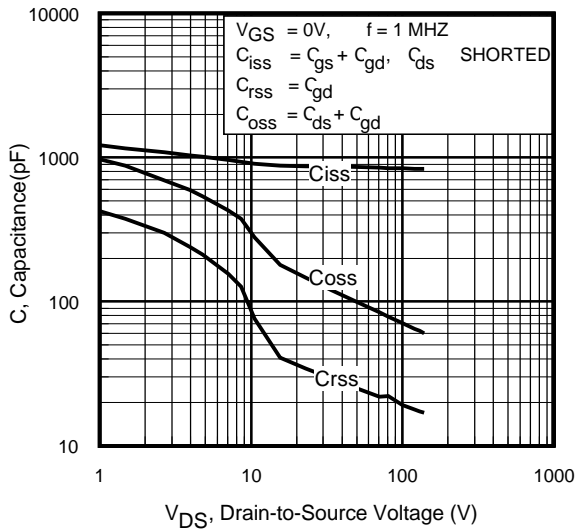


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

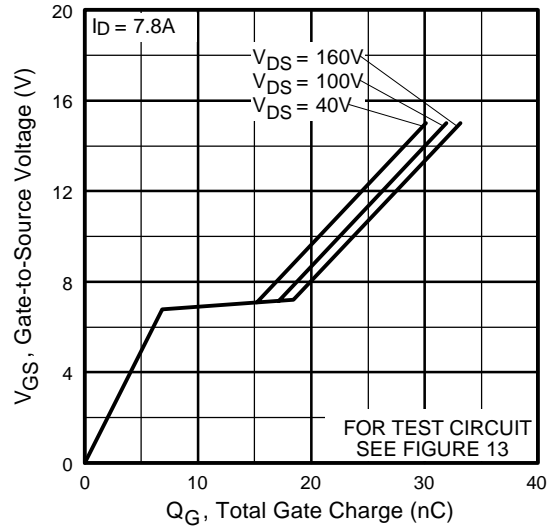


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

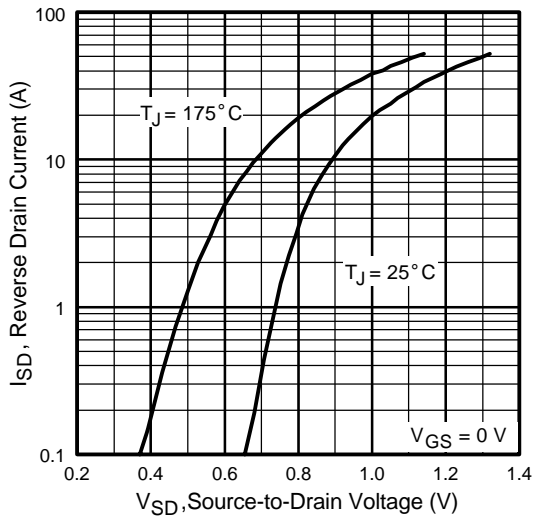


Fig 7. Typical Source-Drain Diode Forward Voltage

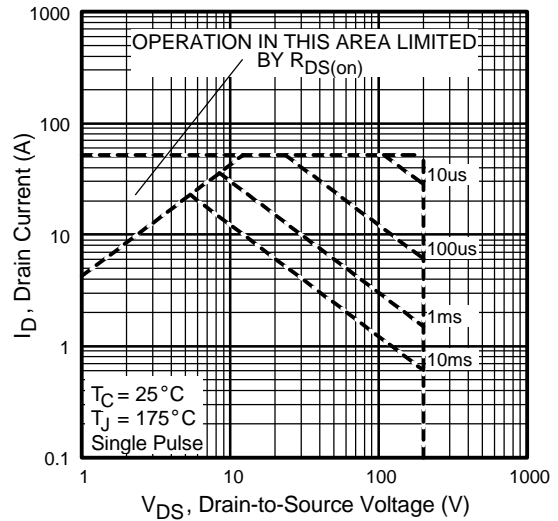


Fig 8. Maximum Safe Operating Area

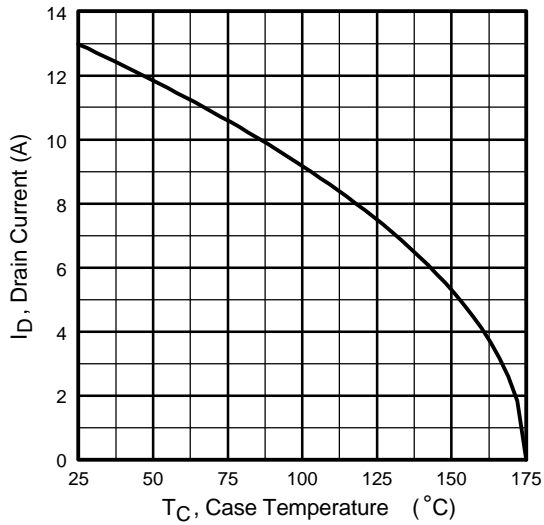


Fig 9. Maximum Drain Current Vs. Case Temperature

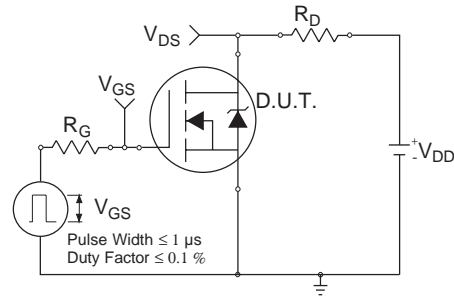


Fig 10a. Switching Time Test Circuit

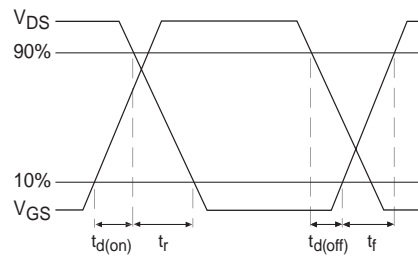


Fig 10b. Switching Time Waveforms

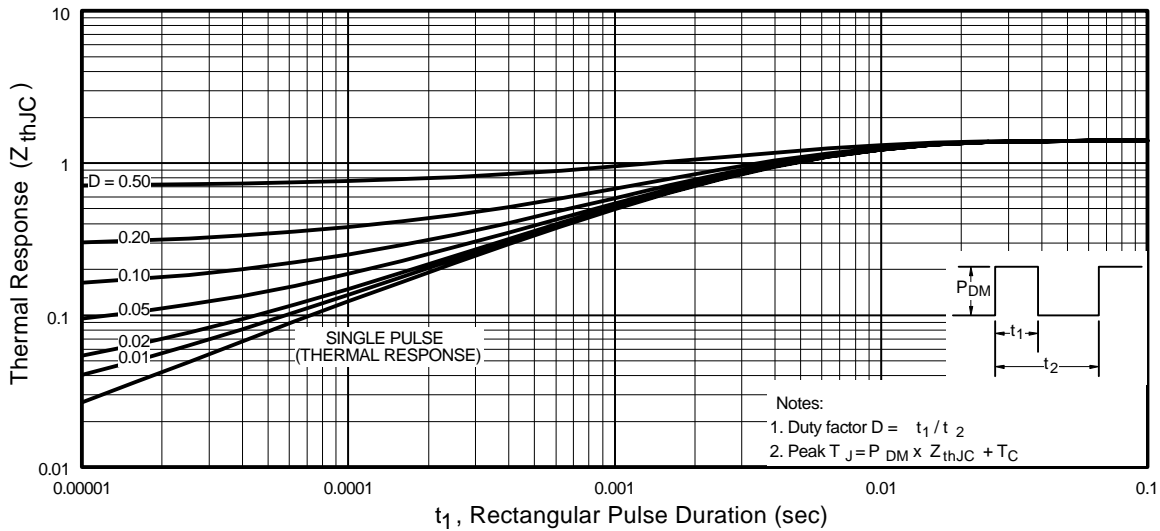
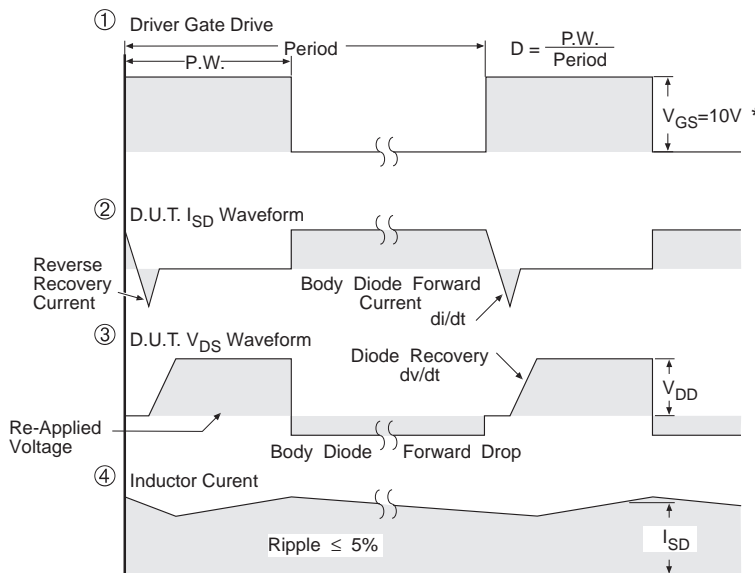
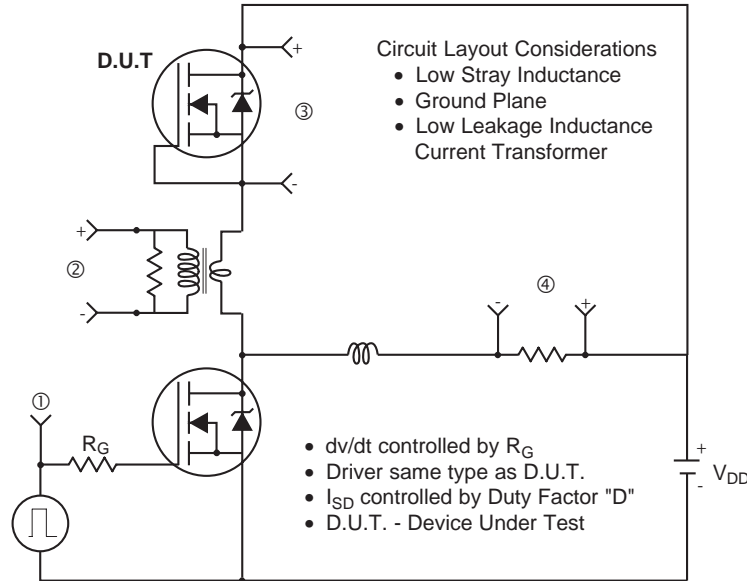


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

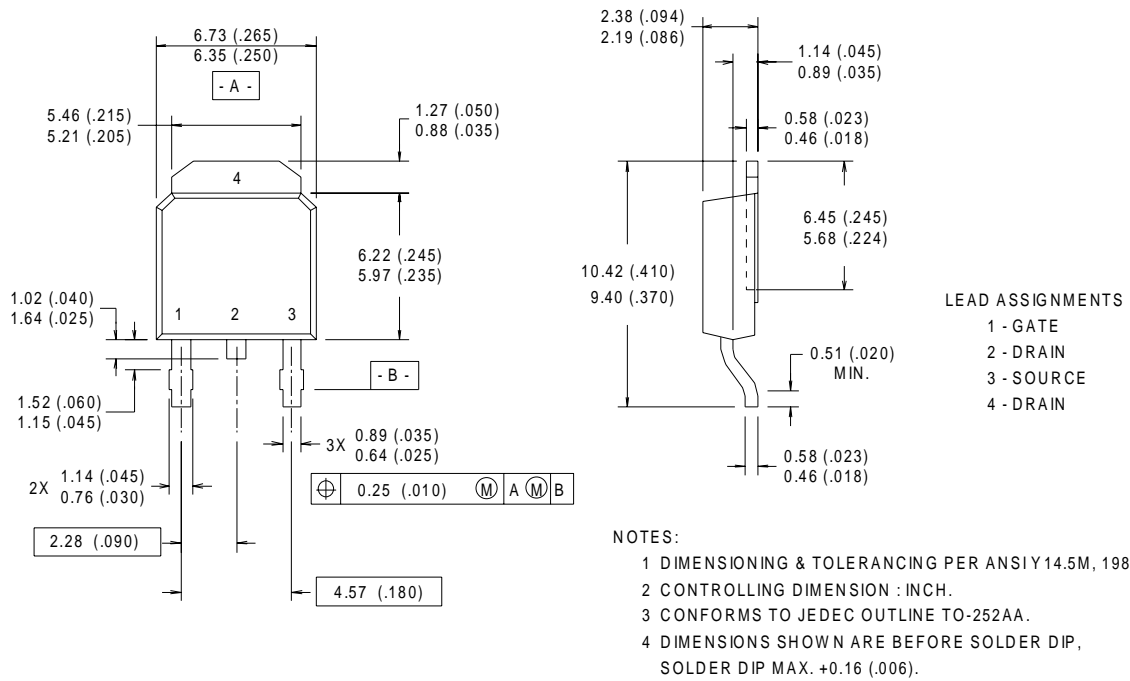
Fig 14. For N-Channel HEXFET® Power MOSFETs

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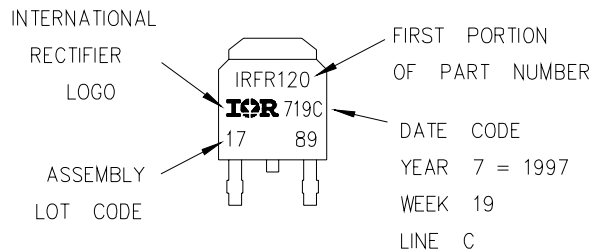
D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



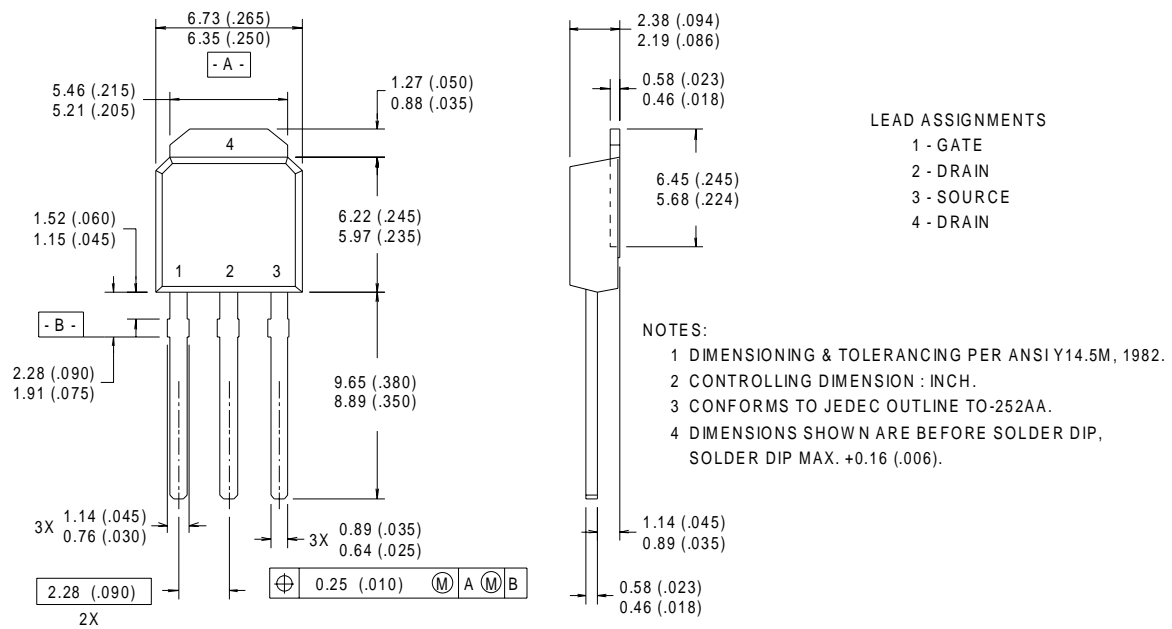
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"



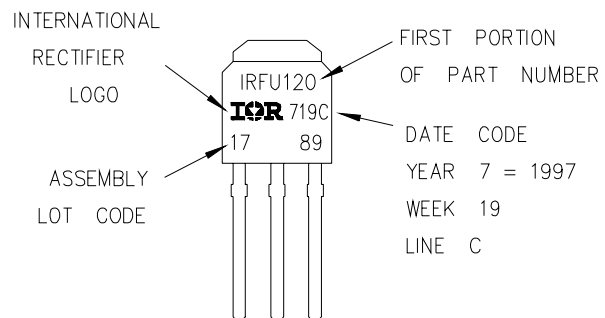
I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"

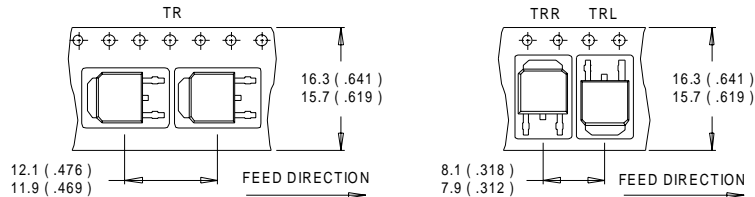


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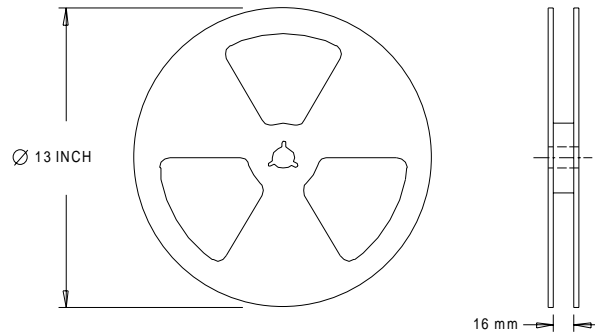
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 4.3\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 7.8\text{A}$.
- ③ $I_{SD} \leq 7.8\text{A}$, $di/dt \leq 81\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

* When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

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Data and specifications subject to change without notice. 2/2000