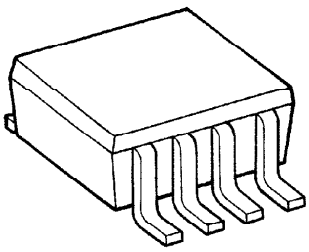
TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7WT74FU

(UNDER DEVELOPMENT)

D-TYPE FLIP FLOP WITH PRESET AND CLEAR

The TC7WT74FU is a high speed CMOS D-FLIP FLOP fabricated with silicon gate CMOS technology.
It achieves the high speed operation similar to equivalent Bipolar schottky TTL while maintaining the CMOS low power dissipation.
The input threshold levels are compatible with TTL output voltage.
The signal level applied to the D-INPUT is tranceferred to Q-OUTPUT during the positive going transition of the CK pulse. CLEAR and PRESET are independent of the CK and are accomplished by setting the appropriate input low.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



SSOP8-P-0.65

Weight : 0.02g (Typ.)

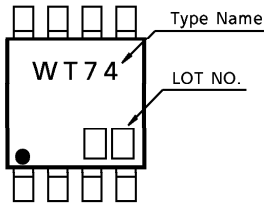
FEATURES

- High Speed ····· f_{MAX} = 53MHz (Typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 2μA (Max.) at Ta = 25°C
- Compatible with TTL outputs ····· V_{IL} = 0.8V (Max.), V_{IH} = 2.0V (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 4mA (Min.)

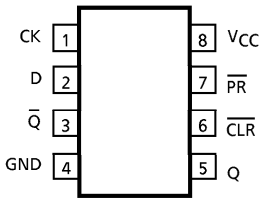
MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
DC Input Voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} / Ground Current	I_{CC}	±25	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature (10 s)	T_L	260	°C

MARKING



PIN ASSIGNMENT (TOP VIEW)



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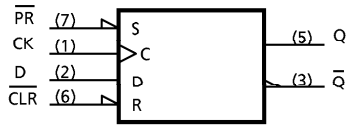
LOGIC DIAGRAM



TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	×	×	L	H	CLEAR
H	L	×	×	H	L	PRESET
L	L	×	×	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	×	↓	Q_n	$\overline{Q}_n$	NO CHANGE

× : Don't care

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	t_r, t_f	0~500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5~5.5	2.0	—	—	2.0	—	V
Low-Level Input Voltage	V_{IL}			4.5~5.5	—	—	0.8	—	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IL} or V_{IL}	I_{OH} = −20μA	4.5	4.4	4.5	—	4.4	—	V
			I_{OH} = −4mA	4.5	4.18	4.31	—	4.13	—	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH}	I_{OL} = 20μA	4.5	—	0.0	0.10	—	0.10	V
			I_{OL} = 4mA	4.5	—	0.17	0.26	—	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	2.0	—	20.0	μA
	I_{CCT}	PER INPUT: V_{IN} = 0.5V or 2.4V OTHER INPUT: V_{CC} or GND		5.5	—	—	2.0	—	2.9	mA

TIMING REQUIREMENTS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		Ta = −40~85°C	UNIT
			V_{CC} (V)	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CLOCK)	t_W (L) t_W (H)		4.5	—	25	29	ns
			5.5	—	20	23	
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	t_W (L)		4.5	—	30	34	ns
			5.5	—	25	28	
Minimum Set-up Time	t_s		4.5	—	25	29	ns
			5.5	—	20	23	
Minimum Hold Time	t_h		4.5	—	10	10	ns
			5.5	—	8	8	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		4.5	—	10	10	ns
			5.5	—	10	10	
Clock Frequency	f		4.5	—	22	16	MHz
			5.5	—	25	19	

AC ELECTRICAL CHARACTERISTICS ($C_L = 15pF$, $V_{CC} = 5V$, Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}	—	—	6	12	ns
Propagation Delay Time (CLOCK-Q, Q)	t_{pLH} t_{pHL}	—	—	17	28	ns
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$-Q, Q)	t_{pLH} t_{pHL}	—	—	20	30	ns
Maximum Clock Frequency	f_{MAX}	—	24	53	—	MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}	—	4.5	—	8	15	—	19	ns
	t_{THL}		5.5	—	7	13	—	16	
Propagation Delay Time (CLOCK-Q, $\overline{Q}$)	t_{pLH}	—	4.5	—	21	33	—	41	ns
	t_{pHL}		5.5	—	19	30	—	37	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$-Q, $\overline{Q}$)	t_{pLH}	—	4.5	—	23	35	—	43	ns
	t_{pHL}		5.5	—	20	32	—	40	
Maximum Clock Frequency	f_{MAX}	—	4.5	22	48	—	16	—	MHz
			5.5	25	53	—	19	—	
Input Capacitance	C_{IN}	—		—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 1)		—	34	—	—	—	pF

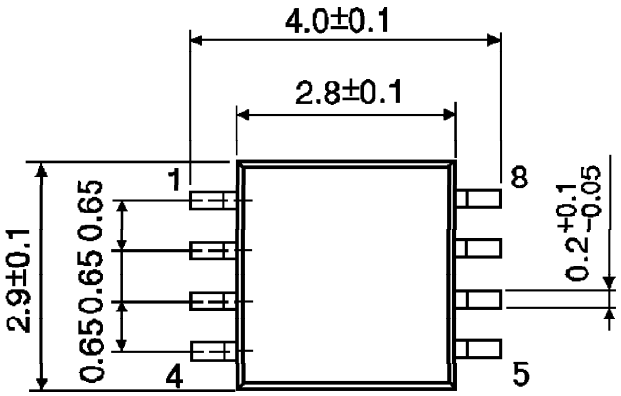
(Note 1) : C_{PD} is defined as the value of internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation.

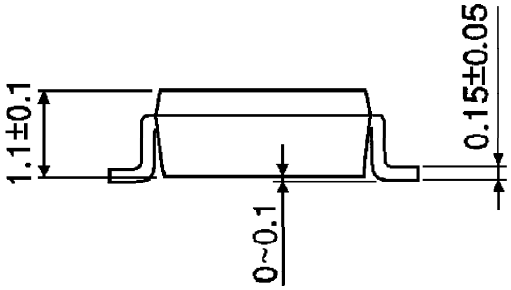
$$I_{CC\,(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

OUTLINE DRAWING

SSOP8-P-0.65

Unit : mm





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