

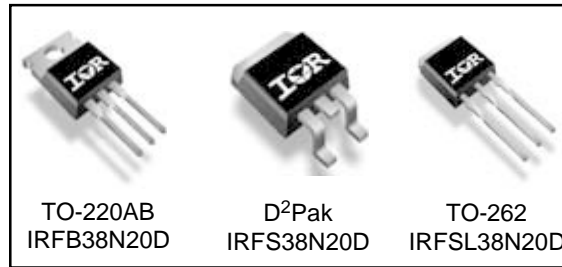
**Applications**

- High frequency DC-DC converters

<b>V<sub>DSS</sub></b>	<b>R<sub>DS(on) max</sub></b>	<b>I<sub>D</sub></b>
<b>200V</b>	<b>0.054Ω</b>	<b>44A</b>

**Benefits**

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C<sub>OSS</sub> to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



**Absolute Maximum Ratings**

	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	44	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	32	
I <sub>DM</sub>	Pulsed Drain Current ①	180	
P <sub>D</sub> @ T <sub>A</sub> = 25°C	Power Dissipation ②	3.8	W
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Power Dissipation	320	
	Linear Derating Factor	2.1	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	9.5	V/ns
T <sub>J</sub>	Operating Junction and	-55 to + 175	°C
T <sub>STG</sub>	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	
	Mounting torque, 6-32 or M3 screw④	10 lbf•in (1.1N•m)	

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	0.47	°C/W
R <sub>θCS</sub>	Case-to-Sink, Flat, Greased Surface ⑤	0.50	—	
R <sub>θJA</sub>	Junction-to-Ambient⑥	—	62	
R <sub>θJA</sub>	Junction-to-Ambient⑦	—	40	

Notes ① through ⑦ are on page 11

# IRFB/IRFS/IRFSL38N20D

International  
**IR** Rectifier

## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.22	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.054	$\Omega$	$V_{GS} = 10V, I_D = 26A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 160V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

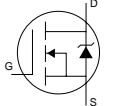
## Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	17	—	—	S	$V_{DS} = 50V, I_D = 26A$
$Q_g$	Total Gate Charge	—	76	110	nC	$I_D = 26A$
$Q_{gs}$	Gate-to-Source Charge	—	22	34		$V_{DS} = 160V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	34	51		$V_{GS} = 10V, \text{④}$
$t_{d(on)}$	Turn-On Delay Time	—	16	—	ns	$V_{DD} = 100V$
$t_r$	Rise Time	—	95	—		$I_D = 26A$
$t_{d(off)}$	Turn-Off Delay Time	—	29	—		$R_G = 2.5\Omega$
$t_f$	Fall Time	—	47	—		$V_{GS} = 10V, \text{④}$
$C_{iss}$	Input Capacitance	—	2900	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	450	—		$V_{DS} = 25V$
$C_{riss}$	Reverse Transfer Capacitance	—	73	—		$f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	3550	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	180	—		$V_{GS} = 0V, V_{DS} = 160V, f = 1.0\text{MHz}$
$C_{oss\ eff.}$	Effective Output Capacitance	—	380	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 160V \text{ ⑤}$

## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy②⑥	—	460	mJ
$I_{AR}$	Avalanche Current①	—	26	A
$E_{AR}$	Repetitive Avalanche Energy①	—	32	mJ

## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	44	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①⑥	—	—	180		
$V_{SD}$	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 26A, V_{GS} = 0V, \text{④}$
$t_{rr}$	Reverse Recovery Time	—	160	240	nS	$T_J = 25^\circ\text{C}, I_F = 26A$
$Q_{rr}$	Reverse Recovery Charge	—	1.3	2.0	$\mu C$	$di/dt = 100A/\mu s, \text{④}$
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

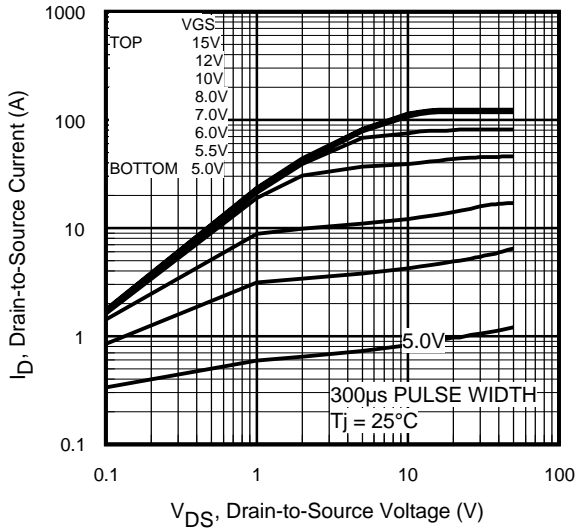


Fig 1. Typical Output Characteristics

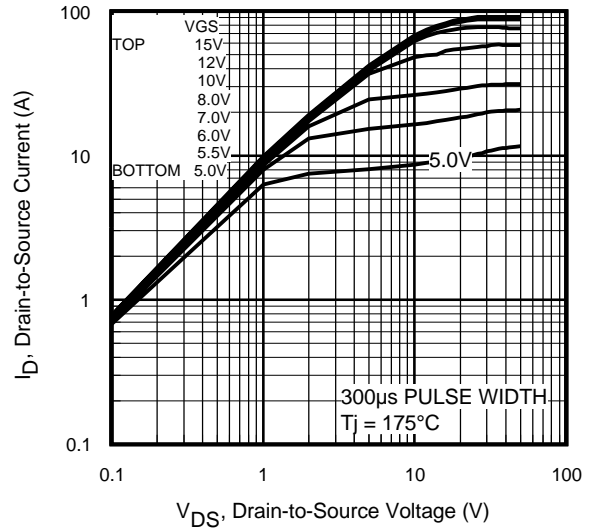


Fig 2. Typical Output Characteristics

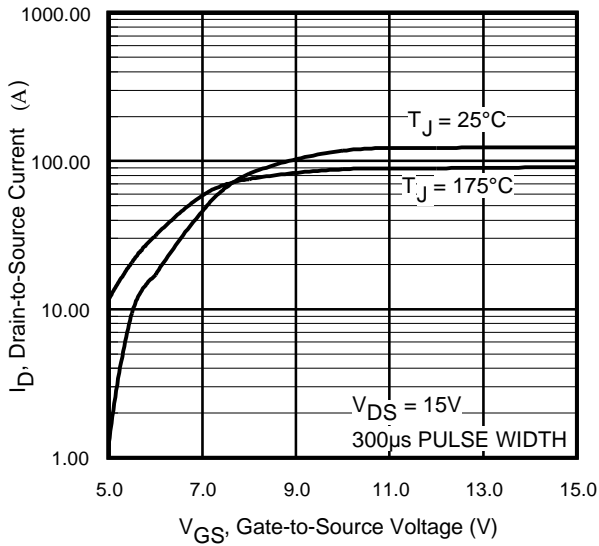


Fig 3. Typical Transfer Characteristics

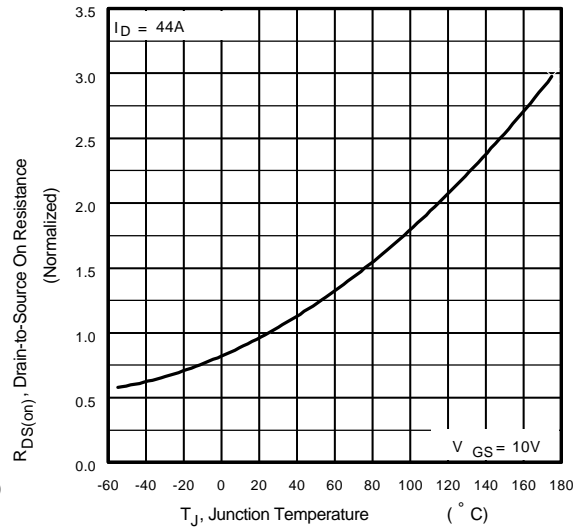
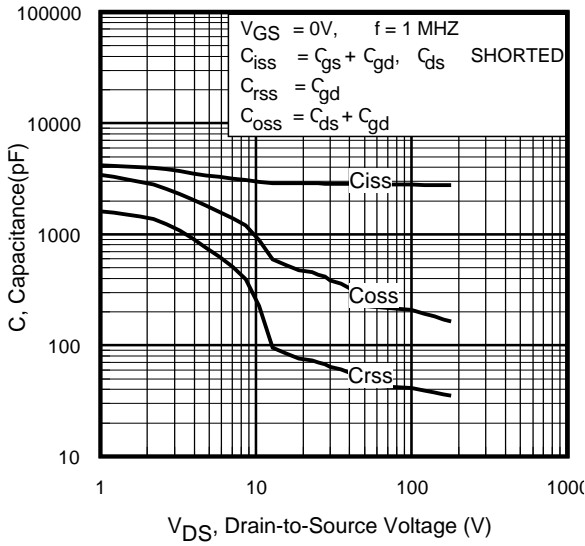
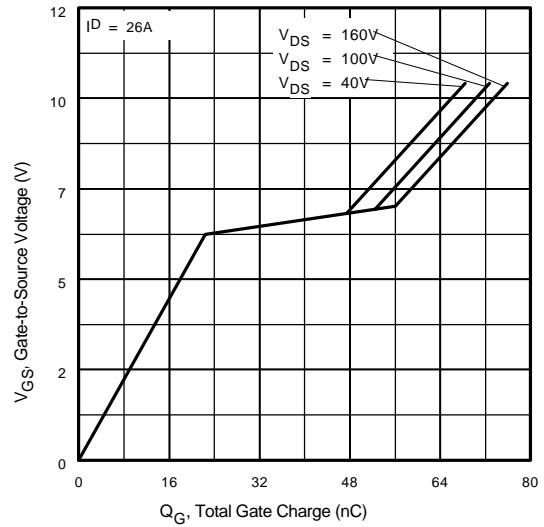


Fig 4. Normalized On-Resistance Vs. Temperature

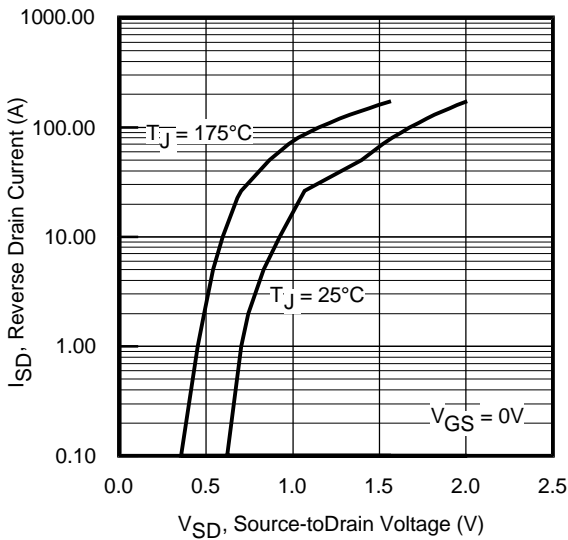
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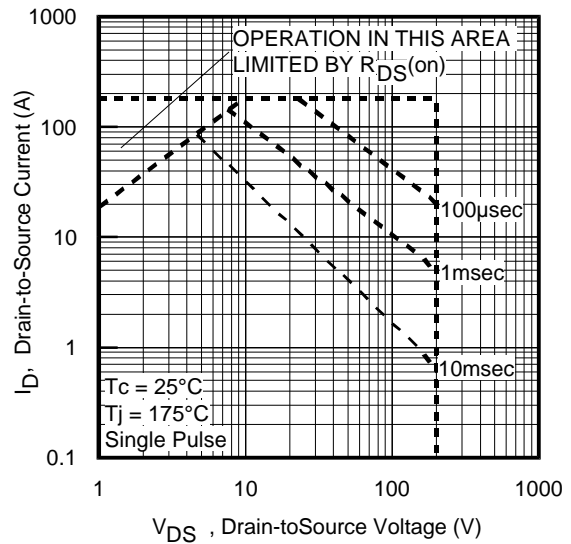
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



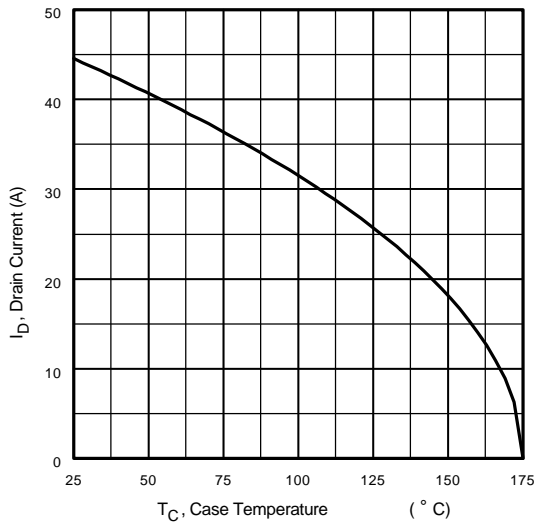
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



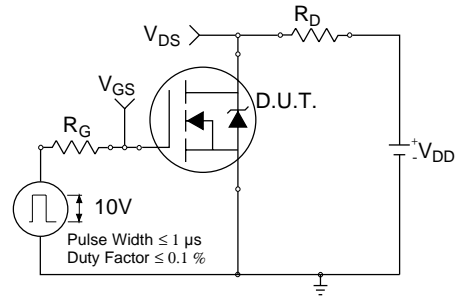
**Fig 7.** Typical Source-Drain Diode Forward Voltage



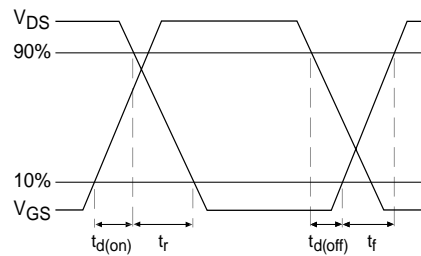
**Fig 8.** Maximum Safe Operating Area



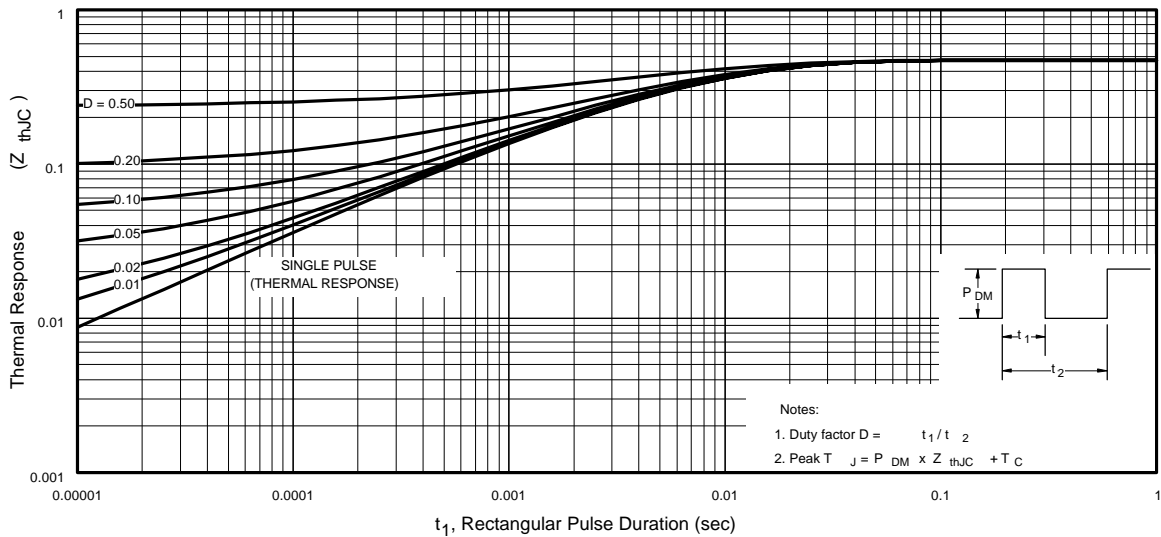
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



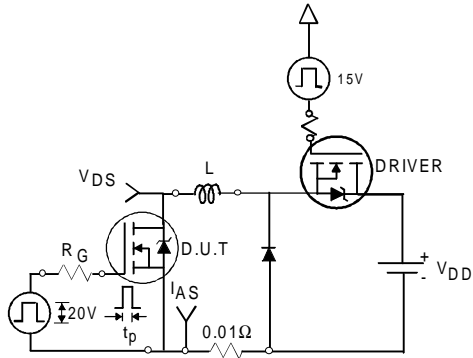
**Fig 10b.** Switching Time Waveforms



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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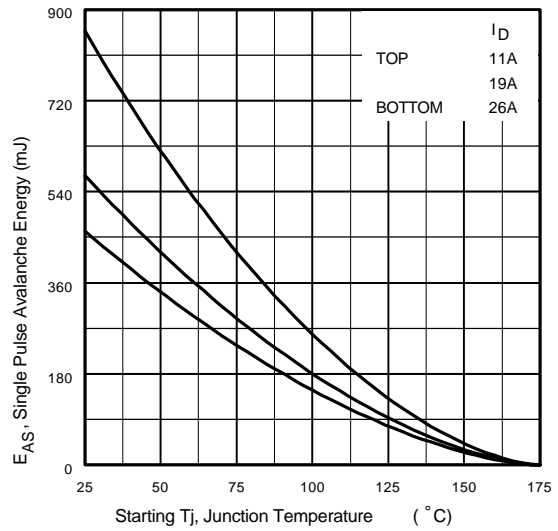
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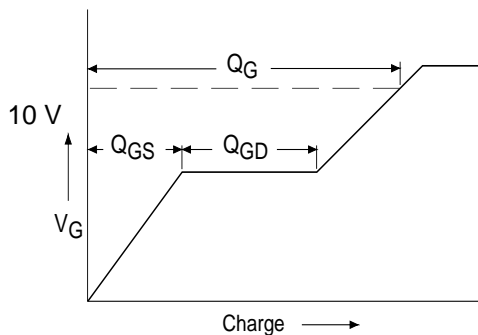
**Fig 12a.** Unclamped Inductive Test Circuit



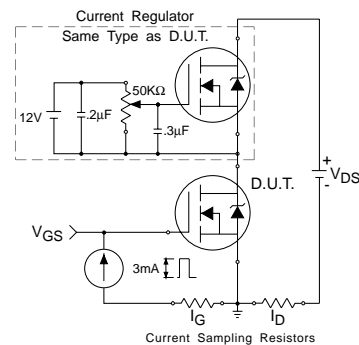
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

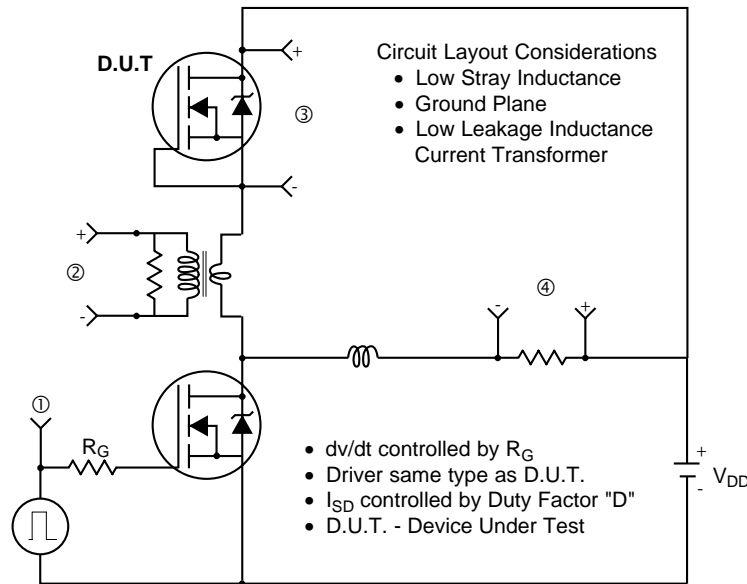


**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

**Peak Diode Recovery dv/dt Test Circuit**



\*  $V_{GS} = 5V$  for Logic Level Devices

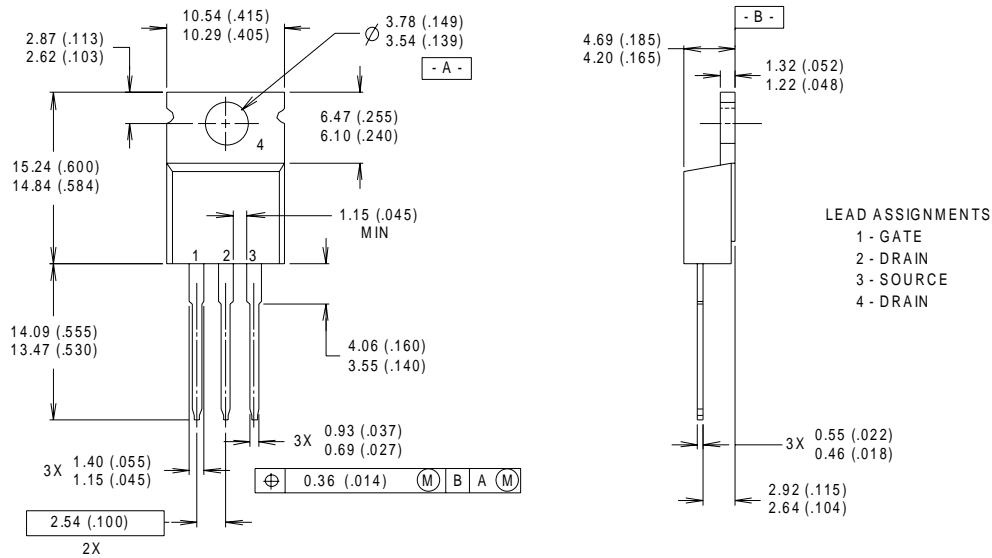
**Fig 14.** For N-Channel HEXFET® Power MOSFETs

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## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

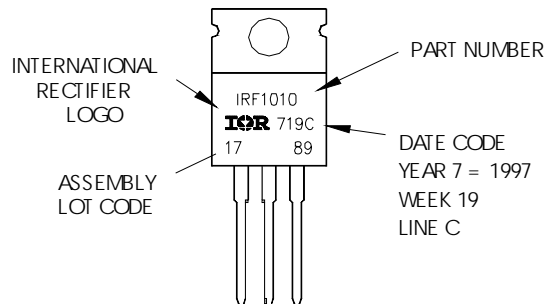


### NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANS Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

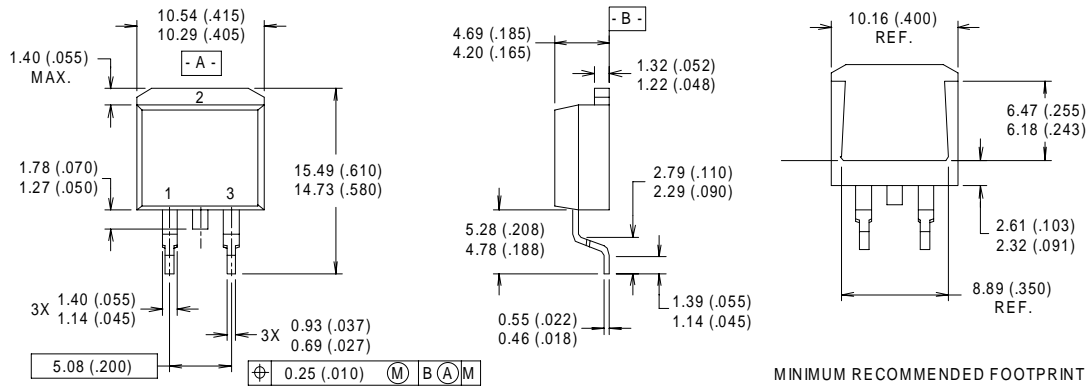
## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW19, 1997  
 IN THE ASSEMBLY LINE "C"





## D<sup>2</sup>Pak Package Outline



**NOTES:**

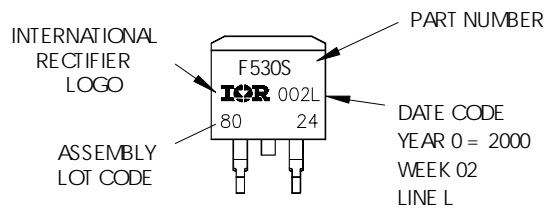
- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

**LEAD ASSIGNMENTS**

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

## D<sup>2</sup>Pak Part Marking Information

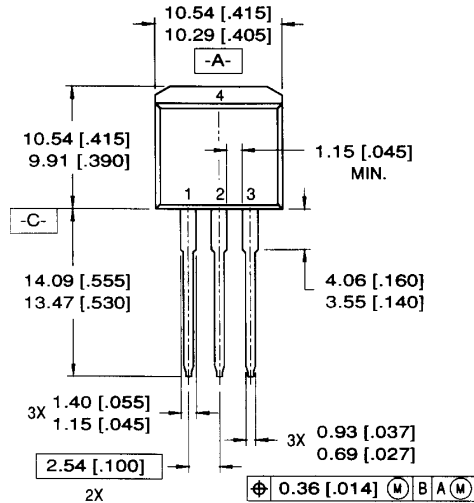
EXAMPLE: THIS IS AN IRF530S WITH  
 LOT CODE 8024  
 ASSEMBLED ON WW02, 2000  
 IN THE ASSEMBLY LINE "L"



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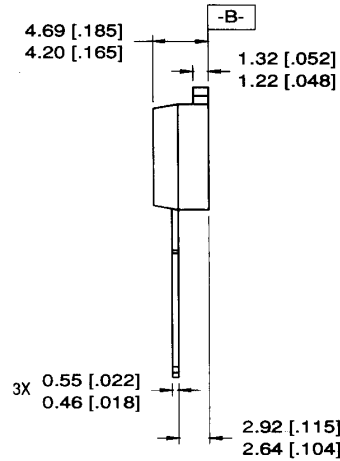
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## TO-262 Package Outline



### LEAD ASSIGNMENTS

1 = GATE      3 = SOURCE  
2 = DRAIN    4 = DRAIN

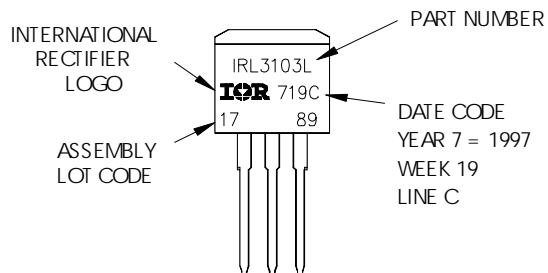


### NOTES:

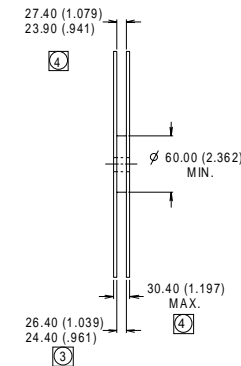
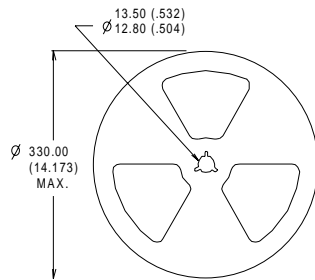
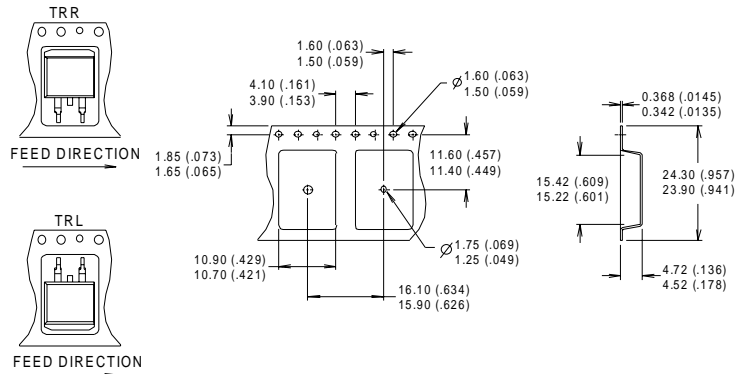
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
LOT CODE 1789  
ASSEMBLED ON WW 19, 1997  
IN THE ASSEMBLY LINE "C"



## D<sup>2</sup>Pak Tape & Reel Information



- NOTES:
1. CONFORMS TO EIA-418.
  2. CONTROLLING DIMENSION: MILLIMETER.
  - ③ DIMENSION MEASURED @ HUB.
  - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1.3\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 26\text{A}$ .
- ③  $I_{SD} \leq 26\text{A}$ ,  $di/dt \leq 390\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{OSS}$  eff. is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥ This is only applied to TO-220AB package.
- ⑦ This is applied to D<sup>2</sup>Pak, when mounted on 1" square PCB ( FR-4 or G-10 Material ).  
 For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.  
 This product has been designed and qualified for the Automotive [Q101] (IRFB38N20D),  
 & Industrial (IRFS/SL38N20D) market.  
 Qualification Standards can be found on IR's Web site.