

# DAC121S101

## 12-Bit Micro Power Digital-to-Analog Converter with Rail-to-Rail Output

### General Description

The DAC121S101 is a full-featured, general purpose 12-bit voltage-output digital-to-analog converter (DAC) that can operate from a single +2.7V to 5.5V supply and consumes just 177  $\mu$ A of current at 3.6 Volts. The on-chip output amplifier allows rail-to-rail output swing and the three wire serial interface operates at clock rates up to 30 MHz over the specified supply voltage range and is compatible with standard SPI™, QSPI, MICROWIRE and DSP interfaces. Competitive devices are limited to 20 MHz clock rates at supply voltages in the 2.7V to 3.6V range.

The supply voltage for the DAC121S101 serves as its voltage reference, providing the widest possible output dynamic range. A power-on reset circuit ensures that the DAC output powers up to zero volts and remains there until there is a valid write to the device. A power-down feature reduces power consumption to less than a microWatt.

The low power consumption and small packages of the DAC121S101 make it an excellent choice for use in battery operated equipment.

The DAC121S101 is a direct replacement for the AD5320 and the DAC7512 and is one of a family of pin compatible DACs, including the 8-bit DAC081S101 and the 10-bit DAC101S101. The DAC121S101 operates over the extended industrial temperature range of  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ .

### Features

- Guaranteed Monotonicity
- Low Power Operation
- Rail-to-Rail Voltage Output
- Power-on Reset to Zero Volts Output
- SYNC Interrupt Facility
- Wide power supply range (+2.7V to +5.5V)
- Small Packages
- Power Down Feature

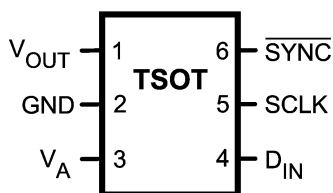
### Key Specifications

- Resolution 12 bits
- DNL  $+0.25, -0.15$  LSB (typ)
- Output Settling Time 8  $\mu$ s (typ)
- Zero Code Error 4 mV (typ)
- Full-Scale Error  $-0.06$  %FS (typ)
- Power Consumption
  - Normal Mode 0.64mW (3.6V) / 1.43mW (5.5V) typ
  - Pwr Down Mode 0.14 $\mu$ W (3.6V) / 0.39 $\mu$ W (5.5V) typ

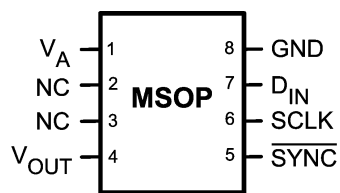
### Applications

- Battery-Powered Instruments
- Digital Gain and Offset Adjustment
- Programmable Voltage & Current Sources
- Programmable Attenuators

### Pin Configuration



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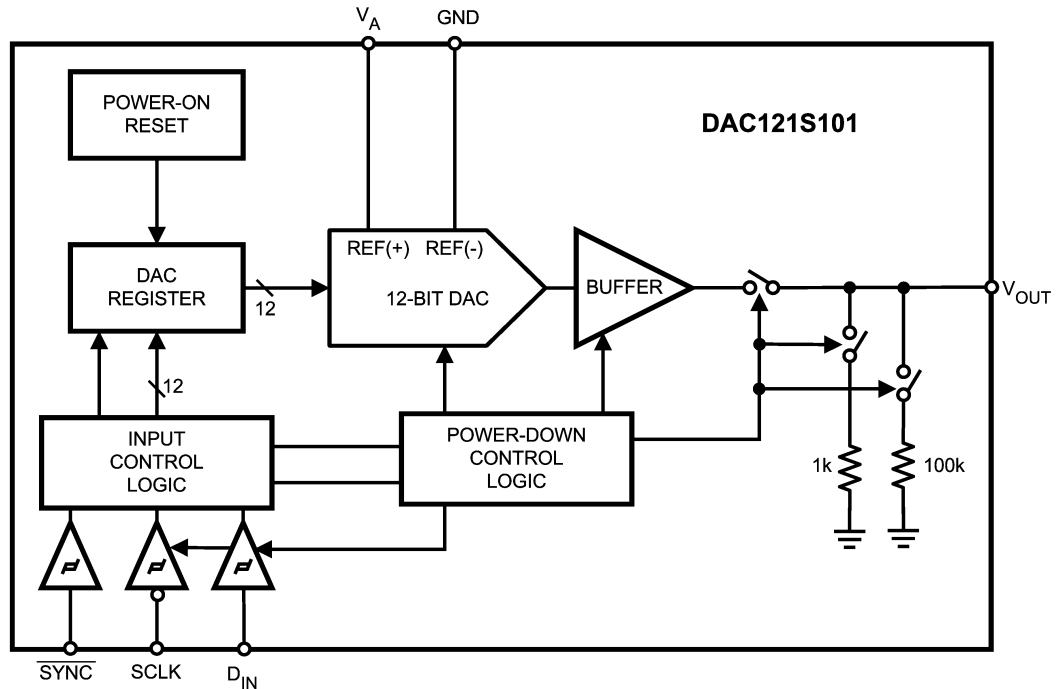
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### Ordering Information

Order Numbers	Temperature Range	Package	Top Mark
DAC121S101CIMM	$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$	MSOP	X60C
DAC121S101CIMMX	$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$	MSOP Tape-and-Reel	X60C
DAC121S101CIMK	$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$	TSOT	X61C
DAC121S101CIMKX	$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$	TSOT Tape-and-Reel	X61C
DAC121S101EVAL		Evaluation Board	

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## Block Diagram



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## Pin Descriptions

TSOT (SOT-23) Pin No.	MSOP Pin No.	Symbol	Description
1	4	V <sub>OUT</sub>	DAC Analog Output Voltage.
2	8	GND	Ground reference for all on-chip circuitry.
3	1	V <sub>A</sub>	Power supply and Reference input. Should be decoupled to GND.
4	7	D <sub>IN</sub>	Serial Data Input. Data is clocked into the 16-bit shift register on the falling edges of SCLK after the fall of $\overline{\text{SYNC}}$ .
5	6	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edges of this pin.
6	5	$\overline{\text{SYNC}}$	Frame synchronization input for the data input. When this pin goes low, it enables the input shift register and data is transferred on the falling edges of SCLK. The DAC is updated on the 16th clock cycle unless $\overline{\text{SYNC}}$ is brought high before the 16th clock, in which case the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the DAC.
	2, 3	NC	No Connect. There is no internal connection to these pins.

## Absolute Maximum Ratings

(Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, $V_A$	6.5V
Voltage on any Input Pin	-0.3V to ( $V_A + 0.3V$ )
Input Current at Any Pin (Note 3)	10 mA
Package Input Current (Note 3)	20 mA
Power Consumption at $T_A = 25^\circ\text{C}$	See (Note 4)
ESD Susceptibility (Note 5)	
Human Body Model	2500V
Machine Model	250V
Soldering Temperature, Infrared, 10 Seconds (Note 6)	235°C

Storage Temperature

-65°C to +150°C

## Operating Ratings (Notes 1, 2)

Operating Temperature Range	-40°C ≤ $T_A$ ≤ +105°C
Supply Voltage, $V_A$	+2.7V to 5.5V
Any Input Voltage (Note 7)	-0.1 V to ( $V_A + 0.1$ V)
Output Load	0 to 1500 pF
SCLK Frequency	Up to 30 MHz

## Package Thermal Resistances

Package	$\theta_{JA}$
8-Lead MSOP	240°C/W
6-Lead TSOT	250°C/W

## Electrical Characteristics

Values shown in this table are design targets and are subject to change before product release. The following specifications apply for  $V_A = +2.7V$  to +5.5V,  $R_L = 2k\Omega$  to GND,  $C_L = 200$  pF to GND,  $f_{SCLK} = 30$  MHz, input code range 48 to 4047.

**Boldface limits apply for  $T_{MIN} \leq T_A \leq T_{MAX}$ :** all other limits  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 9)	Units (Limits)
<b>STATIC PERFORMANCE</b>					
	Resolution			<b>12</b>	Bits (min)
	Monotonicity			<b>12</b>	Bits (min)
INL	Integral Non-Linearity	Over Decimal codes 48 to 4047	±2.6	<b>±8</b>	LSB (max)
DNL	Differential Non-Linearity	$V_A = 2.7V$ to 5.5V	+0.25 -0.15	<b>+1.0</b> <b>-0.7</b>	LSB (max) LSB (min)
		$V_A = 4.5V$ to 5.5V (Note 10)	±0.11	<b>±0.5</b>	LSB (max)
ZE	Zero Code Error	$I_{OUT} = 0$	+4	<b>+15</b>	mV (max)
FSE	Full-Scale Error	$I_{OUT} = 0$	-0.06	<b>-1.0</b>	%FSR (max)
GE	Gain Error	All ones Loaded to DAC register	-0.10	<b>±1.0</b>	%FSR
ZCED	Zero Code Error Drift		-20		$\mu\text{V}/^\circ\text{C}$
TC GE	Gain Error Tempco	$V_A = 3V$	-0.7		ppm/ $^\circ\text{C}$
		$V_A = 5V$	-1.0		ppm/ $^\circ\text{C}$
<b>OUTPUT CHARACTERISTICS</b>					
	Output Voltage Range	(Note 10)		<b>0</b> <b><math>V_A</math></b>	V (min) V (max)
ZCO	Zero Code Output	$V_A = 3V$ , $I_{OUT} = 10 \mu\text{A}$	1.8		mV
		$V_A = 3V$ , $I_{OUT} = 100 \mu\text{A}$	5.0		mV
		$V_A = 5V$ , $I_{OUT} = 10 \mu\text{A}$	3.7		mV
		$V_A = 5V$ , $I_{OUT} = 100 \mu\text{A}$	5.4		mV
FSO	Full Scale Output	$V_A = 3V$ , $I_{OUT} = 10 \mu\text{A}$	2.997		V
		$V_A = 3V$ , $I_{OUT} = 100 \mu\text{A}$	2.990		V
		$V_A = 5V$ , $I_{OUT} = 10 \mu\text{A}$	4.995		V
		$V_A = 5V$ , $I_{OUT} = 100 \mu\text{A}$	4.992		V
	Maximum Load Capacitance	$R_L = \infty$	1500		pF
		$R_L = 2k\Omega$	1500		pF
	DC Output Impedance		1.3		Ohm

## Electrical Characteristics (Continued)

Values shown in this table are design targets and are subject to change before product release. The following specifications apply for  $V_A = +2.7V$  to  $+5.5V$ ,  $R_L = 2k\Omega$  to GND,  $C_L = 200$  pF to GND,  $f_{SCLK} = 30$  MHz, input code range 48 to 4047. **Boldface limits apply for  $T_{MIN} \leq T_A \leq T_{MAX}$** ; all other limits  $T_A = 25^\circ C$ , unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 9)	Units (Limits)		
$I_{OS}$	Output Short Circuit Current	$V_A = 5V$ , $V_{OUT} = 0V$ , Input code = FFFh	-63		mA		
		$V_A = 3V$ , $V_{OUT} = 0V$ , Input code = FFFh	-50		mA		
		$V_A = 5V$ , $V_{OUT} = 5V$ , Input code = 000h	74		mA		
		$V_A = 3V$ , $V_{OUT} = 3V$ , Input code = 000h	53		mA		
<b>LOGIC INPUT</b>							
$I_{IN}$	Input Current (Note 10)			<b><math>\pm 1</math></b>	$\mu A$ (max)		
$V_{IL}$	Input Low Voltage (Note 10)	$V_A = 5V$		<b>0.8</b>	V (max)		
		$V_A = 3V$		<b>0.5</b>	V (max)		
$V_{IH}$	Input High Voltage (Note 10)	$V_A = 5V$		<b>2.4</b>	V (min)		
		$V_A = 3V$		<b>2.1</b>	V (min)		
$C_{IN}$	Input Capacitance (Note 10)			<b>3</b>	pF (max)		
<b>POWER REQUIREMENTS</b>							
$I_A$	Supply Current (output unloaded)	Normal Mode $f_{SCLK} = 30$ MHz	$V_A = 5.5V$	260	<b>312</b>	$\mu A$ (max)	
			$V_A = 3.6V$	177	<b>217</b>	$\mu A$ (max)	
		Normal Mode $f_{SCLK} = 20$ MHz	$V_A = 5.5V$	224	<b>279</b>	$\mu A$ (max)	
			$V_A = 3.6V$	158	<b>197</b>	$\mu A$ (max)	
		Normal Mode $f_{SCLK} = 0$	$V_A = 5.5V$	153		$\mu A$ (max)	
			$V_A = 3.6V$	118		$\mu A$ (max)	
		All PD Modes, $f_{SCLK} = 30$ MHz	$V_A = 5.0V$	84		$\mu A$ (max)	
			$V_A = 3.0V$	42		$\mu A$ (max)	
All PD Modes, $f_{SCLK} = 20$ MHz	$V_A = 5.0V$	56		$\mu A$ (max)			
	$V_A = 3.0V$	28		$\mu A$ (max)			
All PD Modes, $f_{SCLK} = 0$ (Note 10)	$V_A = 5.5V$	0.07		<b>1.0</b>	$\mu A$ (max)		
	$V_A = 3.6V$	0.04		<b>1.0</b>	$\mu A$ (max)		
$P_C$	Power Consumption (output unloaded)	Normal Mode $f_{SCLK} = 30$ MHz	$V_A = 5.5V$	1.43	<b>1.72</b>	mW (max)	
			$V_A = 3.6V$	0.64	<b>0.78</b>	mW (max)	
		Normal Mode $f_{SCLK} = 20$ MHz	$V_A = 5.5V$	1.23		<b>1.53</b>	mW (max)
			$V_A = 3.6V$	0.57		<b>0.71</b>	mW (max)
		Normal Mode $f_{SCLK} = 0$	$V_A = 5.5V$	0.84			$\mu W$ (max)
			$V_A = 3.6V$	0.42			$\mu W$ (max)
		All PD Modes, $f_{SCLK} = 30$ MHz	$V_A = 5.0V$	0.42			$\mu W$ (max)
			$V_A = 3.0V$	0.13			$\mu W$ (max)
All PD Modes, $f_{SCLK} = 20$ MHz	$V_A = 5.0V$	0.28			$\mu W$ (max)		
	$V_A = 3.0V$	0.08			$\mu W$ (max)		
All PD Modes, $f_{SCLK} = 0$ (Note 10)	$V_A = 5.5V$	0.39		<b>5.5</b>	$\mu W$ (max)		
	$V_A = 3.6V$	0.14		<b>3.6</b>	$\mu W$ (max)		
$I_{OUT} / I_A$	Power Efficiency	$I_{LOAD} = 2mA$	$V_A = 5V$	91		%	
			$V_A = 3V$	94		%	

## A.C. and Timing Characteristics

Values shown in this table are design targets and are subject to change before product release. The following specifications apply for  $V_A = +2.7V$  to  $+5.5V$ ,  $R_L = 2k\Omega$  to GND,  $C_L = 200$  pF to GND,  $f_{SCLK} = 30$  MHz, input code range 48 to 4047.

**Boldface limits apply for  $T_{MIN} \leq T_A \leq T_{MAX}$** ; all other limits  $T_A = 25^\circ C$ , unless otherwise specified.

Symbol	Parameter	Conductions	Typical	Limits	Units (Limits)	
$f_{SCLK}$	SCLK Frequency			<b>30</b>	MHz (max)	
$t_s$	Output Voltage Settling Time (Note 10)	400h to C00h code change, $R_L = 2k\Omega$	$C_L \leq 200$ pF	8	<b>10</b>	$\mu s$ (max)
			$C_L = 500$ pF	12		$\mu s$
		00Fh to FF0h code change, $R_L = 2k\Omega$	$C_L \leq 200$ pF	8		$\mu s$
			$C_L = 500$ pF	12		$\mu s$
SR	Output Slew Rate		1		V/ $\mu s$	
	Glitch Impulse	Code change from 800h to 7FFh	12		nV-sec	
	Digital Feedthrough		0.5		nV-sec	
$t_{WU}$	Wake-Up Time	$V_A = 5V$	1.6		$\mu s$	
		$V_A = 3V$	1.9		$\mu s$	
$1/f_{SCLK}$	SCLK Cycle Time			<b>33</b>	ns (min)	
$t_H$	SCLK High time		5	<b>13</b>	ns (min)	
$t_L$	SCLK Low Time		5	<b>13</b>	ns (min)	
$t_{SUCL}$	Set-up Time $\overline{SYNC}$ to SCLK Rising Edge		-15	<b>0</b>	ns (min)	
$t_{SUD}$	Data Set-Up Time		2.5	<b>5</b>	ns (min)	
$t_{DHD}$	Data Hold Time		2.5	<b>4.5</b>	ns (min)	
$t_{CS}$	SCLK fall to rise of $\overline{SYNC}$	$V_A = 5V$	0	<b>3</b>	ns (min)	
		$V_A = 3V$	-2	<b>1</b>	ns (min)	
$t_{SYNC}$	$\overline{SYNC}$ High Time	$2.7 \leq V_A \leq 3.6$	9	<b>20</b>	ns (min)	
		$3.6 \leq V_A \leq 5.5$	5	<b>10</b>	ns (min)	

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

**Note 2:** All voltages are measured with respect to GND = 0V, unless otherwise specified

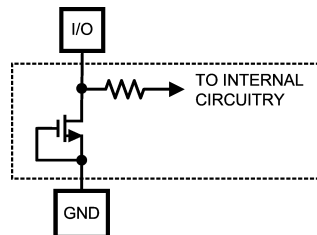
**Note 3:** When the input voltage at any pin exceeds the power supplies (that is, less than GND, or greater than  $V_A$ ), the current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.

**Note 4:** The absolute maximum junction temperature ( $T_{Jmax}$ ) for this device is  $150^\circ C$ . The maximum allowable power dissipation is dictated by  $T_{Jmax}$ , the junction-to-ambient thermal resistance ( $\theta_{JA}$ ), and the ambient temperature ( $T_A$ ), and can be calculated using the formula  $P_{DMAX} = (T_{Jmax} - T_A) / \theta_{JA}$ . The values for maximum power dissipation will be reached only when the device is operated in a severe fault condition (e.g., when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

**Note 5:** Human body model is 100 pF capacitor discharged through a 1.5 k $\Omega$  resistor. Machine model is 220 pF discharged through ZERO Ohms.

**Note 6:** See the section entitled "Surface Mount" found in any post 1986 National Semiconductor Linear Data Book for methods of soldering surface mount devices.

**Note 7:** The analog inputs are protected as shown below. Input voltage magnitudes up to  $V_A + 300$  mV or to 300 mV below GND will not damage this device. However, errors in the conversion result can occur if any input goes above  $V_A$  or below GND by more than 100 mV. For example, if  $V_A$  is  $2.7V_{DC}$ , ensure that  $-100mV \leq$  input voltages  $\leq 2.8V_{DC}$  to ensure accurate conversions.



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**Note 8:** To guarantee accuracy, it is required that  $V_A$  be well bypassed.

**Note 9:** Typical figures are at  $T_J = 25^\circ C$ , and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

**Note 10:** This parameter is guaranteed by design and/or characterization and is not tested in production.

## Specification Definitions

**DIFFERENTIAL NON-LINEARITY (DNL)** is the measure of the maximum deviation from the ideal step size of 1 LSB, which is  $V_{REF} / 4096 = V_A / 4096$ .

**DIGITAL FEEDTHROUGH** is a measure of the energy injected into the analog output of the DAC from the digital inputs when the DAC outputs are not updated. It is measured with a full-scale code change on the data bus.

**FULL-SCALE ERROR** is the difference between the actual output voltage with a full scale code (FFFh) loaded into the DAC and the value of  $V_A \times 4095 / 4096$ .

**GAIN ERROR** is the deviation from the ideal slope of the transfer function. It can be calculated from Zero and Full-Scale Errors as  $GE = FSE - ZE$ , where GE is Gain error, FSE is Full-Scale Error and ZE is Zero Error.

**GLITCH IMPULSE** is the energy injected into the analog output when the input code to the DAC register changes. It is specified as the area of the glitch in nanovolt-seconds.

**INTEGRAL NON-LINEARITY (INL)** is a measure of the deviation of each individual code from a straight line through the input to output transfer function. The deviation of any given code from this straight line is measured from the center of that code value. The end point method is used. INL for this product is specified over a limited range, per the Electrical Tables.

**LEAST SIGNIFICANT BIT (LSB)** is the bit that has the smallest value or weight of all bits in a word. This value is

$$LSB = V_{REF} / 2^n$$

where  $V_{REF}$  is the supply voltage for this product, and "n" is the DAC resolution in bits, which is 12 for the DAC121S101.

**MAXIMUM LOAD CAPACITANCE** is the maximum capacitance that can be driven by the DAC with output stability maintained.

**MONOTONICITY** is the condition of being monotonic, where the DAC has an output that never decreases when the input code increases.

**MOST SIGNIFICANT BIT (MSB)** is the bit that has the largest value or weight of all bits in a word. Its value is 1/2 of  $V_A$ .

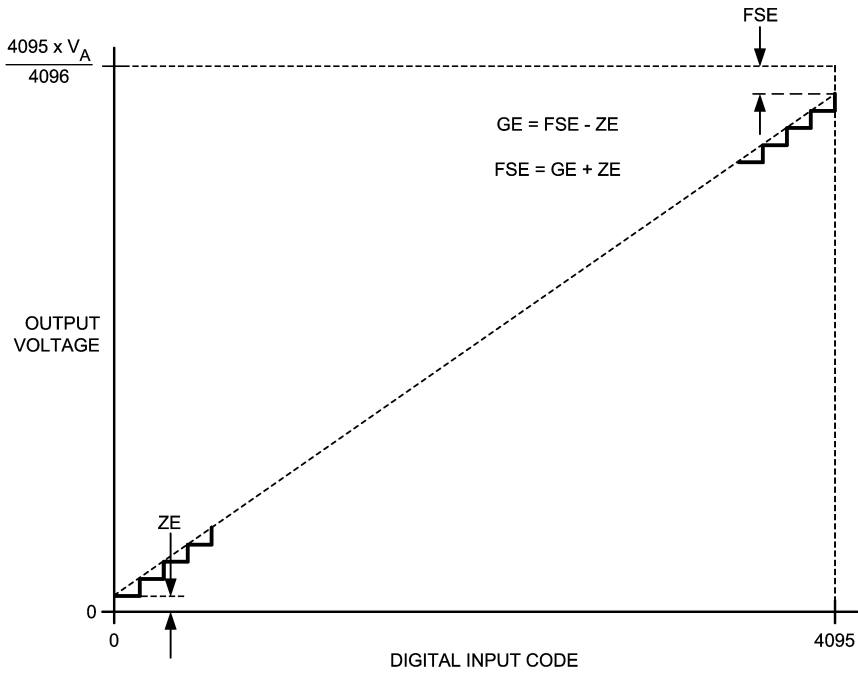
**POWER EFFICIENCY** is the ratio of the output current to the total supply current. The output current comes from the power supply. The difference between the supply and output currents is the power consumed by the device without a load.

**SETTLING TIME** is the time for the output to settle to within 1/2 LSB of the final value after the input code is updated.

**WAKE-UP TIME** is the time for the output to settle to within 1/2 LSB of the final value after the device is commanded to the active mode from any of the power down modes.

**ZERO CODE ERROR** is the output error, or voltage, present at the DAC output after a code of 000h has been entered.

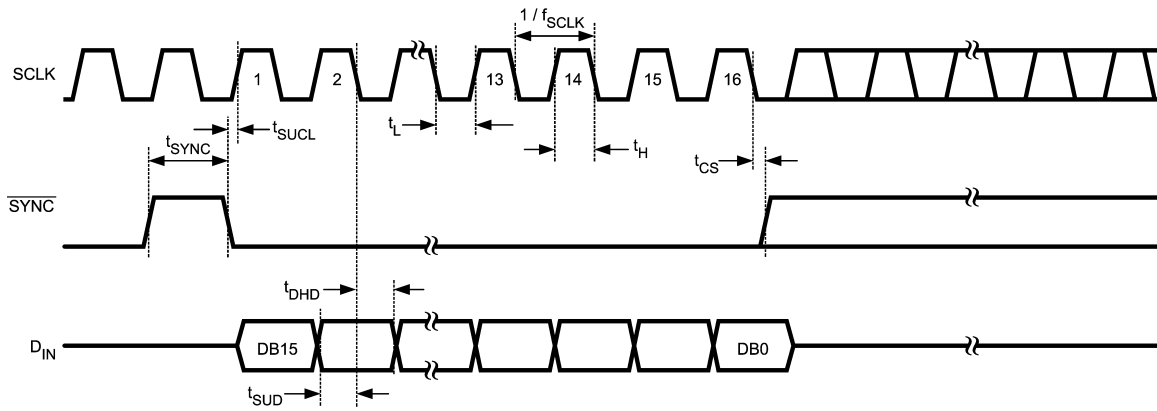
# Transfer Characteristic



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FIGURE 1. Input / Output Transfer Characteristic

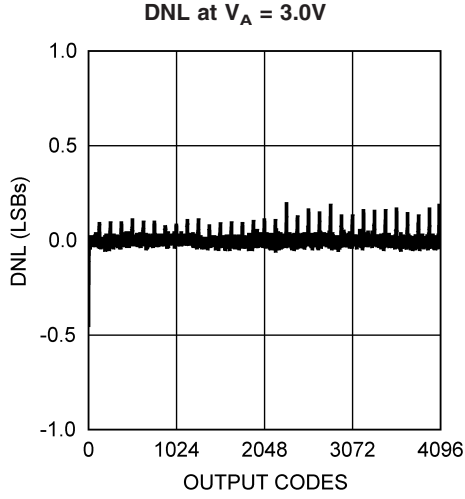
# Timing Diagram



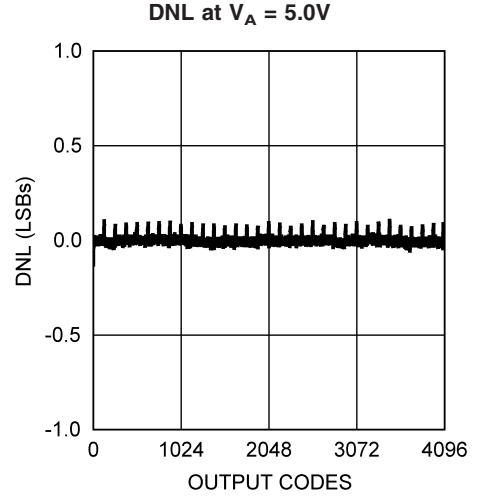
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FIGURE 2. DAC121S101 Timing

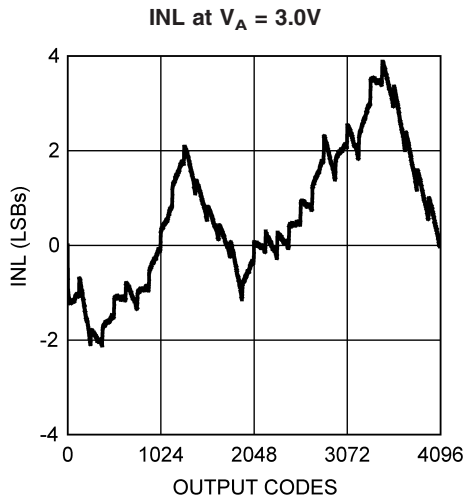
**Typical Performance Characteristics**  $f_{SCLK} = 30 \text{ MHz}$ ,  $T_A = 25^\circ\text{C}$ , Input Code Range 48 to 4047, unless otherwise stated



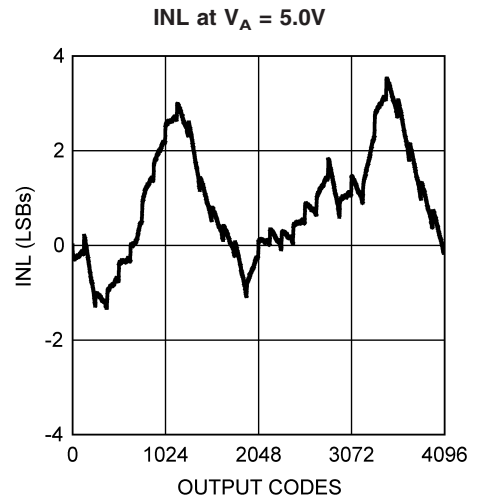
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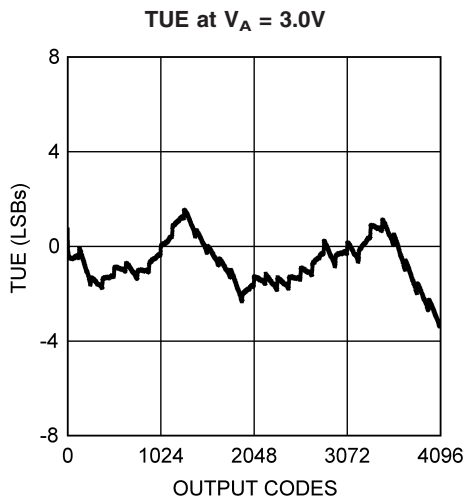
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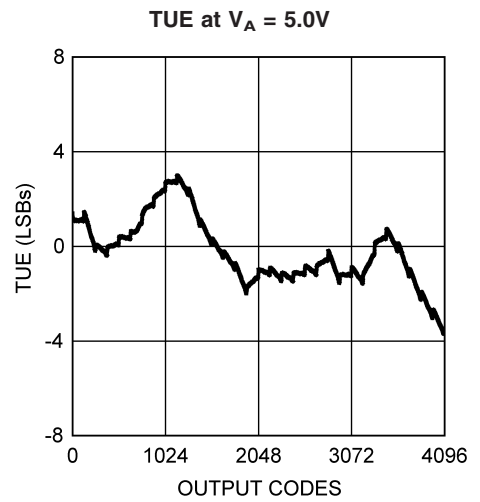
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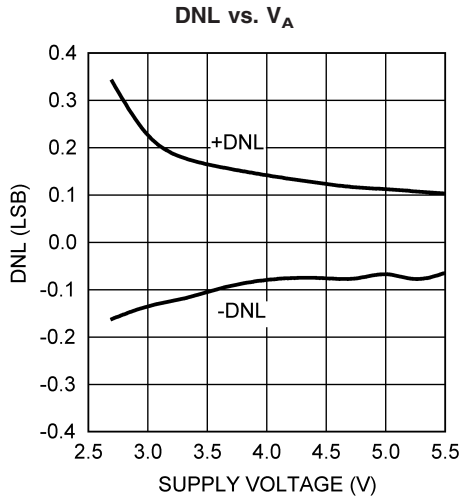
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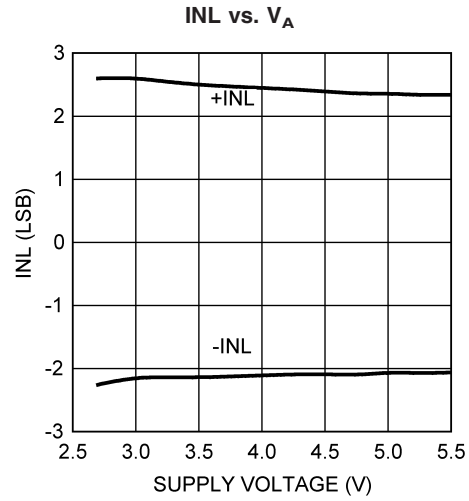
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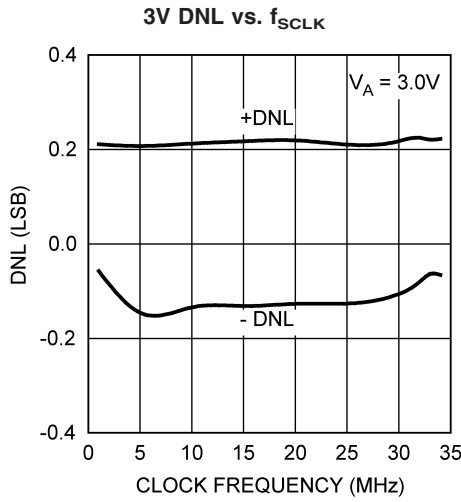
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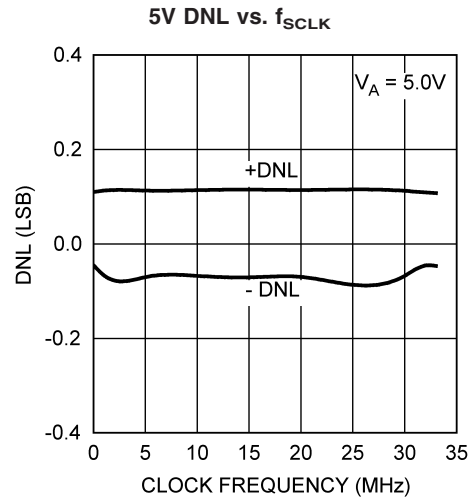
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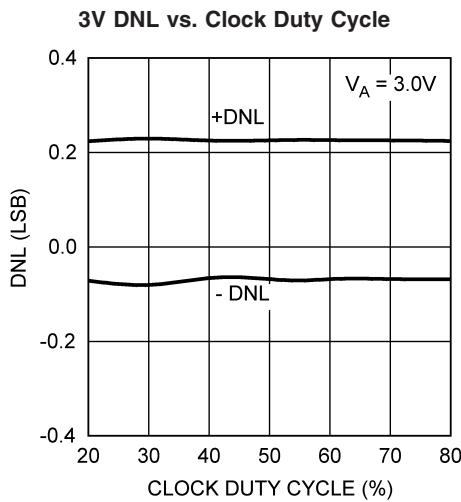
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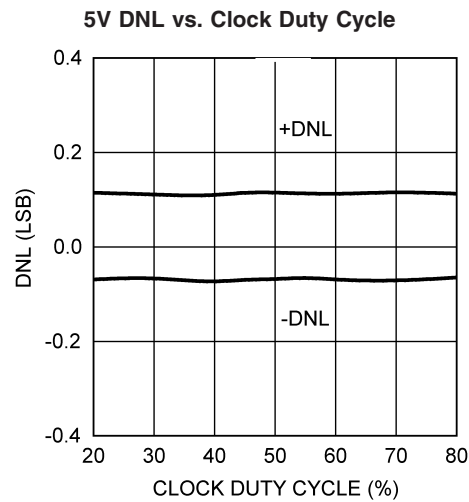
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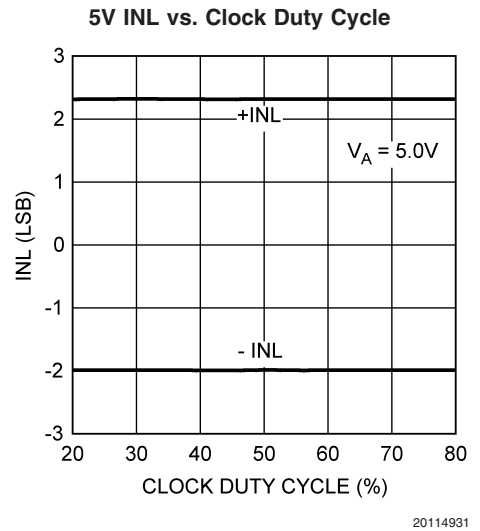
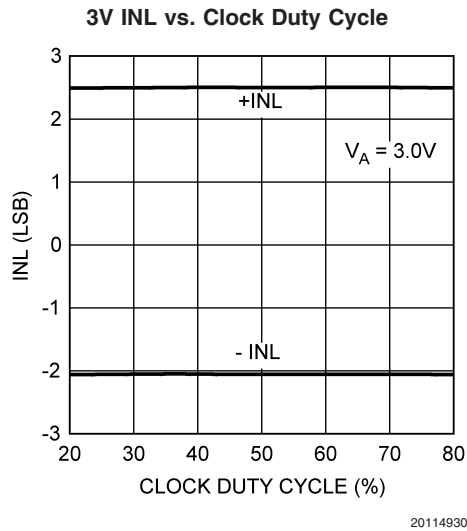
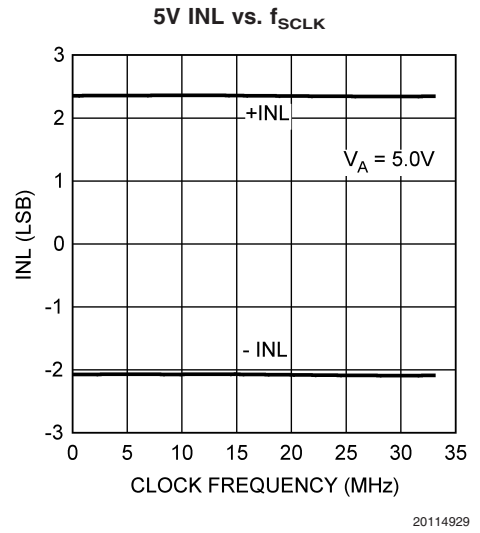
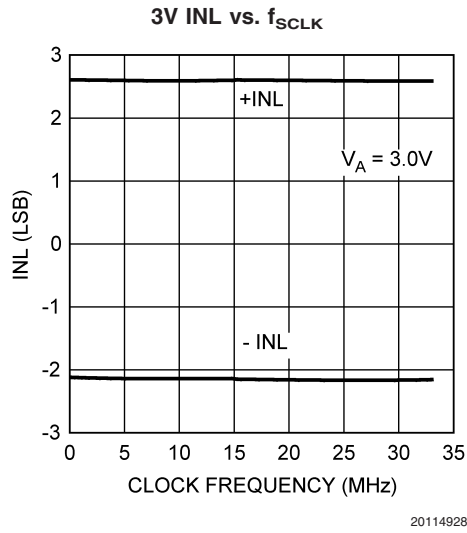
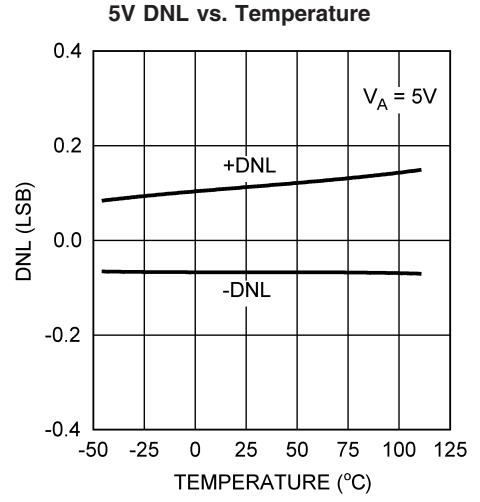
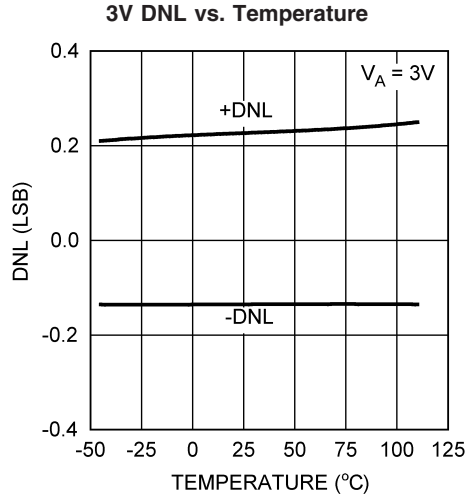


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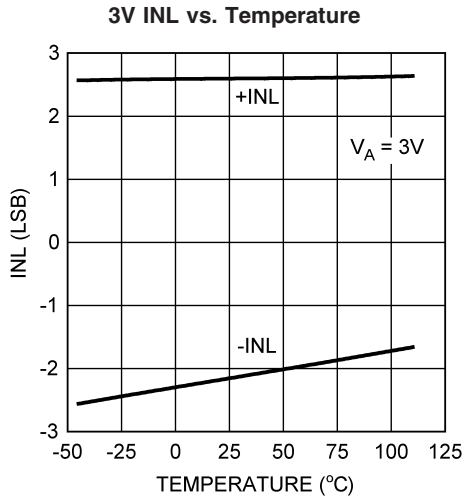


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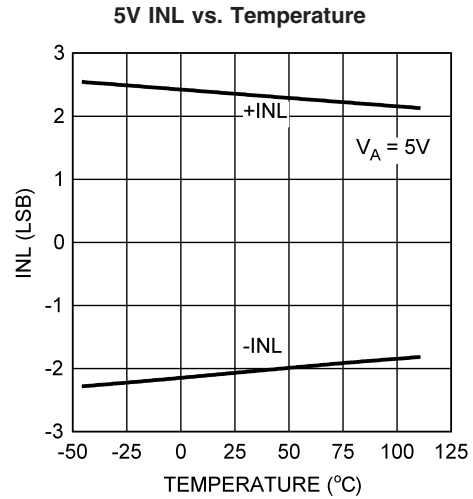
**Typical Performance Characteristics**  $f_{SCLK} = 30 \text{ MHz}$ ,  $T_A = 25^\circ\text{C}$ , Input Code Range 48 to 4047, unless otherwise stated (Continued)



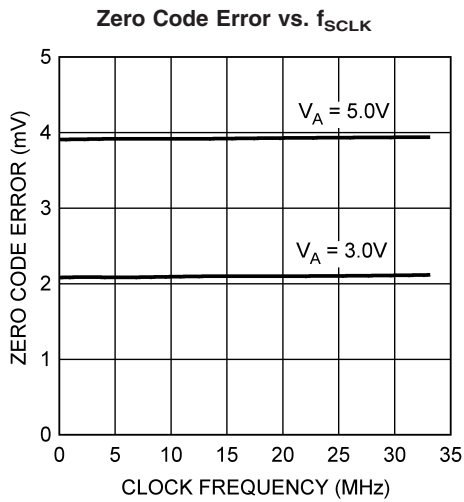
**Typical Performance Characteristics**  $f_{SCLK} = 30 \text{ MHz}$ ,  $T_A = 25^\circ\text{C}$ , Input Code Range 48 to 4047, unless otherwise stated (Continued)



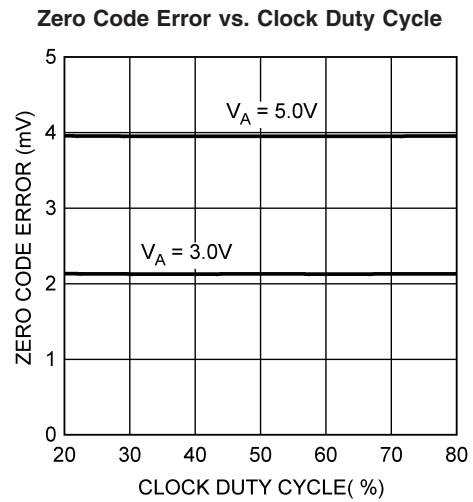
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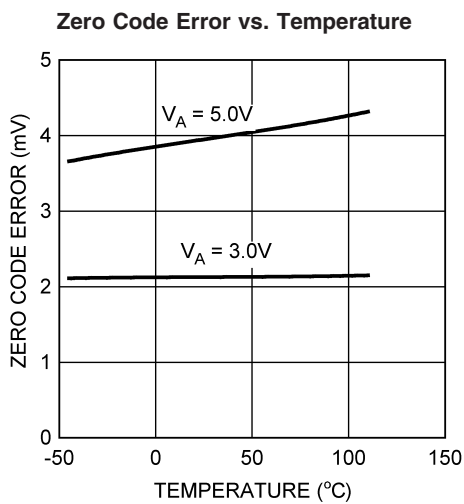
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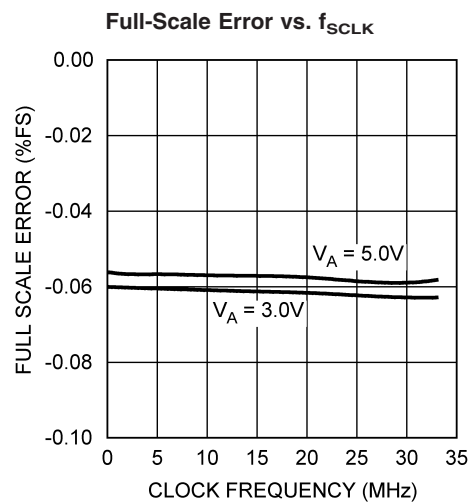
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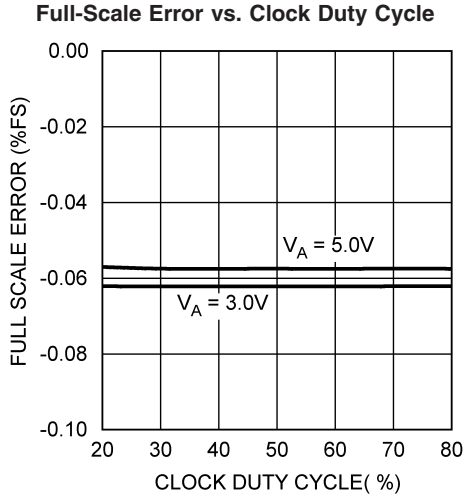


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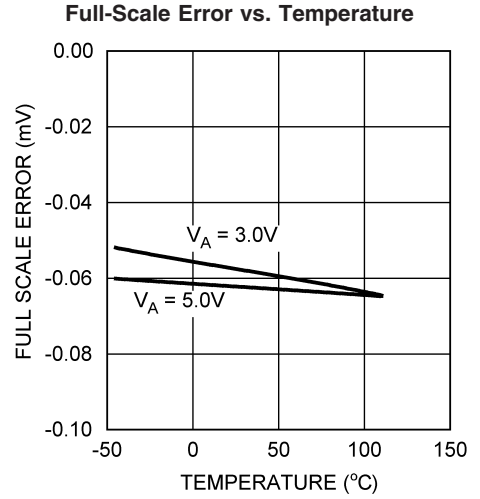


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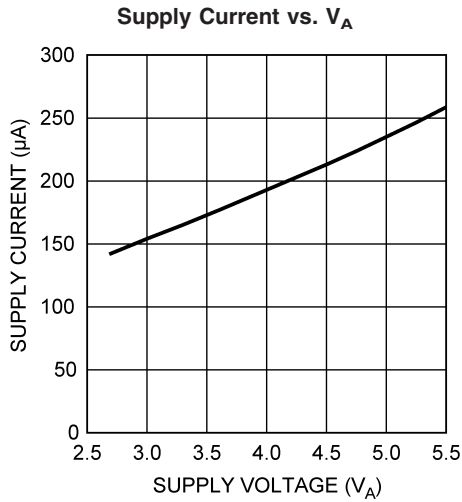
**Typical Performance Characteristics**  $f_{SCLK} = 30 \text{ MHz}$ ,  $T_A = 25^\circ\text{C}$ , Input Code Range 48 to 4047, unless otherwise stated (Continued)



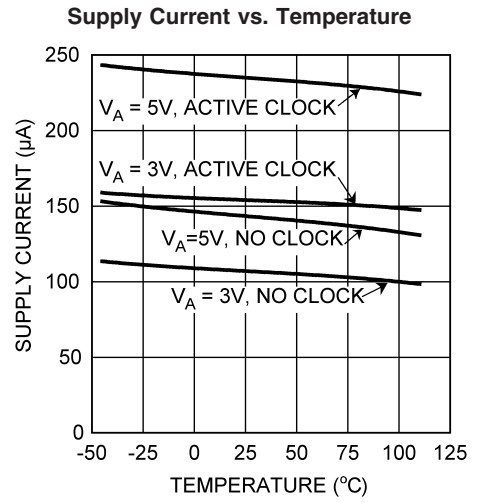
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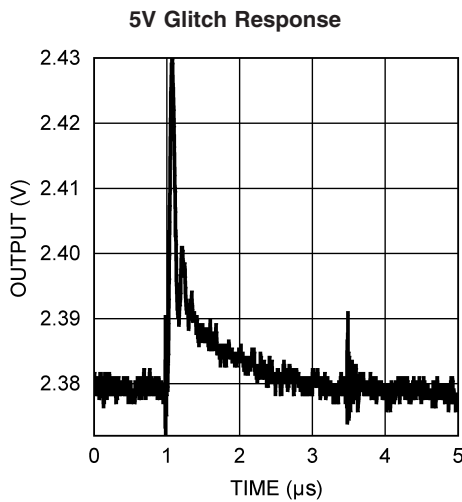
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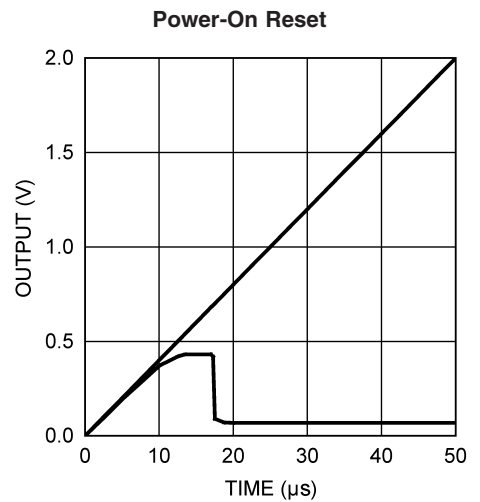
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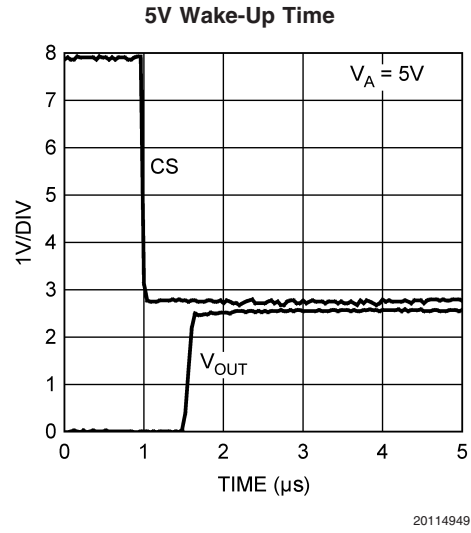
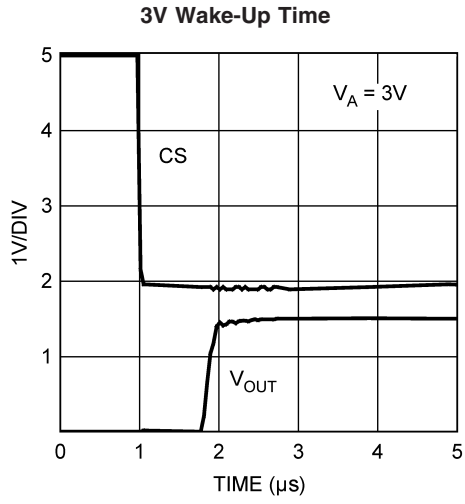


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**Typical Performance Characteristics**  $f_{SCLK} = 30 \text{ MHz}$ ,  $T_A = 25\text{C}$ , Input Code Range 48 to 4047, unless otherwise stated (Continued)



# 1.0 Functional Description

## 1.1 DAC SECTION

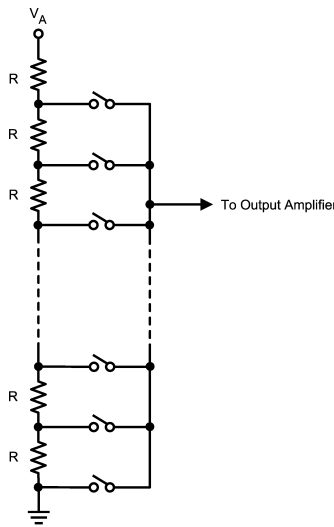
The DAC121S101 is fabricated on a CMOS process with an architecture that consists of switches and a resistor string that are followed by an output buffer. The power supply serves as the reference voltage. The input coding is straight binary with an ideal output voltage of:

$$V_{OUT} = V_A \times (D / 4096)$$

where *D* is the decimal equivalent of the binary code that is loaded into the DAC register and can take on any value between 0 and 4095.

## 1.2 RESISTOR STRING

The resistor string is shown in *Figure 3*. This string consists of 4096 equal valued resistors with a switch at each junction of two resistors, plus a switch to ground. The code loaded into the DAC register determines which switch is closed, connecting the proper node to the amplifier. This configuration guarantees that the DAC is monotonic.



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FIGURE 3. DAC Resistor String

## 1.3 OUTPUT AMPLIFIER

The output buffer amplifier is a rail-to-rail type, providing an output voltage range of 0V to *V<sub>A</sub>*. All amplifiers, even rail-to-rail types, exhibit a loss of linearity as the output approaches the supply rails (0V and *V<sub>A</sub>*, in this case). For this reason, linearity is specified over less than the full output range of the DAC. The output capabilities of the amplifier are described in the Electrical Tables.

## 1.4 SERIAL INTERFACE

The three-wire interface is compatible with SPI, QSPI and MICROWIRE, as well as most DSPs. See the Timing Diagram for information on a write sequence.

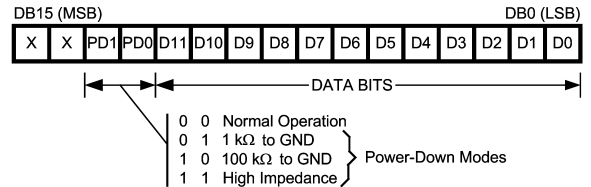
A write sequence begins by bringing the *SYNC* line low. Once *SYNC* is low, the data on the *D<sub>IN</sub>* line is clocked into the 16-bit serial input register on the falling edges of *SCLK*. On the 16th falling clock edge, the last data bit is clocked in and the programmed function (a change in the mode of operation and/or a change in the DAC register contents) is executed. At this point the *SYNC* line may be kept low or

brought high. In either case, it must be brought high for the minimum specified time before the next write sequence as a falling edge of *SYNC* can initiate the next write cycle.

Since the *SYNC* and *D<sub>IN</sub>* buffers draw more current when they are high, they should be idled low between write sequences to minimize power consumption.

## 1.5 INPUT SHIFT REGISTER

The input shift register, *Figure 4*, has sixteen bits. The first two bits are "don't cares" and are followed by two bits that determine the mode of operation (normal mode or one of three power-down modes). The contents of the serial input register are transferred to the DAC register on the sixteenth falling edge of *SCLK*. See Timing Diagram, *Figure 2*.



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FIGURE 4. Input Register Contents

Normally, the *SYNC* line is kept low for at least 16 falling edges of *SCLK* and the DAC is updated on the 16th *SCLK* falling edge. However, if *SYNC* is brought high before the 16th falling edge, the shift register is reset and the write sequence is invalid. The DAC register is not updated and there is no change in the mode of operation or in the output voltage.

## 1.6 POWER-ON RESET

The power-on reset circuit controls the output voltage during power-up. Upon application of power the DAC register is filled with zeros and the output voltage is 0 Volts and remains there until a valid write sequence is made to the DAC.

## 1.7 POWER-DOWN MODES

The DAC121S101 has four modes of operation. These modes are set with two bits (DB13 and DB12) in the control register.

TABLE 1. Modes of Operation

DB13	DB12	Operating Mode
0	0	Normal Operation
0	1	Power-Down with 1kΩ to GND
1	0	Power-Down with 100kΩ to GND
1	1	Power-Down with Hi-Z

When both DB13 and DB12 are 0, the device operates normally. For the other three possible combinations of these bits the supply current drops to its power-down level and the output is pulled down with either a 1kΩ or a 100KΩ resistor, or is in a high impedance state, as described in *Table 1*.

The bias generator, output amplifier, the resistor string and other linear circuitry are all shut down in any of the power-down modes. However, the contents of the DAC register are unaffected when in power-down, so when coming out of power down the output voltage returns to the same voltage it

## 1.0 Functional Description (Continued)

was before entering power down. Minimum power consumption is achieved in the power-down mode with SCLK disabled and SYNC and  $D_{IN}$  idled low.

## 2.0 Applications Information

The simplicity of the DAC121S101 implies ease of use. However, it is important to recognize that any data converter that utilizes its supply voltage as its reference voltage will have essentially zero PSRR (Power Supply Rejection Ratio). Therefore, it is necessary to provide a noise-free supply voltage to the device.

### 2.1 DSP/MICROPROCESSOR INTERFACING

Interfacing the DAC121S101 to microprocessors and DSPs is quite simple. The following guidelines are offered to hasten the design process.

#### 2.1.1 ADSP-2101/ADSP2103 Interfacing

Figure 5 shows a serial interface between the DAC121S101 and the ADSP-2101/ADSP2103. The DSP should be set to operate in the SPORT Transmit Alternate Framing Mode. It is programmed through the SPORT control register and should be configured for Internal Clock Operation, Active Low Framing and 16-bit Word Length. Transmission is started by writing a word to the Tx register after the SPORT mode has been enabled.

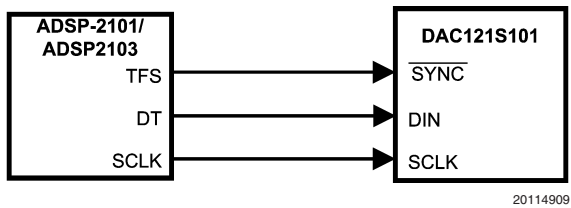


FIGURE 5. ADSP-2101/2103 Interface

#### 2.1.2 80C51/80L51 Interface

A serial interface between the DAC121S101 and the 80C51/80L51 microcontroller is shown in Figure 6. The SYNC signal comes from a bit-programmable pin on the microcontroller. The example shown here uses port line P3.3. This line is taken low when data is to be transmitted to the DAC121S101. Since the 80C51/80L51 transmits 8-bit bytes, only eight falling clock edges occur in the transmit cycle. To load data into the DAC, the P3.3 line must be left low after the first eight bits are transmitted. A second write cycle is initiated to transmit the second byte of data, after which port line P3.3 is brought high. The 80C51/80L51 transmit routine must recognize that the 80C51/80L51 transmits data with the LSB first while the DAC121S101 requires data with the MSB first.

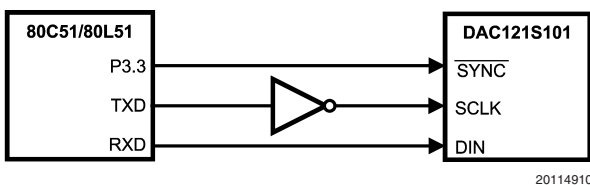


FIGURE 6. 80C51/80L51 Interface

#### 2.1.3 68HC11 Interface

A serial interface between the DAC121S101 and the 68HC11 microcontroller is shown in Figure 7. The SYNC line of the DAC121S101 is driven from a port line (PC7 in the figure), similar to the 80C51/80L51.

The 68HC11 should be configured with its CPOL bit as a zero and its CPHA bit as a one. This configuration causes data on the MOSI output to be valid on the falling edge of SCLK. PC7 is taken low to transmit data to the DAC. The 68HC11 transmits data in 8-bit bytes with eight falling clock edges. Data is transmitted with the MSB first. PC7 must remain low after the first eight bits are transferred. A second write cycle is initiated to transmit the second byte of data to the DAC, after which PC7 should be raised to end the write sequence.

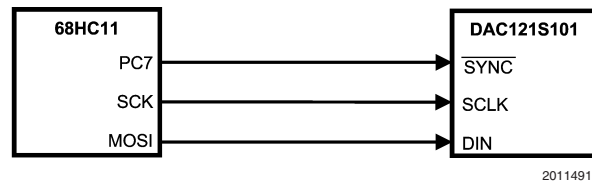


FIGURE 7. 68HC11 Interface

#### 2.1.4 Microwire Interface

Figure 8 shows an interface between a Microwire compatible device and the DAC121S101. Data is clocked out on the rising edges of the SCLK signal.

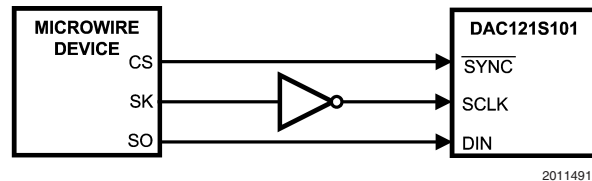


FIGURE 8. Microwire Interface

## 2.2 USING REFERENCES AS POWER SUPPLIES

Recall the need for a quiet supply source for devices that use their power supply voltage as a reference voltage.

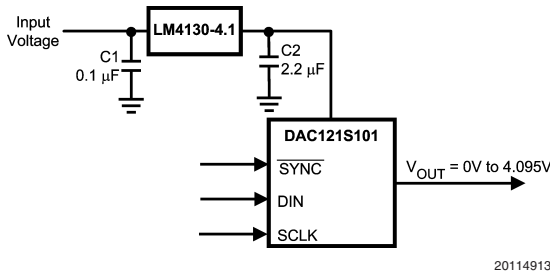
Since the DAC121S101 consumes very little power, a reference source may be used as the supply voltage. The advantages of using a reference source over a voltage regulator are accuracy and stability. Some low noise regulators can also be used for the power supply of the DAC121S101. Listed below are a few power supply options for the DAC121S101.

### 2.2.1 LM4130

The LM4130 reference, with its 0.05% accuracy over temperature, is a good choice as a power source for the DAC121S101. Its primary disadvantage is the lack of 3V and 5V versions. However, the 4.096V version is useful if a 0 to 4.095V output range is desirable or acceptable. Bypassing the LM4130 VIN pin with a 0.1μF capacitor and the VOUT pin with a 2.2μF capacitor will improve stability and reduce output noise. The LM4130 comes in a space-saving 5-pin SOT23.

## 2.0 Applications Information

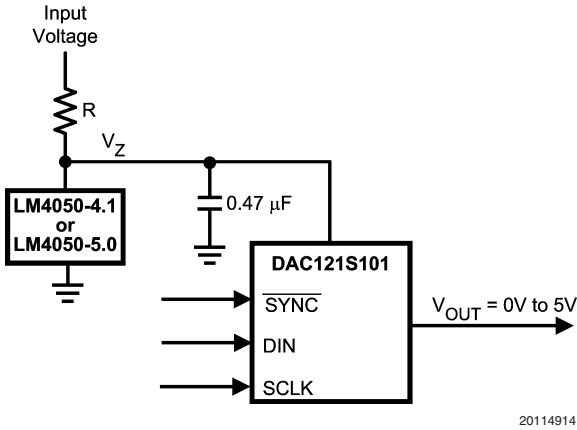
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**FIGURE 9. The LM4130 as a power supply**

### 2.2.2 LM4050

Available with accuracy of 0.44%, the LM4050 shunt reference is also a good choice as a power regulator for the DAC121S101. It does not come in a 3 Volt version, but 4.096V and 5V versions are available. It comes in a space-saving 3-pin SOT23.



**FIGURE 10. The LM4050 as a power supply**

The minimum resistor value in the circuit of *Figure 10* should be chosen such that the maximum current through the LM4050 does not exceed its 15 mA rating. The conditions for maximum current include the input voltage at its maximum, the LM4050 voltage at its minimum, the resistor value at its minimum due to tolerance, and the DAC121S101 draws zero current. The maximum resistor value must allow the LM4050 to draw more than its minimum current for regulation plus the maximum DAC121S101 current in full operation. The conditions for minimum current include the input voltage at its minimum, the LM4050 voltage at its maximum, the resistor value at its maximum due to tolerance, and the DAC121S101 draws its maximum current. These conditions can be summarized as

$$R(\min) = (V_{IN}(\max) - V_Z(\min)) / (I_A(\min) + I_Z(\max))$$

and

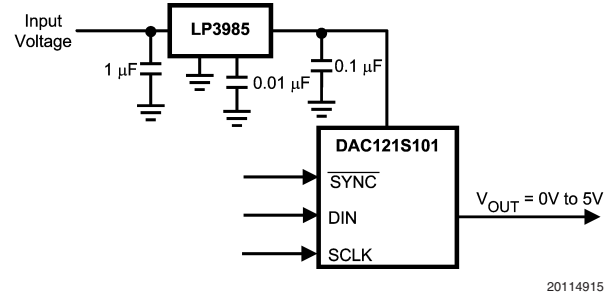
$$R(\max) = (V_{IN}(\min) - V_Z(\max)) / (I_A(\max) + I_Z(\min))$$

where  $V_Z(\min)$  and  $V_Z(\max)$  are the nominal LM4050 output voltages  $\pm$  the LM4050 output tolerance over temperature,  $I_Z(\max)$  is the maximum allowable current through the LM4050,  $I_Z(\min)$  is the minimum current required by the

LM4050 for proper regulation,  $I_A(\max)$  is the maximum DAC121S101 supply current, and  $I_A(\min)$  is the minimum DAC121S101 supply current.

### 2.2.3 LP3985

The LP3985 is a low noise, ultra low dropout voltage regulator with a 3% accuracy over temperature. It is a good choice for applications that do not require a precision reference for the DAC121S101. It comes in 3.0V, 3.3V and 5V versions, among others, and sports a low 30  $\mu$ V noise specification at low frequencies. Since low frequency noise is relatively difficult to filter, this specification could be important for some applications. The LP3985 comes in a space-saving 5-pin SOT23 and 5-bump micro SMD packages.

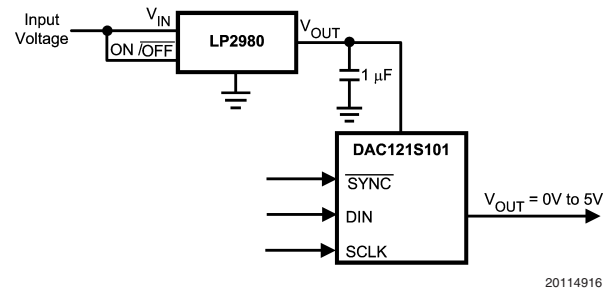


**FIGURE 11. Using the LP3985 regulator**

An input capacitance of 1.0 $\mu$ F without any ESR requirement is required at the LP3985 input, while a 1.0 $\mu$ F ceramic capacitor with an ESR requirement of 5m $\Omega$  to 500m $\Omega$  is required at the output. Careful interpretation and understanding of the capacitor specification is required to ensure correct device operation.

### 2.2.4 LP2980

The LP2980 is an ultra low dropout regulator with a 0.5% or 1.0% accuracy over temperature, depending upon grade. It is available in 3.0V, 3.3V and 5V versions, among others.



**FIGURE 12. Using the LP2980 regulator**

Like any low dropout regulator, the LP2980 requires an output capacitor for loop stability. This output capacitor must be at least 1.0 $\mu$ F over temperature, but values of 2.2 $\mu$ F or more will provide even better performance. The ESR of this capacitor should be within the range specified in the LP2980 data sheet. Surface-mount solid tantalum capacitors offer a good combination of small size and ESR. Ceramic capacitors are attractive due to their small size but generally have ESR values that are too low for use with the LP2980. Alumi-



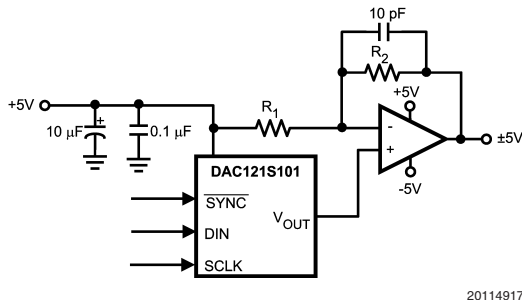
## 2.0 Applications Information

(Continued)

num electrolytic capacitors are typically not a good choice due to their large size and have ESR values that may be too high at low temperatures.

### 2.3 BIPOLAR OPERATION

The DAC121S101 is designed for single supply operation and thus has a unipolar output. However, a bipolar output may be obtained with the circuit in *Figure 13*. This circuit will provide an output voltage range of  $\pm 5$  Volts. A rail-to-rail amplifier should be used if the amplifier supplies are limited to  $\pm 5$ V.



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**FIGURE 13. Bipolar Operation**

The output voltage of this circuit for any code is found to be

$$V_O = (V_A \times (D / 4096) \times ((R1 + R2) / R1) - V_A \times R2 / R1)$$

where D is the input code in decimal form. With  $V_A = 5$ V and  $R1 = R2$ ,

$$V_O = (10 \times D / 4096) - 5$$

A list of rail-to-rail amplifiers suitable for this application are indicated in *Table 2*.

**TABLE 2. Some Rail-to-Rail Amplifiers**

AMP	PKGS	Typ $V_{OS}$	Typ $I_{SUPPLY}$
LMC7111	DIP-8 SOT23-5	0.9 mV	25 $\mu$ A
LM7301	SO-8 SOT23-5	0.03 mV	620 $\mu$ A
LM8261	SOT23-5	0.7 mV	1 mA

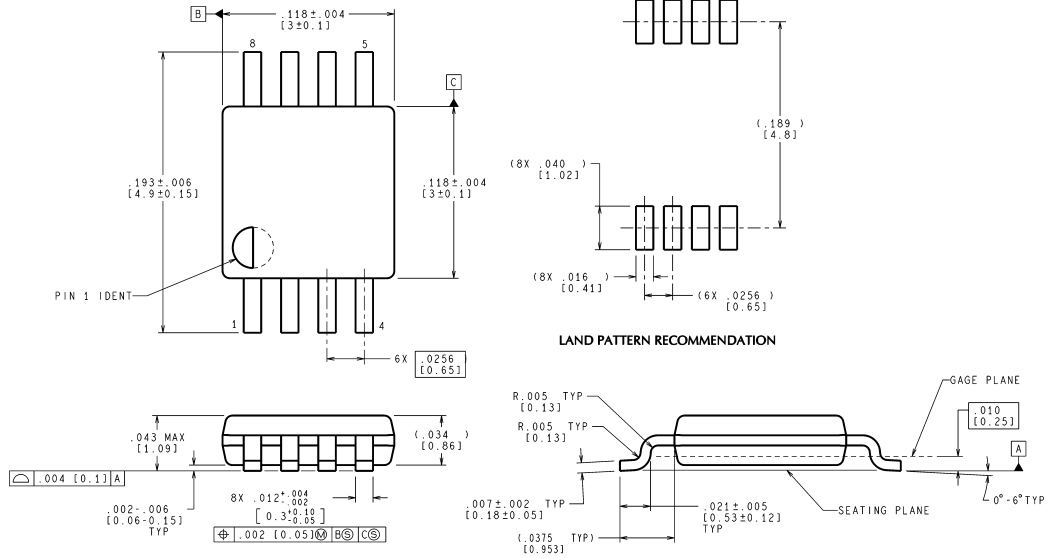
### 2.4 LAYOUT, GROUNDING, AND BYPASSING

For best accuracy and minimum noise, the printed circuit board containing the DAC121S101 should have separate analog and digital areas. The areas are defined by the locations of the analog and digital power planes. Both of these planes should be located in the same board layer. There should be a single ground plane. A single ground plane is preferred if digital return current does not flow through the analog ground area. Frequently a single ground plane design will utilize a "fencing" technique to prevent the mixing of analog and digital ground current. Separate ground planes should only be utilized when the fencing technique is inadequate. The separate ground planes must be connected in one place, preferably near the DAC121S101. Special care is required to guarantee that digital signals with fast edge rates do not pass over split ground planes. They must always have a continuous return path below their traces.

The DAC121S101 power supply should be bypassed with a 10 $\mu$ F and a 0.1 $\mu$ F capacitor as close as possible to the device with the 0.1 $\mu$ F right at the device supply pin. The 10 $\mu$ F capacitor should be a tantalum type and the 0.1 $\mu$ F capacitor should be a low ESL, low ESR type. The power supply for the DAC121S101 should only be used for analog circuits.

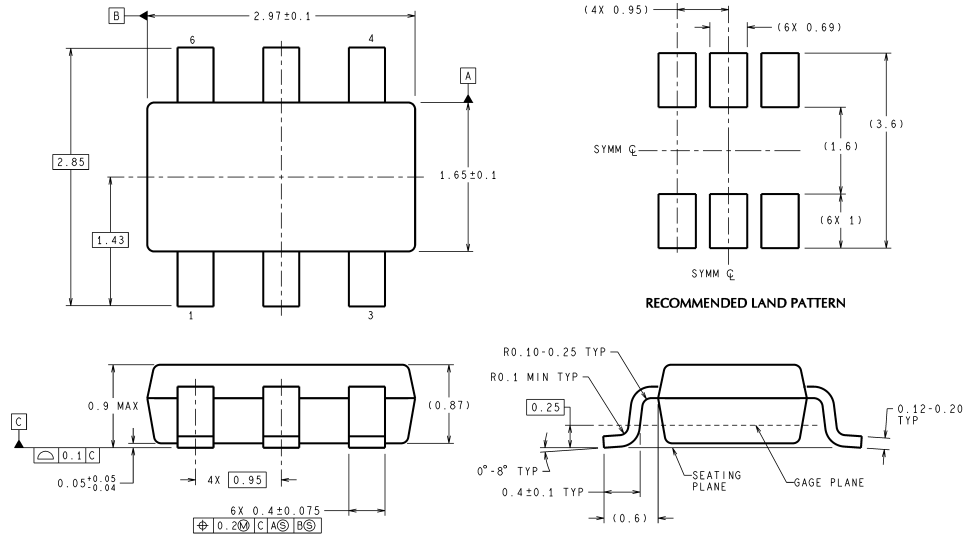
Avoid crossover of analog and digital signals and keep the clock and data lines on the component side of the board. The clock and data lines should have controlled impedances.

**Physical Dimensions** inches (millimeters)  
unless otherwise noted



**8-Lead MSOP**  
Order Numbers DAC121S101CIMM  
NS Package Number MUA08A

MUA08A (Rev E)



**6-Lead TSOT**  
Order Numbers DAC121S101CIMK  
NS Package Number MK06A

MK06A (Rev C)

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