



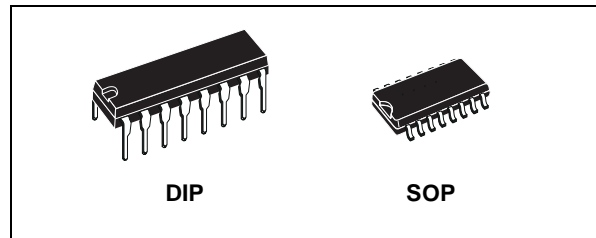
# HCF4094B

## 8 STAGE SHIFT AND STORE BUS REGISTER WITH 3-STATE OUTPUTS

- 3- STATE PARALLEL OUTPUTS FOR CONNECTION TO COMMON BUS
- SEPARATE SERIAL OUTPUTS SYNCHRONOUS TO BOTH POSITIVE AND NEGATIVE CLOCK EDGES FOR CASCADING
- MEDIUM SPEED OPERATION 5MHz at 10V
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT  
 $I_l = 100\text{nA}$  (MAX) AT  $V_{DD} = 18\text{V}$   $T_A = 25^\circ\text{C}$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"

### DESCRIPTION

The HCF4094B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. The HCF4094B is an 8 stages serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data

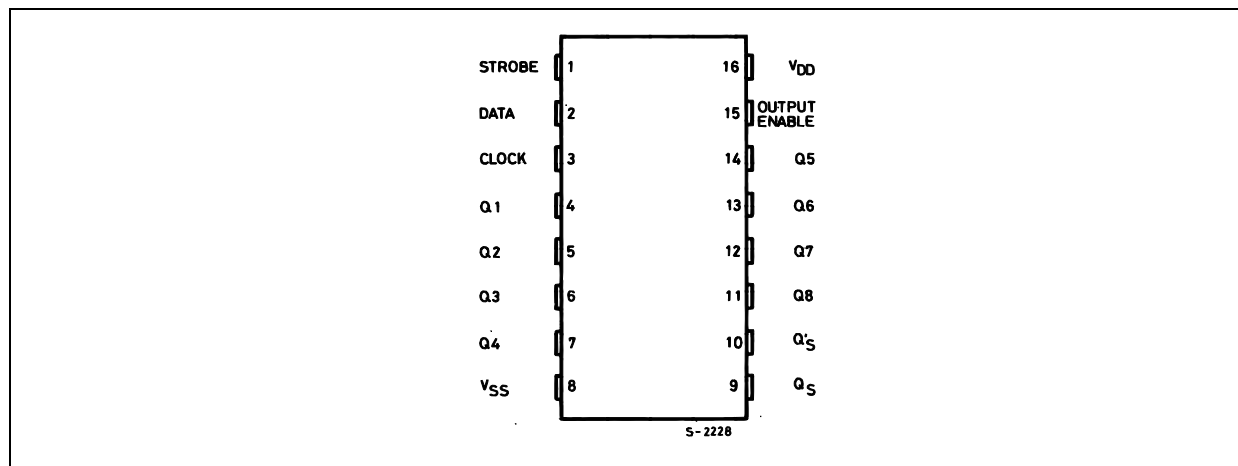


### ORDER CODES

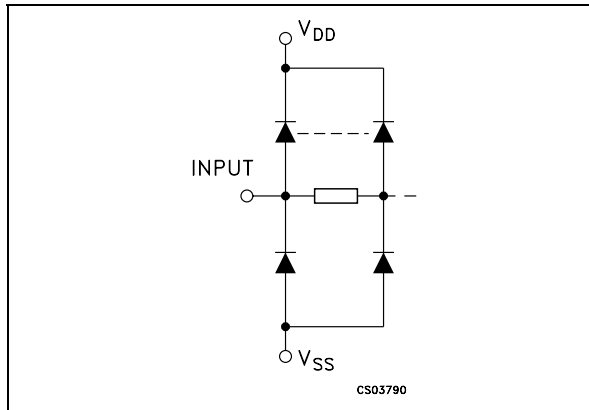
PACKAGE	TUBE	T & R
DIP	HCF4094BEY	
SOP	HCF4094BM1	HCF4094M013TR

is shifted on positive clock transition. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high. Two serial outputs are available for cascading a number of HCF4094B devices. Data is available at the  $Q_S$  serial output terminal on positive clock edges to allow for high speed operation in cascaded system in which the clock rise time is fast. The same serial information, available at the  $Q'_S$  terminal on the next negative clock edge, provides a means for cascading HCF4094B devices when the clock rise time is slow.

### PIN CONNECTION



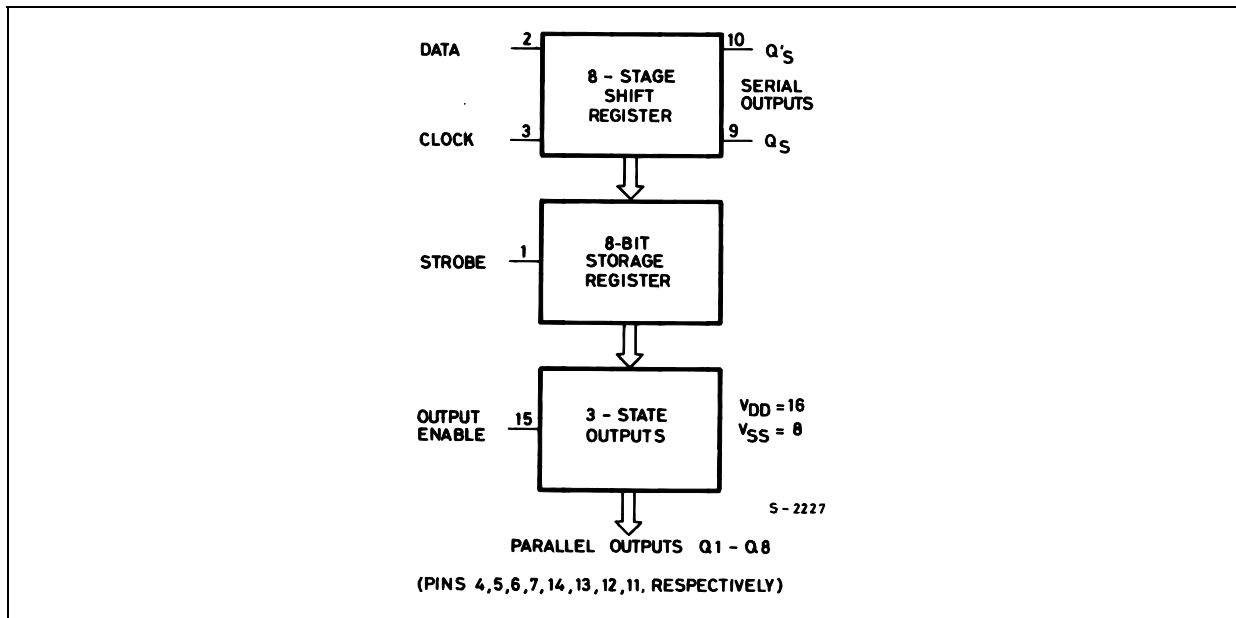
**IINPUT EQUIVALENT CIRCUIT**



**PIN DESCRIPTION**

PIN No	SYMBOL	NAME AND FUNCTION
2	DATA	Data Input
1	STROBE	Strobe Input
3	CLOCK	Clock Input
9, 10	Q <sub>S</sub> , Q' <sub>S</sub>	Serial Outputs
4, 5, 6, 7, 14, 13, 12, 11	Q1 to Q8	Parallel Outputs
15	OUTPUT ENABLE	Output Enable Input
8	V <sub>SS</sub>	Negative Supply Voltage
16	V <sub>DD</sub>	Positive Supply Voltage

**FUNCTIONAL DIAGRAM**



**TRUTH TABLE**

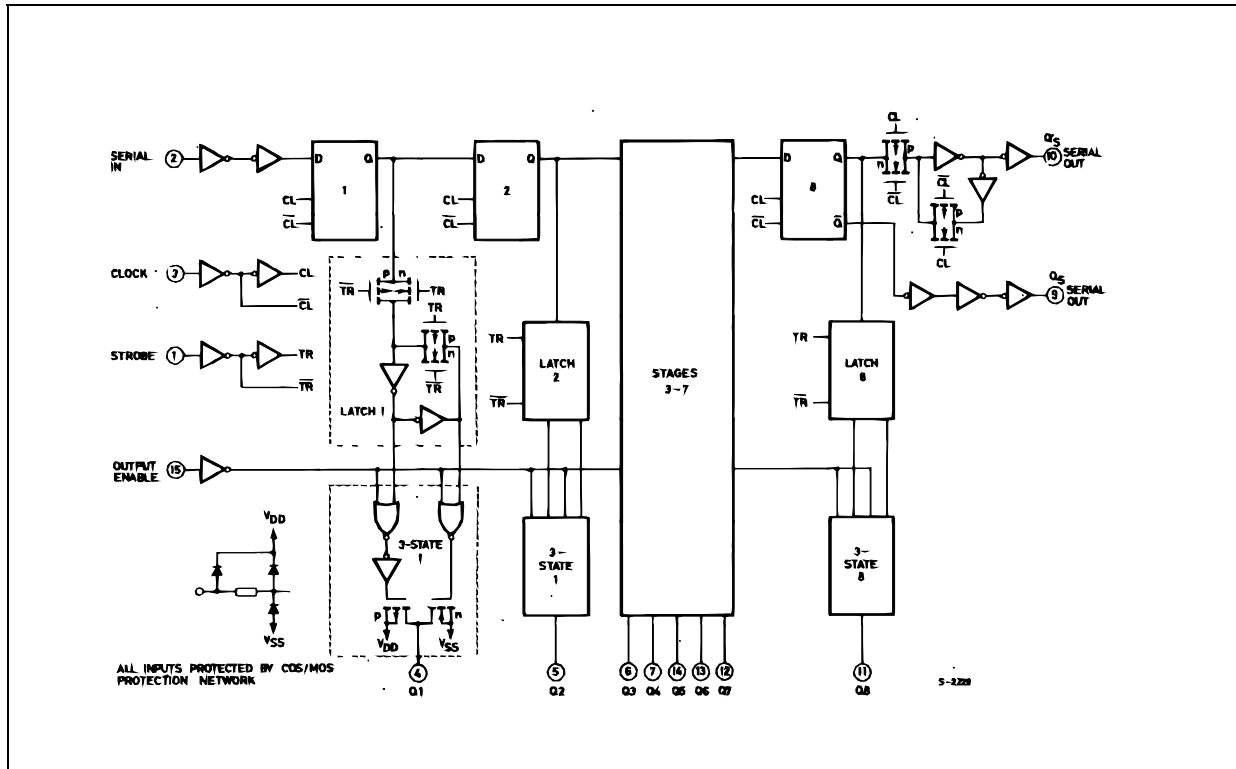
CLOCK	OUTPUTS ENABLE	STROBE	DATA	PARALLEL OUTPUTS		SERIAL OUTPUTS	
				Q <sub>1</sub>	Q <sub>n</sub>	Q* <sub>S</sub>	Q' <sub>S</sub>
	L	X	X	OC	OC	Q7	No Change
	L	X	X	OC	OC	No Change	Q7
	H	L	X	No Change	No Change	Q7	No Change
	H	H	L	L	Q <sub>n</sub> - 1	Q7	No Change
	H	H	H	H	Q <sub>n</sub> - 1	Q7	No Change
	H	H	H	No Change	No Change	No Change	Q7

X : Don't Care

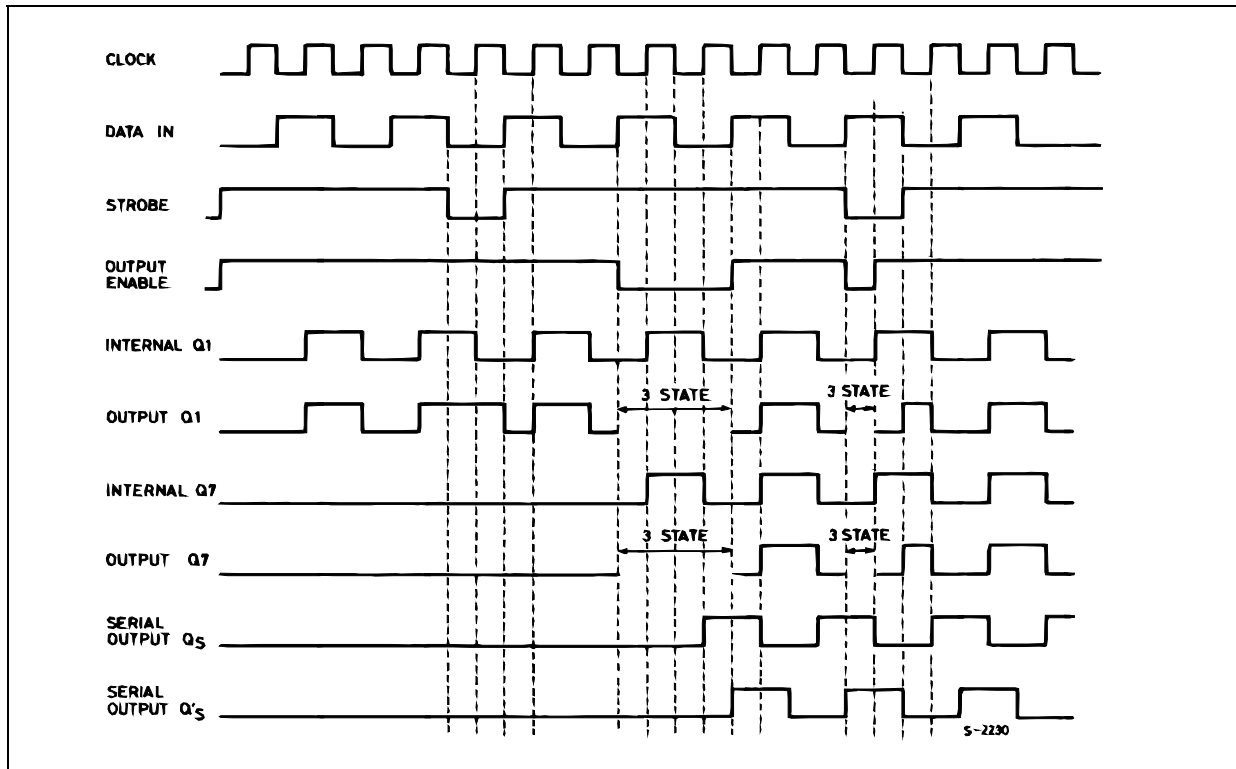
OC : Open Circuit

\* At the positive clock edge information on the 7th shift register stage is transferred to the 8th register stage and the Q<sub>S</sub> output.

LOGIC DIAGRAM



TIMING CHART



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	-0.5 to +22	V
$V_I$	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
$I_I$	DC Input Current	$\pm 10$	mA
$P_D$	Power Dissipation per Package	500 (*)	mW
	Power Dissipation per Output Transistor	100	mW
$T_{op}$	Operating Temperature	-55 to +125	°C
$T_{stg}$	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to  $V_{SS}$  pin voltage.

(\*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	3 to 20	V
$V_I$	Input Voltage	0 to $V_{DD}$	V
$T_{op}$	Operating Temperature	-55 to 125	°C

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value						Unit	
		V <sub>I</sub> (V)	V <sub>O</sub> (V)	I <sub>OL</sub>   ( $\mu$ A)	V <sub>DD</sub> (V)	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.		Max.
I <sub>L</sub>	Quiescent Current	0/5			5		0.04	5		150		150	$\mu$ A
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V <sub>OH</sub>	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V <sub>OL</sub>	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V <sub>IH</sub>	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V <sub>IL</sub>	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I <sub>OH</sub>	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I <sub>OL</sub>	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I <sub>I</sub>	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu$ A
I <sub>OH</sub> , I <sub>OL</sub>	3-State Output Leakage Current	0/18	0/18		18		$\pm 10^{-4}$	$\pm 0.4$		$\pm 12$		$\pm 12$	$\mu$ A
C <sub>I</sub>	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V<sub>DD</sub>=5V, 2V min. with V<sub>DD</sub>=10V, 2.5V min. with V<sub>DD</sub>=15V

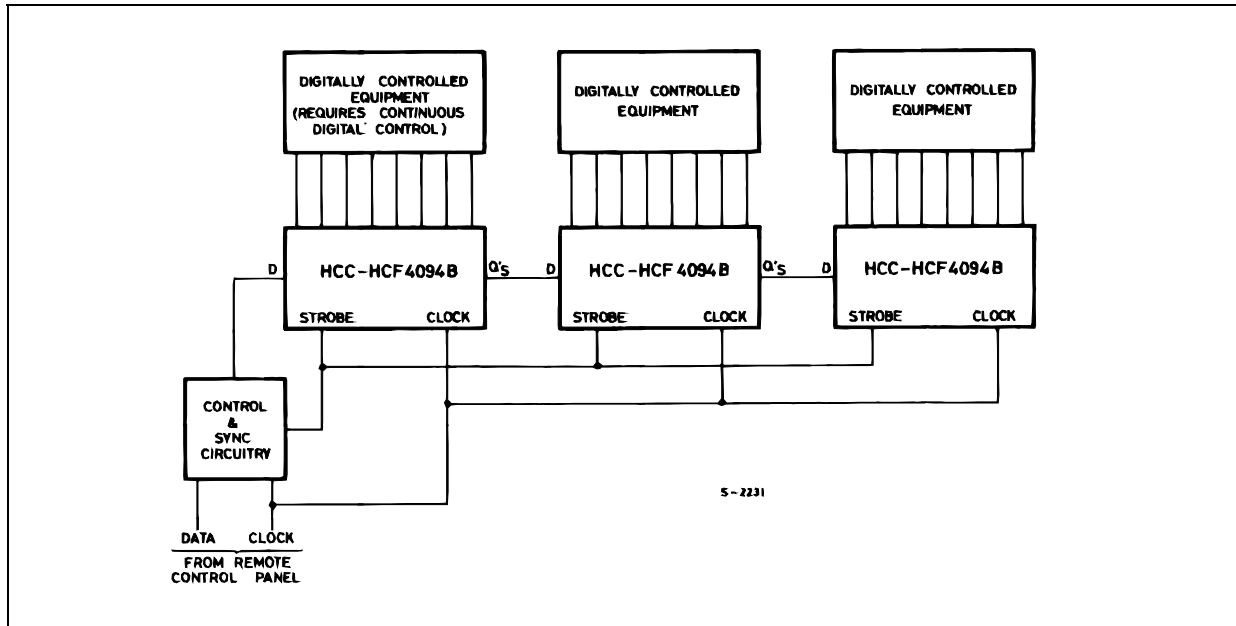
## HCF4094B

### DYNAMIC ELECTRICAL CHARACTERISTICS ( $T_{amb} = 25^{\circ}\text{C}$ , $C_L = 50\text{pF}$ , $R_L = 200\text{K}\Omega$ , $t_r = t_f = 20\text{ ns}$ )

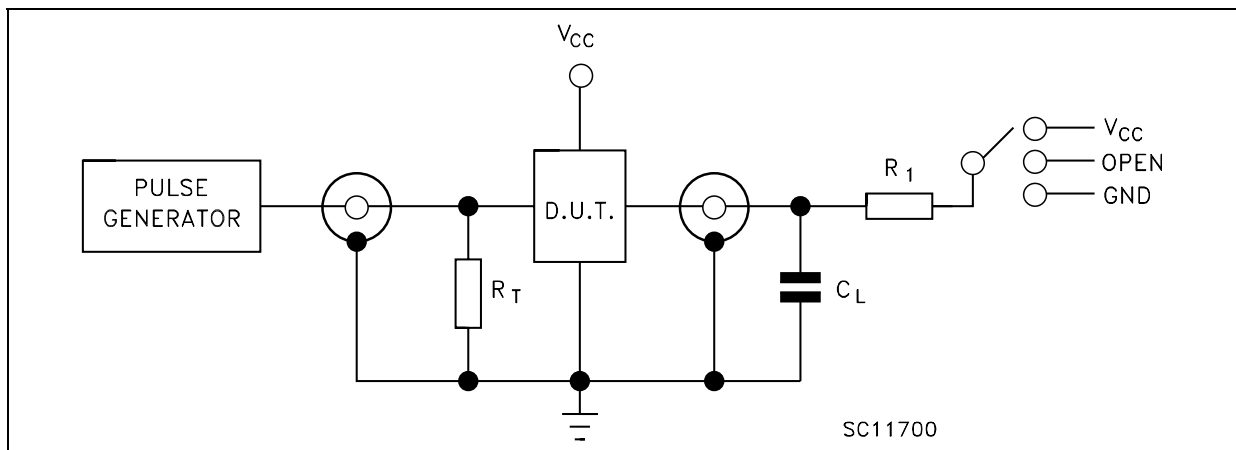
Symbol	Parameter	Test Condition		Value (*)			Unit
		$V_{DD}$ (V)		Min.	Typ.	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (Clock to serial Output $Q_S$ )	5			300	600	ns
		10			125	250	
		15			95	190	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (Clock to serial Output $Q'_S$ )	5			230	460	ns
		10			110	220	
		15			75	150	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (Clock to Parallel Output)	5			420	840	ns
		10			195	390	
		15			135	270	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (Strobe to Parallel Output)	5			290	580	ns
		10			145	290	
		15			100	200	
$t_{PZL}$ $t_{PZH}$	Propagation Delay Time Output Enable to Parallel Out : Output High to High Impedance	5			140	280	ns
		10			75	150	
		15			55	110	
$t_{PHZ}$ $t_{PLZ}$	Propagation Delay Time Output Enable to Parallel Out : Output Low to High Impedance	5			225	450	ns
		10			95	190	
		15			70	140	
$t_W$	Strobe Pulse Width	5		200	100		ns
		10		80	40		
		15		70	35		
$t_W$	Clock Pulse Width	5		200	100		ns
		10		100	50		
		15		83	40		
$t_{setup}$	Data Setup Time	5		125	60		ns
		10		55	30		
		15		35	20		
$t_{hold}$	Minimum Hold Time	5		0	0	0	ns
		10		0	0	0	
		15		0	0	0	
$t_{TLH}$ $t_{THL}$	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
$t_r$ $t_f$	Clock input Rise or Fall Time	5		15			$\mu\text{s}$
		10		5			
		15		5			
$f_{max}$	Maximum Clock Input Frequency	5		1.25	2.5		MHz
		10		2.5	5		
		15		3	6		

(\*) Typical temperature coefficient for all  $V_{DD}$  value is 0.3 %/°C.

**TYPICAL APPLICATION (REMOTE CONTROL HOLDING REGISTER)**



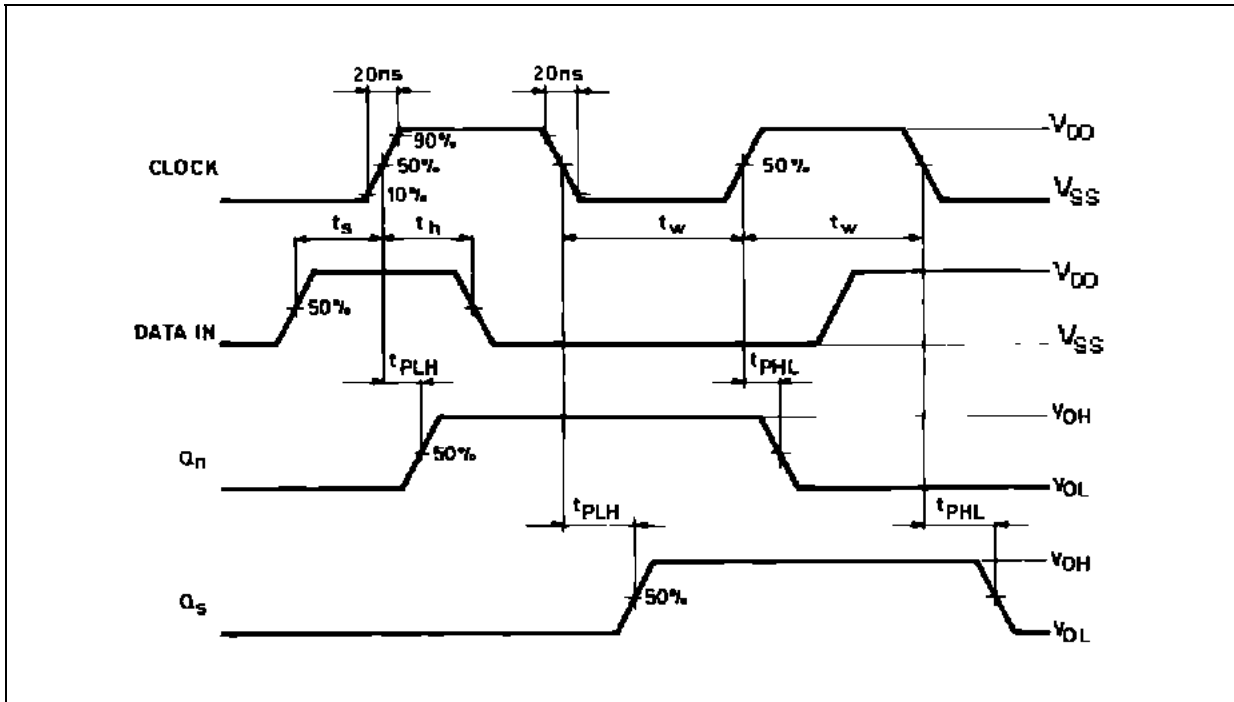
**TEST CIRCUIT**



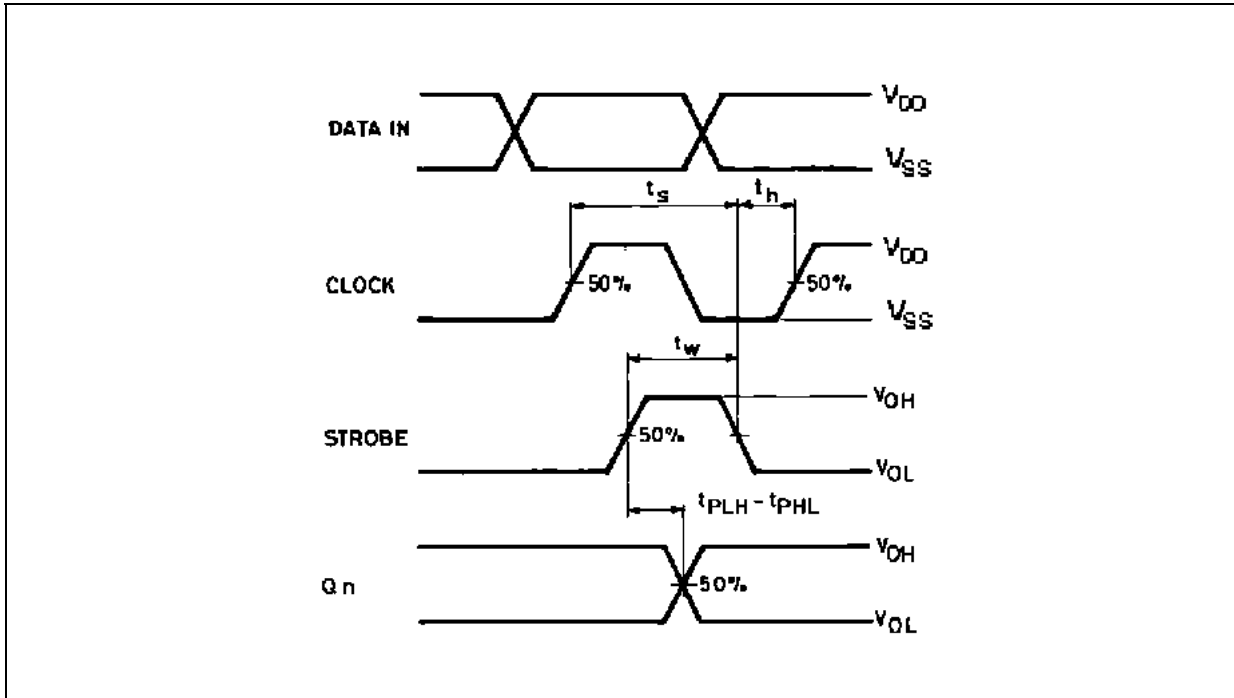
TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	$V_{CC}$
$t_{PZH}$ , $t_{PHZ}$	GND

$C_L$  = 50pF or equivalent (includes jig and probe capacitance)  
 $R_L$  = 200K $\Omega$   
 $R_T$  =  $Z_{OUT}$  of pulse generator (typically 50 $\Omega$ )

**WAVEFORM 1 : PROPAGATION DELAY TIMES, PULSE WIDTH (CLOCK), SETUP AND HOLD TIME (DATA IN TO CLOCK) (f=1MHz; 50% duty cycle)**

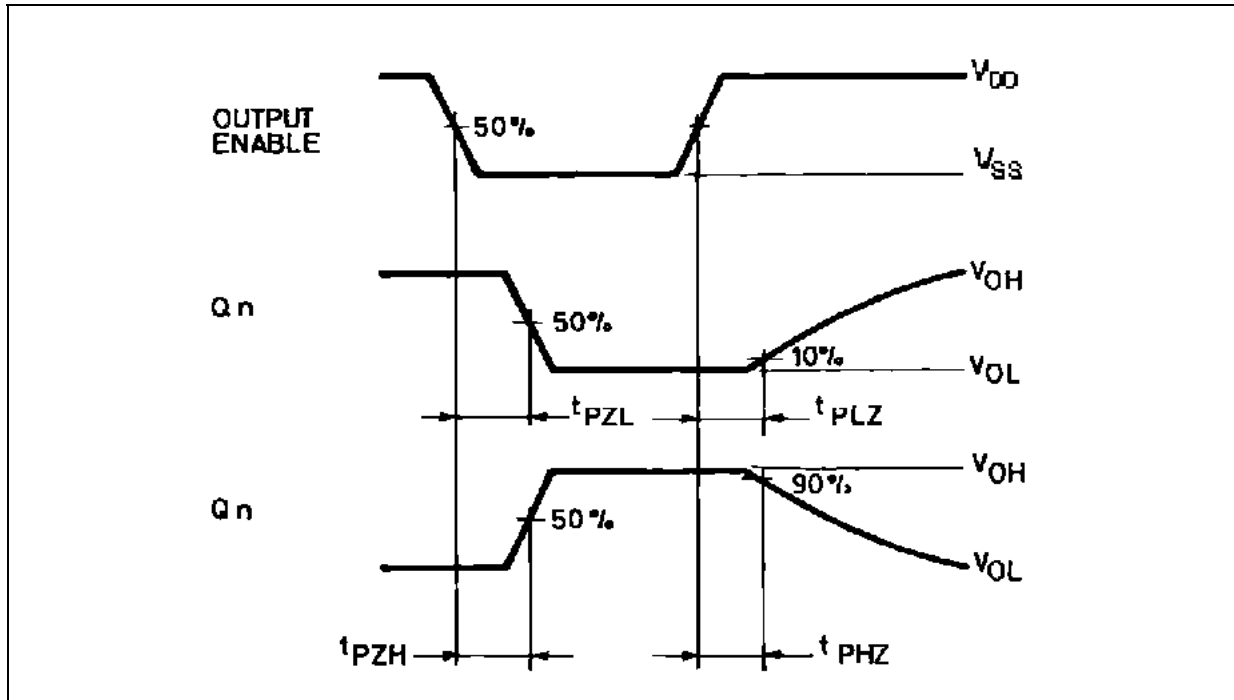


**WAVEFORM 2 : PROPAGATION DELAY TIME, PULSE WIDTH (STROBE), SETUP AND HOLD TIME (STROBE TO CLOCK) (f=1MHz; 50% duty cycle)**



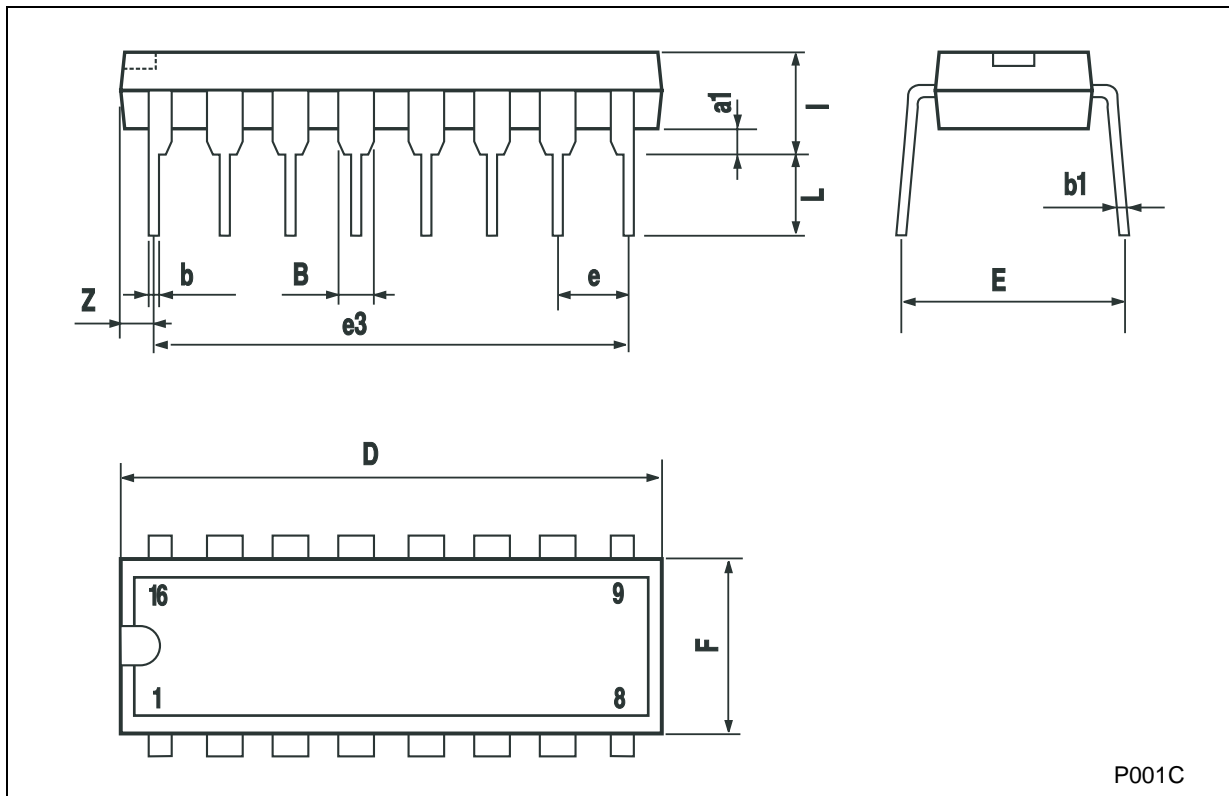


WAVEFORM 3 : OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)



**Plastic DIP-16 (0.25) MECHANICAL DATA**

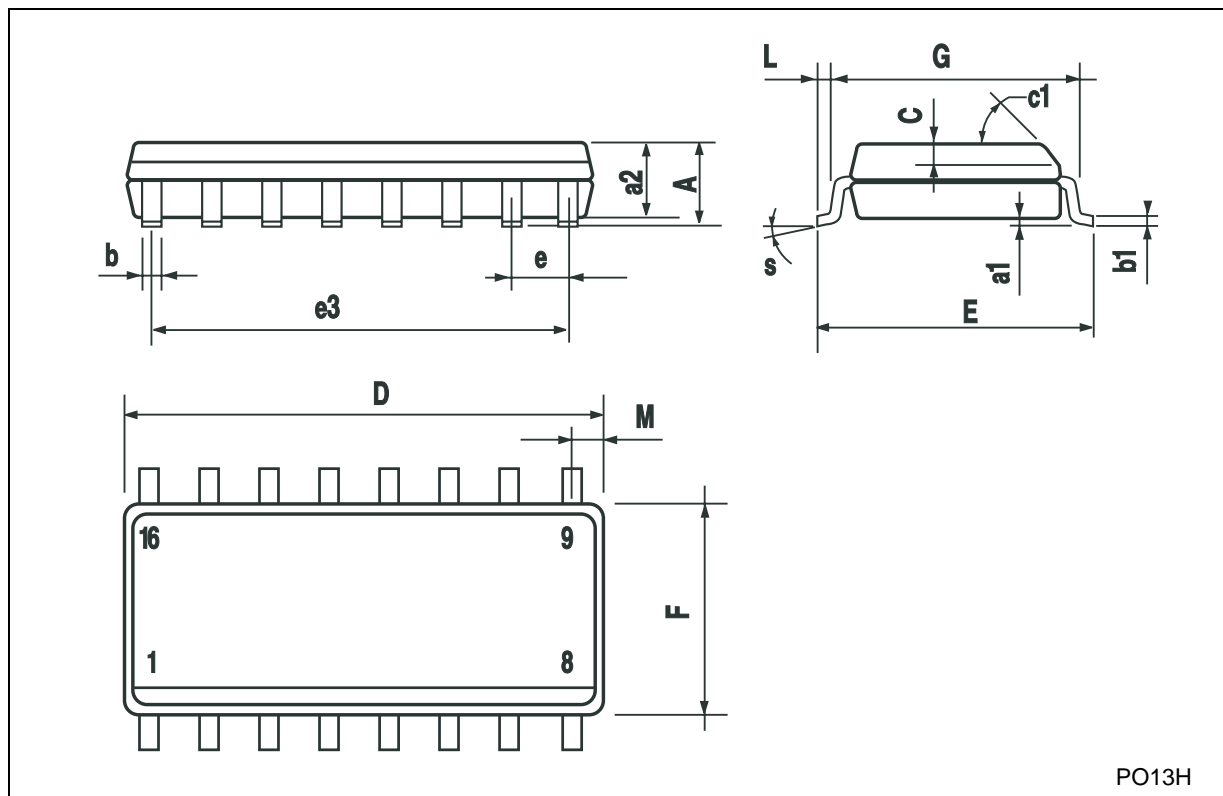
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

**SO-16 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



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