National Semiconductor

**PRELIMINARY**
June 1999

# LMX2335L/LMX2336L
# PLLatinum™ Low Power Dual Frequency Synthesizer for RF Personal Communications

**LMX2335L 1.1 GHz/1.1 GHz**
**LMX2336L 2.0 GHz/1.1 GHz**

## General Description

The LMX2335L and LMX2336L are monolithic, integrated dual frequency synthesizers, including two high frequency prescalers, and are designed for applications requiring two RF phase-lock loops. They are fabricated using National's 0.5µ ABiC V silicon BiCMOS process.

The LMX2335L/36L contains two dual modulus prescalers. A 64/65 or a 128/129 prescaler can be selected for each RF synthesizer. A second reference divider chain is included in the IC for improved system noise. The LMX2335L/36L combined with a high quality reference oscillator, two loop filters, and two external voltage controlled oscillators generates very stable low noise RF local oscillator signals.

Serial data is transferred into the LMX2335L/36L via a three wire interface (Data, Enable, Clock). Supply voltage can range from 2.7V to 5.5V. The LMX2335L/36L feature very low current consumption; LMX2335L 4.0 mA at 5V, LMX2336L 5.5 mA at 5V. The LMX2335L is available in SO, TSSOP and CSP 16-pin surface mount plastic packages. The LMX2336L is available in a TSSOP 20-pin and CSP 24-pin surface mount plastic package.

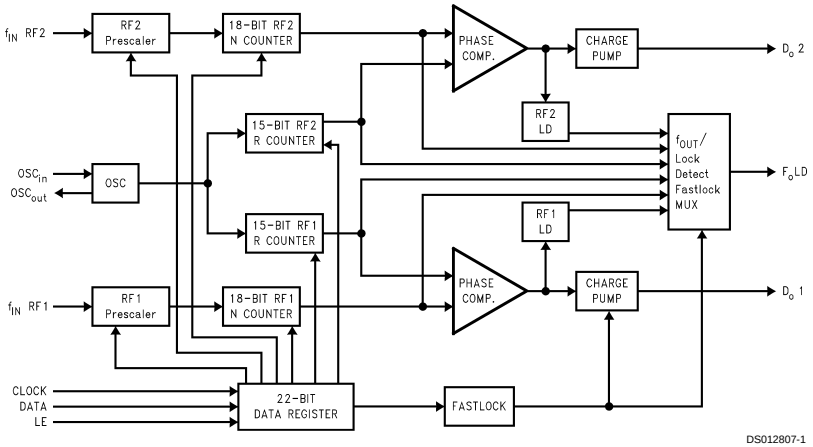
## Features

- Ultra low current consumption
- 2.7V to 5.5V operation
- Selectable synchronous and asynchronous powerdown mode:
  $I_{CC}$ = 1 µA (typ)
- Dual modulus prescaler: 64/65 or 128/129
- Selectable charge pump TRI-STATE® mode
- Selectable charge pump current levels
- Selectable Fastlock™ mode
- Upgrade and compatible to LMX2335/36
- Small-outline, plastic, surface mount TSSOP package
- LMX2336 available in CSP package

## Applications

- Cellular telephone systems (AMPS, ETACS, RCR-27)
- Cordless telephone systems (DECT, ISM , PHS, CT-1+)
- Personal Communication Systems (DCS-1800, PCN-1900)
- Dual Mode PCS phones
- Cable TV Tuners (CATV)
- Other wireless communication systems

## Functional Block Diagram

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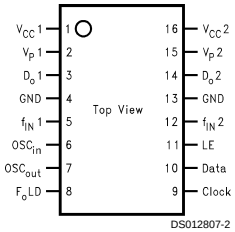
Fastlock™, MICROWIRE™ and PLLatinum™ are trademarks of National Semiconductor Corporation.

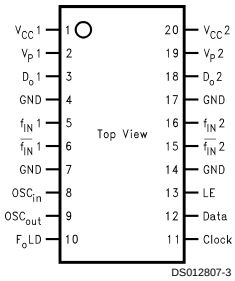
## Connection Diagrams

**LMX2335L**
**(Top View)**



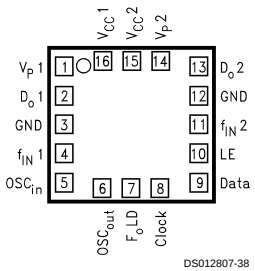

**Order Number LMX2335LM or LM2335LTM**
**NS Package Number M16A and MTC16**

**LMX2336L**
**(Top View)**



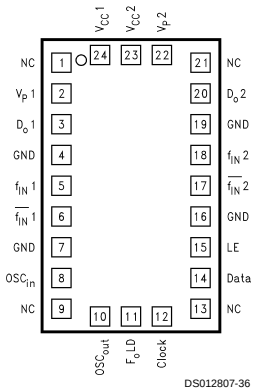

**Order Number LMX2336LTM**
**NS Package Number MTC20**

**LMX2335L**
**(Top View)**




**Order Number LMX2335LSLB**
**NS Package Number SLB16A**

**LMX2336L**
**(Top View)**




**Order Number LMX2336LSLB**
**NS Package Number SLB24A**

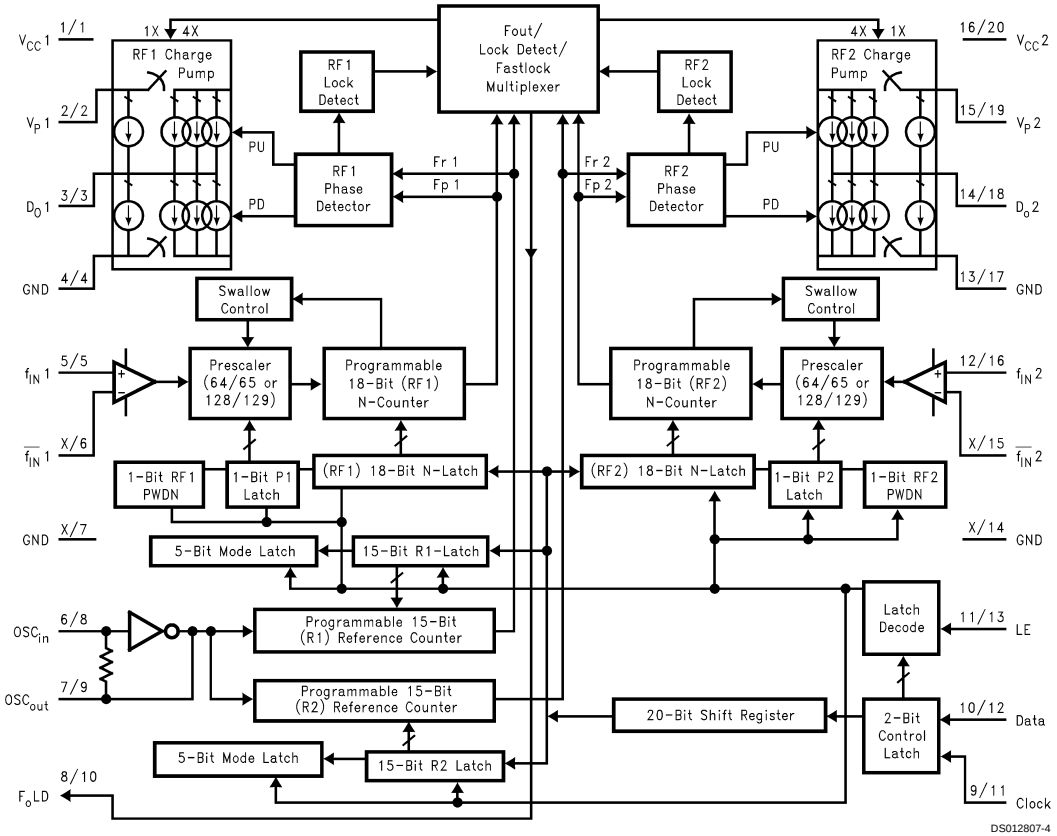
## Pin Descriptions

| Pin No. 2336LTM | Pin No. 2336LSLB | Pin No. 2335LTM | Pin No. 2335LSLB | Pin Name | I/O | Description |
|---|---|---|---|---|---|---|
| 1 | 24 | 1 | 16 | $V_{CC}$1 | | Power supply voltage input for RF1 analog and RF1 digital circuits. Input may range from 2.7V to 5.5V. $V_{CC}$1 must equal $V_{CC}$2. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane. |
| 2 | 2 | 2 | 1 | $V_p$1 | | Power supply for RF1 charge pump. Must be ≥ $V_{CC}$. |
| 3 | 3 | 3 | 2 | $D_o$1 | O | RF1 charge pump output. For connection to a loop filter for driving the input of an external VCO. |
| 4 | 4 | 4 | 3 | GND | | LMX2335L: Ground for RF1 analog and RF1 digital circuits. LMX2336L: Ground for RF digital circuits. |
| 5 | 5 | 5 | 4 | $f_{IN}$ 1 | I | RF1 prescaler input. Small signal input from the VCO. |
| 6 | 6 | X | X | /$f_{IN}$ 1 | I | RF1 prescaler complementary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. Capacitor is optional with loss of some sensitivity. |
| 7 | 7 | X | X | GND | | Ground for RF1 analog circuitry. |

## Pin Descriptions (Continued)

| Pin No. 2336LTM | Pin No. 2336LSLB | Pin No. 2335LTM | Pin No. 2335LSLB | Pin Name | I/O | Description |
|---|---|---|---|---|---|---|
| 8 | 8 | 6 | 5 | $OSC_{in}$ | I | Oscillator input. The input has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate. |
| 9 | 10 | 7 | 6 | $OSC_{out}$ | O | Oscillator output. |
| 10 | 11 | 8 | 7 | $F_o$LD | O | Multiplexed output of the programmable or reference dividers, lock detect signals and Fastlock mode. CMOS output *(see Programmable Modes).* |
| 11 | 12 | 9 | 8 | Clock | I | High impedance CMOS Clock input. Data for the various latches is clocked in on the rising edge, into the 20-bit shift register. |
| 12 | 14 | 10 | 9 | Data | I | Binary serial data input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input. |
| 13 | 15 | 11 | 10 | LE | I | Load enable high impedance CMOS input. When LE goes HIGH, data stored in the shift registers is loaded into one of the 4 appropriate latches (control bit dependent). |
| 14 | 16 | X | X | GND | | Ground for RF2 analog circuitry. |
| 15 | 17 | X | X | $/f_{IN}2$ | I | RF2 prescaler complementary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. Capacitor is optional with loss of some sensitivity. |
| 16 | 18 | 12 | 11 | $f_{IN}$ 2 | I | RF2 prescaler input. Small signal input from the VCO. |
| 17 | 19 | 13 | 12 | GND | | LMX2335L: Ground for RF2 analog, RF2 digital, MICROWIRE, $F_o$LD and Oscillator circuits. LMX2336L: Ground for IF digital, MICROWIRE, $F_o$LD and oscillator circuits. |
| 18 | 20 | 14 | 13 | $D_o$ 2 | O | RF2 charge pump output. For connection to a loop filter for driving the input of an external VCO. |
| 19 | 22 | 15 | 14 | $V_p2$ | | Power supply for RF2 charge pump. Must be $\geq V_{CC}$. |
| 20 | 23 | 16 | 15 | $V_{CC}2$ | | Power supply voltage input for RF2 analog, RF2 digital, MICROWIRE, $F_o$LD and oscillator circuits. Input may range from 2.7V to 5.5V. $V_{CC}2$ must equal $V_{CC}1$. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane. |
| X | 1, 9, 13, 21 | X | X | NC | | No connect. |

## Block Diagram




**Note 1:** $V_{CC}1$ supplies power to the RF1 prescaler, N-counter, R-counter, and phase detector. $V_{CC}2$ supplies power to the RF2 prescaler, N-counter, phase detector, R-counter along with the $OSC_{in}$ buffer, MICROWIRE, and $F_o$LD. $V_{CC}1$ and $V_{CC}2$ are clamped to each other by diodes and must be run at the same voltage level.

**Note 2:** $V_P1$ and $V_P2$ can be run separately as long as $V_P \geq V_{CC}$.

**LMX2335L Pin # → 8/10 ← LMX2336L Pin #**
**Pin Name → $F_o$LD**
**X signifies a function not bonded out to a pin**

## Absolute Maximum Ratings (Notes 1, 2)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

Power Supply Voltage

| | |
|---|---|
| $V_{CC}$ | −0.3V to +6.5V |
| $V_P$ | −0.3V to +6.5V |
| Voltage on Any Pin with GND = 0V ($V_I$) | −0.3V to $V_{CC}$ +0.3V |
| Storage Temperature Range ($T_S$) | −65˚C to +150˚C |
| Lead Temperature (solder 4 sec.) ($T_L$) | +260˚C |

## Recommended Operating Conditions

Power Supply Voltage

| | |
|---|---|
| $V_{CC}$ | 2.7V to 5.5V |
| $V_P$ | $V_{CC}$ to +5.5V |
| Operating Temperature ($T_A$) | −40˚C to +85˚C |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

**Note 2:** This device is a high performance RF integrated circuit with an ESD rating <2 keV and is ESD sensitive. Handling and assembly of this device should only be done at ESD protected work stations.

## Electrical Characteristics

$V_{CC}$ = 5.0V, $V_P$ = 5.0V; $T_A$ = 25˚C, except as specified

| Symbol | Parameter | | Conditions | Value | | | Units |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $I_{CC}$ | Power Supply Current | LMX2335L RF1 and RF2 | $V_{CC}$ = 2.7V to 5.5V | | 4.0 | 5.2 | mA |
| $I_{CC}$ | | LMX2335L RF1 only | | | 2.0 | 2.6 | mA |
| $I_{CC}$ | | LMX2336L RF1 and RF2 | | | 5.5 | 7 | mA |
| | | LMX2336L RF1 only | | | 3.3 | 4.3 | mA |
| $f_{IN}$ 1 | Operating Frequency | LMX2335L | | 0.100 | | 1.1 | GHz |
| $f_{IN}$ 2 | | | | 0.050 | | 1.1 | GHz |
| $f_{IN}$1 | | LMX2336L | | 0.200 | | 2.0 | GHz |
| $f_{IN}$2 | | | | 0.050 | | 1.1 | GHz |
| $I_{CC\text{-}PWDN}$ | Powerdown Current | LMX2335L/2336L | $V_{CC}$ = 5.5V | | 1 | 10 | µA |
| $f_{OSC}$ | Oscillator Frequency | | With resonator load on $OSC_{out}$ | 5 | | 20 | MHz |
| $f_{OSC}$ | | | No load on $OSC_{out}$ | 5 | | 40 | MHz |
| $f_\phi$ | Maximum Phase Detector Frequency | | | | 10 | | MHz |
| $Pf_{IN}$ | RF Input Sensitivity | | $V_{CC}$ = 3.0V, f > 100 MHz | −15 | | 0 | dBm |
| $Pf_{IN}$ | | | $V_{CC}$ = 5.0V, f > 100 MHz | −10 | | 0 | |
| $V_{OSC}$ | Oscillator Sensitivity | | $OSC_{in}$ | 0.5 | | | $V_{PP}$ |
| $V_{IH}$ | High-Level Input Voltage | | (Note 4) | 0.8 $V_{CC}$ | | | V |
| $V_{IL}$ | Low-Level Input Voltage | | (Note 4) | | | 0.2 $V_{CC}$ | V |
| $I_{IH}$ | High-Level Input Current | | $V_{IH}$ = $V_{CC}$ = 5.5V (Note 4) | −1.0 | | 1.0 | µA |
| $I_{IL}$ | Low-Level Input Current | | $V_{IL}$ = 0V, $V_{CC}$ = 5.5V (Note 4) | −1.0 | | 1.0 | µA |
| $I_{IH}$ | Oscillator Input Current | | $V_{IH}$ = $V_{CC}$ = 5.5V | | | 100 | µA |
| $I_{IL}$ | Oscillator Input Current | | $V_{IL}$ = 0V, $V_{CC}$ = 5.5V | −100 | | | µA |
| $I_{Do\text{-}SOURCE}$ | Charge Pump Output Current | | $V_{Do}$ = $V_P$/2, $I_{CPo}$ = LOW (Note 3) | | −1.25 | | mA |
| $I_{Do\text{-}SINK}$ | | | $V_{Do}$ = $V_P$/2, $I_{CPo}$ = LOW (Note 3) | | 1.25 | | mA |
| $I_{Do\text{-}SOURCE}$ | | | $V_{Do}$ = $V_P$/2, $I_{CPo}$ = HIGH (Note 3) | | −4.25 | | mA |
| $I_{Do\text{-}SINK}$ | | | $V_{Do}$ = $V_P$/2, $I_{CPo}$ = HIGH (Note 3) | | 4.25 | | mA |
| $I_{Do\text{-}TRI}$ | Charge Pump TRI-STATE Current | | 0.5V ≤ $V_{Do}$ ≤ $V_{CC}$ − 0.5V T = 25˚C | −5.0 | | 5.0 | nA |
| $V_{OH}$ | High-Level Output Voltage | | $I_{OH}$ = −500 µA | $V_{CC}$ − 0.4 | | | V |
| $V_{OL}$ | Low-Level Output Voltage | | $I_{OL}$ = 500 µA | | | 0.4 | V |

## Electrical Characteristics (Continued)

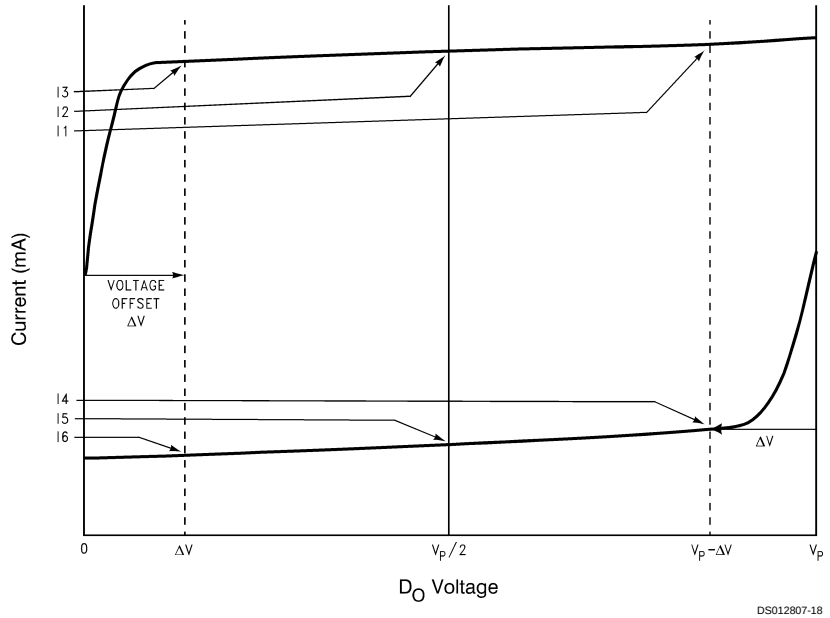
$V_{CC}$ = 5.0V, $V_P$ = 5.0V; $T_A$ = 25˚C, except as specified

| Symbol | Parameter | Conditions | Value | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{CS}$ | Data to Clock Set Up Time | See Data Input Timing | 50 | | | ns |
| $t_{CH}$ | Data to Clock Hold Time | See Data Input Timing | 10 | | | ns |
| $t_{CWH}$ | Clock Pulse Width High | See Data Input Timing | 50 | | | ns |
| $t_{CWL}$ | Clock Pulse Width Low | See Data Input Timing | 50 | | | ns |
| $t_{ES}$ | Clock to Load Enable Set Up Time | See Data Input Timing | 50 | | | ns |
| $t_{EW}$ | Load Enable Pulse Width | See Data Input Timing | 50 | | | ns |

**Note 3:** See PROGRAMMABLE MODES for $I_{CPo}$ description.

**Note 4:** Clock, Data and LE does not include $f_{IN}1$, $f_{IN}2$ and $OSC_{in}$.

## Charge Pump Current Specification Definitions

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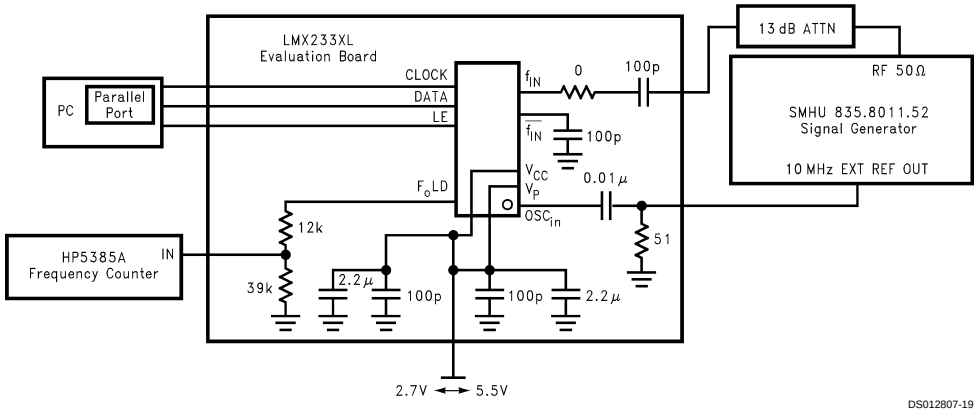
I1 = CP sink current at $V_{Do}$ = $V_P$ − ΔV
I2 = CP sink current at $V_{Do}$ = $V_P$/2
I3 = CP sink current at $V_{Do}$ = ΔV
I4 = CP source current at $V_{Do}$ = $V_P$ − ΔV
I5 = CP source current at $V_{Do}$ = $V_P$/2
I6 = CP source current at $V_{Do}$ = ΔV
V = Voltage offset from positive and negative rails. Dependent on VCO tuning range relative to $V_{CC}$ and ground. Typical values are between 0.5V and 1.0V.

1. $I_{Do}$ vs $V_{Do}$ = Charge Pump Output Current magnitude variation vs Voltage =
   [½ * {|I1| − |I3|}]/[½ * {|I1| + |I3|}] * 100% and [½ * {|I4| − |I6|}]/[½ * {|I4| + |I6|}] * 100%
2. $I_{Do\text{-}sink}$ vs $I_{Do\text{-}source}$ = Charge Pump Output Current Sink vs Source Mismatch =
   [|I2| − |I5|]/[½ * {|I2| + |I5|}] * 100%
3. $I_{Do}$ vs $T_A$ = Charge Pump Output Current magnitude variation vs Temperature =
   [|I2 @ temp| − |I2 @ 25˚C|]/|I2 @ 25˚C| * 100% and [|I5 @ temp| − |I5 @ 25˚C|]/|I5 @ 25˚C| * 100%

## RF Sensitivity Test Block Diagram

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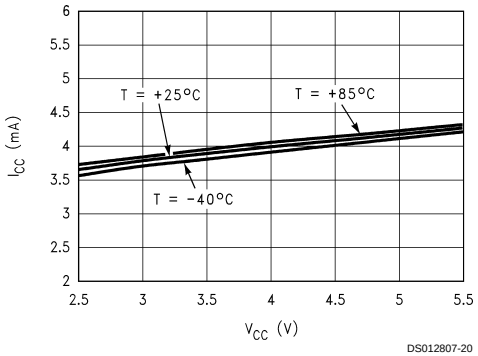
**Note 5:** N = 10,000R = 50P = 64

**Note 6:** Sensitivity limit is reached when the error of the divided RF output, $F_oLD$, is ≥ 1 Hz.

## Typical Performance Characteristics

**$I_{CC}$ vs $V_{CC}$**
**LMX2335L**

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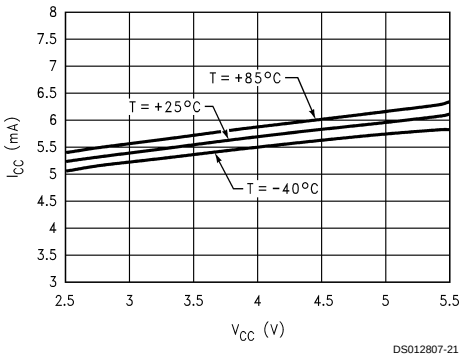
**$I_{CC}$ vs $V_{CC}$**
**LMX2336L**

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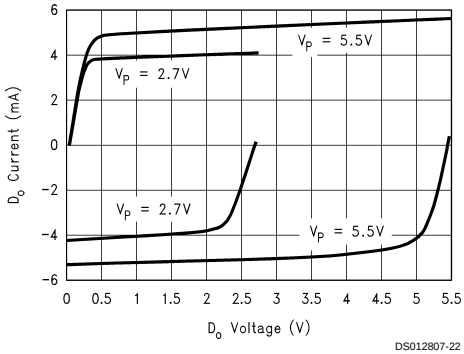
**Charge Pump Current vs $D_o$ Voltage**
**$I_{cp}$ = HIGH**

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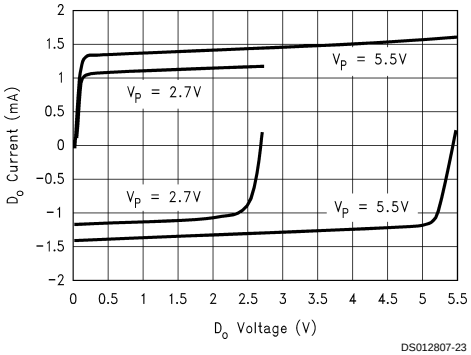
**Charge Pump Current vs $D_o$ Voltage**
**$I_{cp}$ = LOW**

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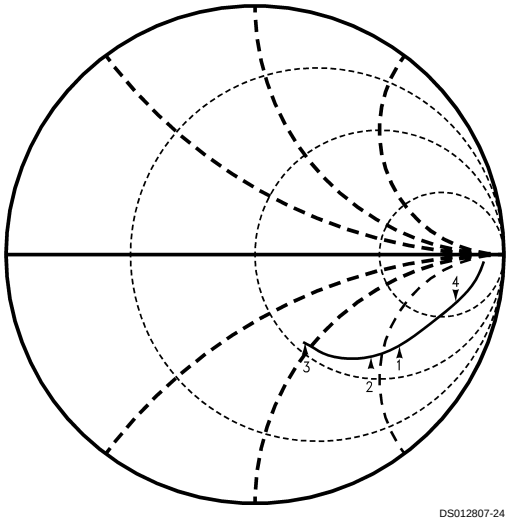
## Typical Performance Characteristics (Continued)

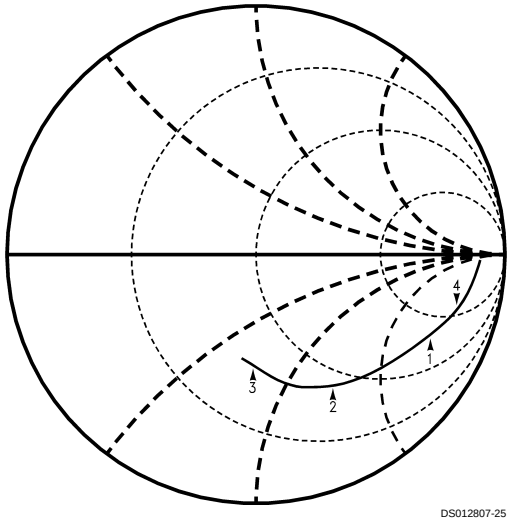
**LMX2335L Input Impedance (for SO package)**
**$V_{CC}$ = 2.7V to 5.5V, $I_{IN}$ = 50 MHz to 1.5 GHz**




DS012807-24

Marker 1 = 1 GHz, Real = 94, Imaginary = −118
Marker 2 = 1.2 GHz, Real = 72, Imaginary = −88
Marker 3 = 1.5 GHz, Real = 53, Imaginary = −45
Marker 4 = 500 MHz, Real = 201, Imaginary = −224

**LMX2336L Input Impedance (for TSSOP package)**
**$V_{CC}$ = 2.7V to 5.5V, $f_{IN}$ = 50 MHz to 2.5 GHz**

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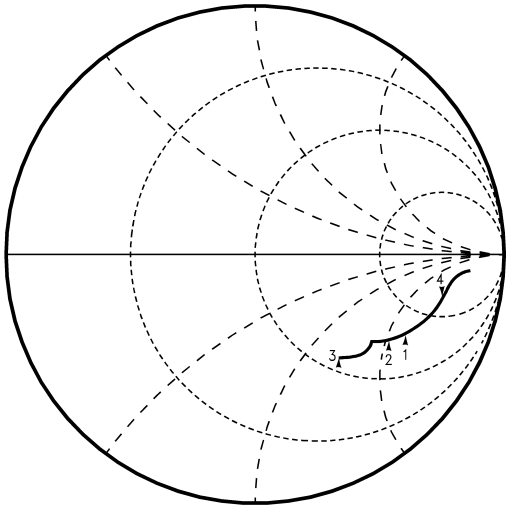
Marker 1 = 1 GHz, Real = 97, Imaginary = −146
Marker 2 = 1.89 GHz, Real = 43, Imaginary = −67
Marker 3 = 2.5 GHz, Real = 30, Imaginary = −33
Marker 4 = 500 MHz, Real = 189, Imaginary = −233

**LMX2335L Input Impedance (for TSSOP package)**
**$V_{CC}$ = 2.7V to 5.5V, $f_{IN}$ = 50 MHz to 2.5 GHz**




Marker 1 = 1 GHz, Real = 111, Imaginary = −129
Marker 2 = 1.2 GHz, Real = 87, Imaginary = −102
Marker 3 = 1.5 GHz, Real = 61, Imaginary = −70
Marker 4 = 500 MHz, Real = 232, Imaginary = −203

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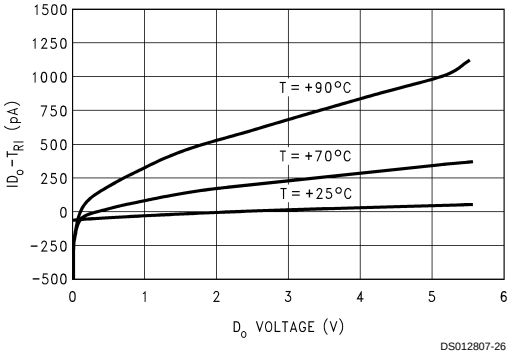
## Typical Performance Characteristics (Continued)

**$I_{DO}$ TRI-STATE vs $D_o$ Voltage**

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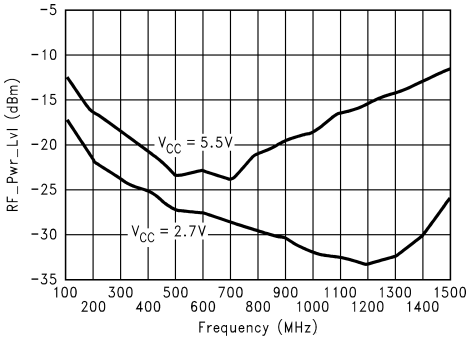
**LMX2335L RF1 Sensitivity vs Frequency**

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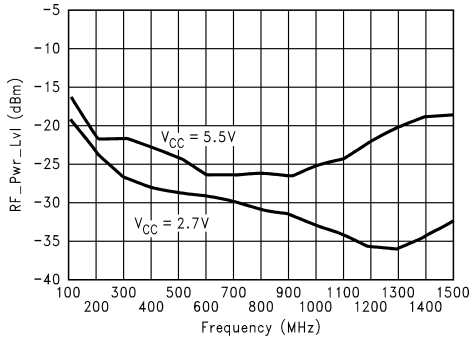
**LMX2335L RF2 Sensitivity vs Frequency**

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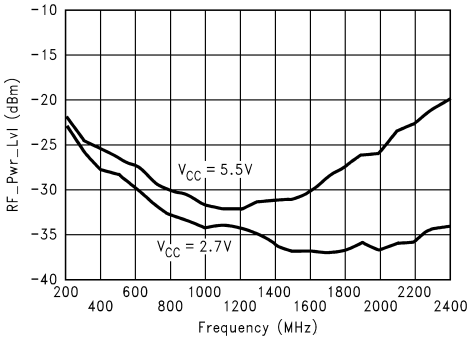
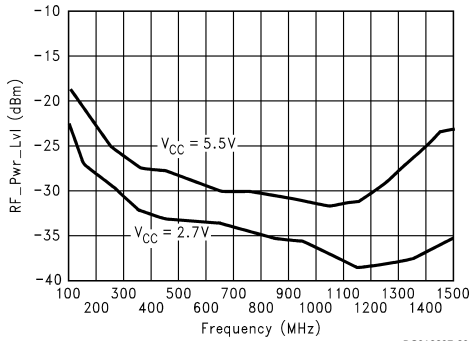
**LMX2336L RF1 Sensitivity vs Frequency**



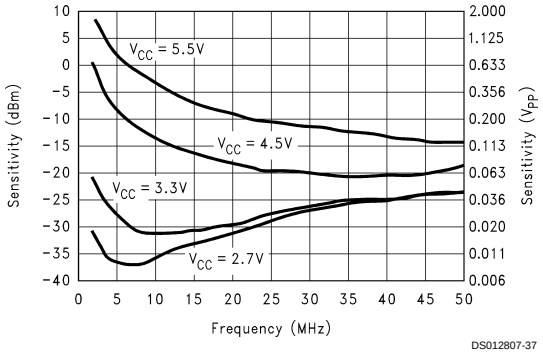

DS012807-29

**LMX2336L RF2 Sensitivity vs Frequency**




DS012807-30

**Oscillator Input Sensitivity vs Frequency**

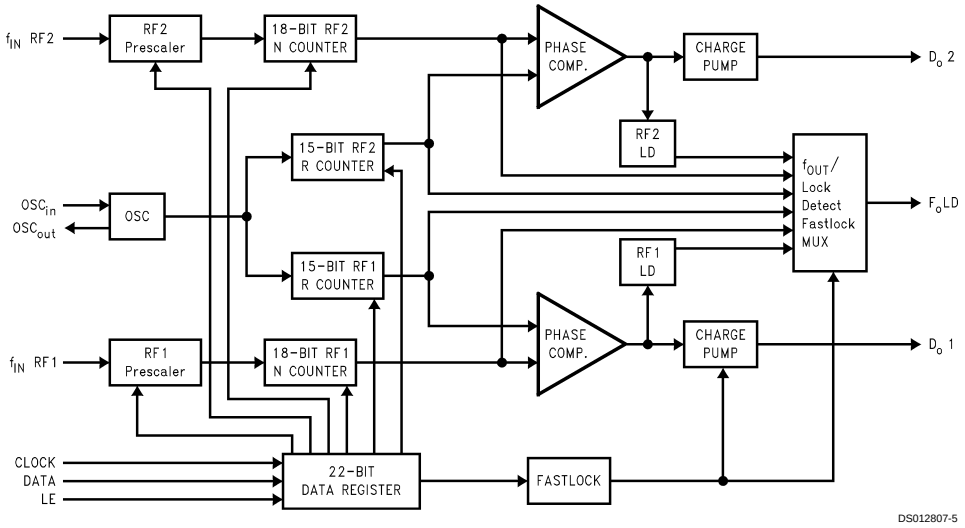



DS012807-37

## Functional Description

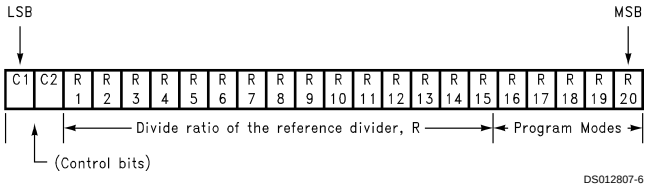
The simplified block diagram below shows the 22-bit data register, two 15-bit R Counters and two 18-bit N Counters (intermediate latches are not shown). The data stream is clocked (on the rising edge of Clock) into the DATA register, MSB first. The data stored in the shift register is loaded into one of the 4 appropriate latches on the rising edge of LE. The last two bits are the Control Bits. The DATA is transferred into the counters as follows:

| Control Bits | | DATA Location |
|---|---|---|
| C1 | C2 | |
| 0 | 0 | RF2 R Counter |
| 0 | 1 | RF1 R Counter |
| 1 | 0 | RF2 N Counter |
| 1 | 1 | RF1 N Counter |




### PROGRAMMABLE REFERENCE DIVIDERS (RF1 AND RF2 R COUNTERS)

If the Control Bits are 00 or 01 (00 for RF2 and 01 for RF1) data is transferred from the 22-bit shift register into a latch which sets the 15-bit R Counter. Serial data format is shown below.




### 15-BIT PROGRAMMABLE REFERENCE DIVIDER RATIO (R COUNTER)

| Divide Ratio | R15 | R14 | R13 | R12 | R11 | R10 | R9 | R8 | R7 | R6 | R5 | R4 | R3 | R2 | R1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 32767 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

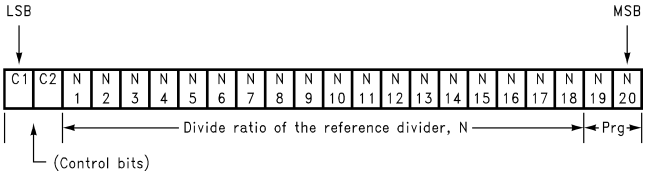
**Notes:**

Divide ratios less than 3 are prohibited.
Divide ratio: 3 to 32767
R1 to R15: These bits select the divide ratio of the programmable reference divider.
Data is shifted in MSB first.

## Functional Description (Continued)

### PROGRAMMABLE DIVIDER (N COUNTER)

Each N counter consists of the 7-bit swallow counter (A counter) and the 11-bit programmable counter (B counter). If the Control Bits are 10 or 11 (10 for RF2 counter and 11 for RF1 counter) data is transferred from the 20-bit shift register into a 7-bit latch (which sets the Swallow (A) Counter) and an 11-bit latch (which sets the 11-bit programmable (B) Counter), MSB first. Serial data format is shown below.




DS012807-7

### 7-BIT SWALLOW COUNTER DIVIDE RATIO (A COUNTER)

| Divide Ratio A | N 7 | N 6 | N 5 | N 4 | N 3 | N 2 | N 1 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| • | • | • | • | • | • | • | • |
| 127 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Notes:**
Divide ratio: 0 to 127
B ≥ A
A < P

### 11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO (B COUNTER)

| Divide Ratio B | N 18 | N 17 | N 16 | N 15 | N 14 | N 13 | N 12 | N 11 | N 10 | N 9 | N 8 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| • | • | • | • | • | • | • | • | • | • | • | • |
| 2047 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Note:**
Divide ratio: 3 to 2047 (Divide ratios less than 3 are prohibited)
B ≥ A

### PULSE SWALLOW FUNCTION

$f_{VCO} = [(P \times B) + A] \times f_{OSC}/R$

$f_{VCO}$: Output frequency of external voltage controlled oscillator (VCO)
B: Preset divide ratio of binary 11-bit programmable counter (3 to 2047)
A: Preset divide ratio of binary 7-bit swallow counter
($0 \le A \le P$; $A \le B$)
$f_{OSC}$: Output frequency of the external reference frequency oscillator
R: Preset divide ratio of binary 15-bit programmable reference counter (3 to 32767)
P: Preset modulus of dual modulus prescaler (P = 64 or 128)

### PROGRAMMABLE MODES

Several modes of operation can be programmed with bits R16–R20 including the phase detector polarity, charge pump tristate and the output of the $F_o$LD pin. The prescaler and power down modes are selected with bits N19 and N20. The programmable modes are shown in *Table 1*. Truth table for the programmable modes and $F_o$LD output are shown in *Table 2* and *Table 3*.

## Functional Description (Continued)

**TABLE 1. Programmable Modes**

| C1 | C2 | R16 | R17 | R18 | R19 | R20 |
|---|---|---|---|---|---|---|
| 0 | 0 | RF2 Phase Detector Polarity | RF2 $I_{CPo}$ | RF2 $D_o$ TRI-STATE | RF2 LD | RF2 $F_o$ |
| 0 | 1 | RF1 Phase Detector Polarity | RF1 $I_{CPo}$ | RF1 $D_o$ TRI-STATE | RF1 LD | RF1 $F_o$ |

| C1 | C2 | N19 | N20 |
|---|---|---|---|
| 1 | 0 | RF2 Prescaler | Pwdn RF2 |
| 1 | 1 | RF1 Prescaler | Pwdn RF1 |

**TABLE 2. Mode Select Truth Table**

| | **Phase Detector Polarity** (Note 9) | **$D_o$ TRI-STATE** (Note 7) | **$I_{CPo}$** (Note 8) | **RF1 Prescaler** | **RF2 Prescaler** | **Pwdn** (Note 7) |
|---|---|---|---|---|---|---|
| 0 | Negative | Normal Operation | LOW | 64/65 | 64/65 | pwrd up |
| 1 | Positive | TRI-STATE | HIGH | 128/129 | 128/129 | pwrd dn |

**Note 7:** Refer to POWERDOWN OPERATION in Functional Description.

**Note 8:** The $I_{CPo}$ LOW current state = 1/4 x $I_{CPo}$ HIGH current.

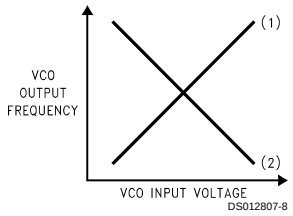
**Note 9:** PHASE DETECTOR POLARITY

Depending upon VCO characteristics, the R16 bits should be set accordingly:

When VCO characteristics are positive like (1), R16 should be set HIGH;

When VCO characteristics are negative like (2), R16 should be set LOW.

**VCO Characteristics**



## Functional Description (Continued)

**TABLE 3. The $F_o$LD Output Truth Table**

| RF1 R[19] (RF1 LD) | RF2 R[19] (RF2 LD) | RF1 R[20] (RF1 $F_O$) | RF2 R[20] (RF2 $F_O$) | $F_o$LD Output State |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disabled (Note 10) |
| 0 | 1 | 0 | 0 | RF2 Lock Detect (Note 11) |
| 1 | 0 | 0 | 0 | RF1 Lock Detect (Note 11) |
| 1 | 1 | 0 | 0 | RF1/RF2 Lock Detect (Note 11) |
| X | 0 | 0 | 1 | RF2 Reference Divider Output |
| X | 0 | 1 | 0 | RF1 Reference Divider Output |
| X | 1 | 0 | 1 | RF2 Programmable Divider Output |
| X | 1 | 1 | 0 | RF1 Programmable Divider Output |
| 0 | 0 | 1 | 1 | Fastlock (Note 12) |
| 0 | 1 | 1 | 1 | RF2 Counter Reset (Note 13) |
| 1 | 0 | 1 | 1 | RF1 Counter Reset (Note 13) |
| 1 | 1 | 1 | 1 | RF1 and RF2 Counter Reset (Note 13) |

X — don't care condition

**Note 10:** When the $F_o$LD output is disabled it is actively pulled to a low logic state.

**Note 11:** Lock detect output provided to indicate when the VCO frequency is in "lock". When the loop is locked and a lock detect mode is selected, the pins output is HIGH, with narrow pulses LOW. In the RF1/RF2 lock detect mode a locked condition is indicated when RF2 and RF1 are both locked.

**Note 12:** The Fastlock mode utilized the $F_o$LD output pin to switch a second loop filter damping resistor to ground during fastlock operation. Activation of Fastlock occurs whenever the RF loop's Icpo magnitude bit #17 is selected HIGH (while the #19 and #20 mode bits are set for Fastlock).

**Note 13:** The RF2 counter reset mode resets RF2 PLL's R and N counters and brings RF2 charge pump output to a TRI-STATE condition. The RF1 counter reset mode resets RF1 PLL's R and N counters and brings RF1 charge pump output to a TRI-STATE condition. The RF1 and RF2 counter reset mode resets all counters and brings both charge pump output to a TRI-STATE condition. Upon removal of the Reset bits the N counter resumes counting in "close" alignment with the R counter. (The maximum error is one prescaler cycle).

**POWERDOWN OPERATION**

Synchronous and asynchronous powerdown modes are both available by microwire selection. Synchronously powerdown occurs if the respective loop's R18 bit (Do TRI-STATE) is LOW when its N20 bit (Pwdn) becomes HI. Asynchronous powerdown occurs if the loop's R18 bit is HI when its N20 bit becomes HI.

In the synchronous powerdown mode, the powerdown function is gated by the charge pump to prevent unwanted frequency jumps. Once the powerdown program bit N20 is loaded, the part will go into powerdown mode when the charge pump reaches a TRI-STATE condition.

In the asynchronous powerdown mode, the device powers down immediately after the LE pin latches in a HI condition on the powerdown bit N20.

Activation of either the IF or RF PLL powerdown conditions in either synchronous or asynchronous modes forces the respective loop's R & N dividers to their load state condition and debiasing of it's respective Fin input to a high impedance state. The oscillator circuitry function does not become disabled until both IF and RF powerdown bits are activated. The MICROWIRE control register remains active and capable of loading and latching data during all of the powerdown modes.

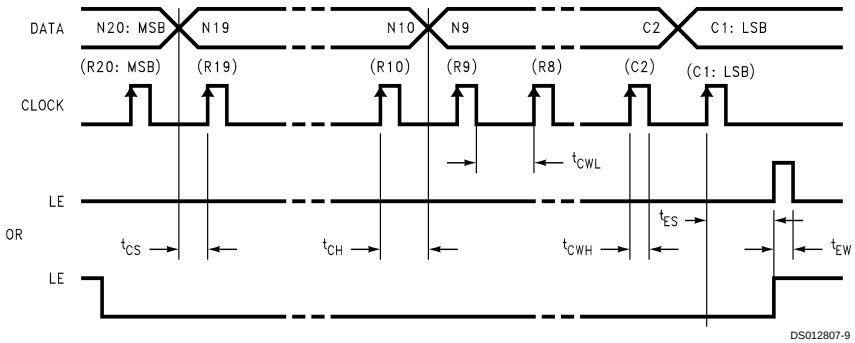
The device returns to an actively powered up condition in either synchronous ar asynchronous modes immediately upon LE latching LOW data into bit N20.

## Powerdown Mode Select Table

| R18 | N20 | Powerdown Status |
|---|---|---|
| 0 | 0 | PLL Active |
| 1 | 0 | PLL Active (Charge Pump Output TRI-STATE) |
| 0 | 1 | Synchronous Powerdown Initiated |
| 1 | 1 | Asynchronous Powerdown Initiated |

## Functional Description (Continued)

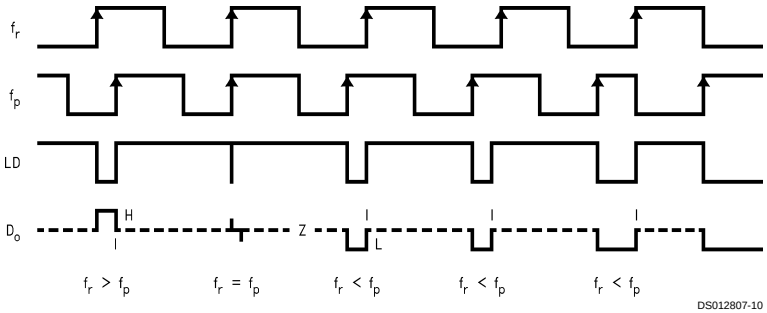
### SERIAL DATA INPUT TIMING




Parenthesis data indicates programmable reference divider data.
Data shifted into register on clock rising edge.
Data is shifted in MSB first.
$t_{CS}$ = Data to Clock Set Up Time
$t_{CH}$ = Data to Clock Hold Time
$t_{CWH}$ = Clock Pulse Width High
$t_{CWL}$ = Clock Pulse Width Low
$t_{ES}$ = Clock to Load Enable Set Up Time
$t_{EW}$ = Load Enable Pulse Width

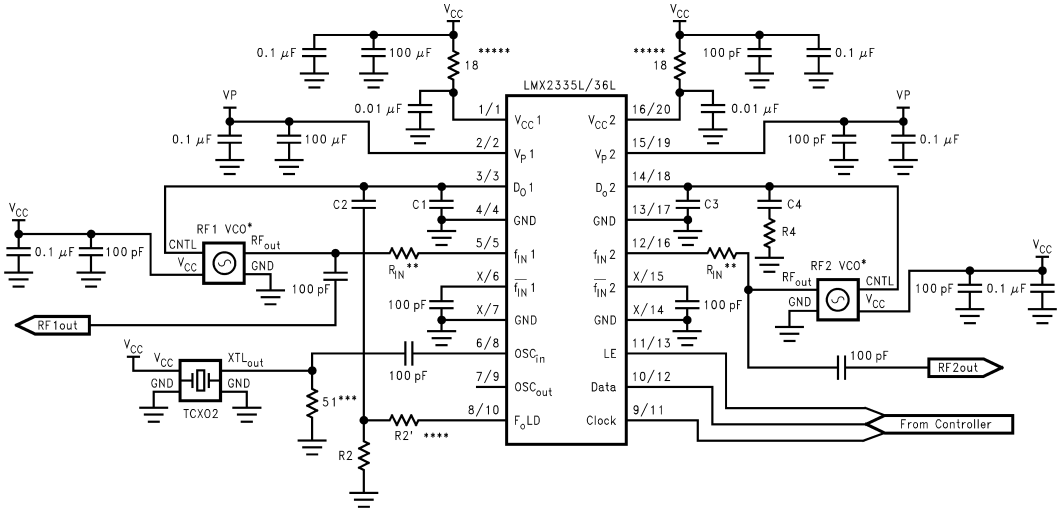
**Test Conditions:** The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC}/2$. The test waveform has an edge rate of 0.6V/ns with amplitudes of 2.2V @ $V_{CC}$ = 2.7V and 2.6V @ $V_{CC}$ = 5.5V.

### PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS




**Notes:** Phase difference detection range: −2π to +2π
The minimum width pump up and pump down current pulses occur at the $D_o$ pin when the loop is locked.

## Typical Application Example




DS012807-11

**Operational Notes:**

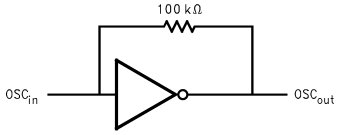
* VCO is assumed AC coupled.

** $R_{IN}$ increases impedance so that VCO output power is provided to the load rather than the PLL. Typical values are 10Ω to 200Ω depending on the VCO power level. $f_{IN}$ RF impedance ranges from 40Ω to 100Ω. $f_{IN}$ IF impedances are higher.

*** 50Ω termination is often used on test boards to allow use of external reference oscillator. For most typical products a CMOS clock is used and no terminating resistor is required. $OSC_{in}$may be AC or DC coupled. AC coupling is recommended because the input circuit provides its own bias. (See *Figure* below).

**** R2 configured $F_oLD$ for use in FastLock mode.

***** Adding RC filters to the $V_{CC}$ lines is recommended to reduce loop-to-loop noise coupling.




DS012807-12

**Application Hints:**

Proper use of grounds and bypass capacitors is essential to achieve a high level of performance. Crosstalk between pins can be reduced by careful board layout.

This is an electrostatic sensitive device. It should be handled only at static free work stations.

## Application Information

A block diagram of the basic phase locked loop is shown in *Figure 1*.

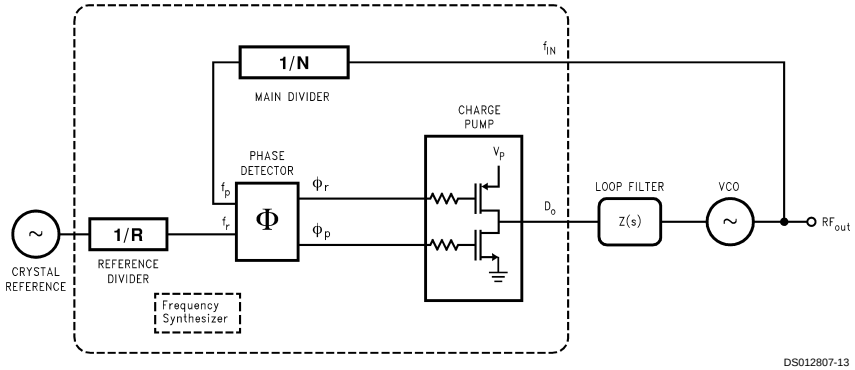



**FIGURE 1. Conventional PLL Architecture**

### Loop Gain Equations

A linear control system model of the phase feedback for a PLL in the locked state is shown in *Figure 2*. The open loop gain is the product of the phase comparator gain ($K_\phi$), the VCO gain ($K_{VCO}/s$), and the loop filter gain Z(s) divided by the gain of the feedback counter modulus (N). The passive loop filter configuration used is displayed in *Figure 3*, WHILE the complex impedance of the filter is given in equation 2.

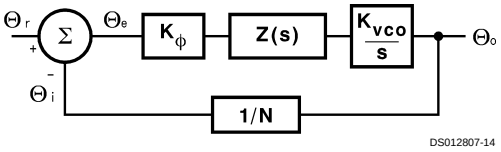



**FIGURE 2. PLL Linear Model**

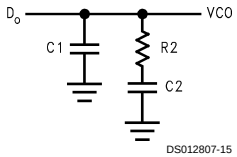



**FIGURE 3. Passive Loop Filter**

$$\text{Open Loop Gain} = H(s)\,G(s) = \frac{\Theta i}{\Theta e} = \frac{K_\phi Z(s) K_{VCO}}{Ns} \quad (1)$$

$$Z(s) = \frac{s(C2 \bullet R2) + 1}{S^2 (C1 \bullet C2 \bullet R2) + sC1 + sC2} \quad (2)$$

The time constants which determine the pole and zero frequencies of the filter transfer function can be defined as

$$T1 = R2 \bullet \frac{C1 \bullet C2}{C1 + C2}$$

$$T2 = R2 \bullet C2 \quad (3)$$

The 3rd order PLL Open Loop Gain can be calculated in terms of frequency, ω, the filter time contants T1 and T2, and the design constants Kϕ, $K_{VCO}$, and N.

$$G(s) \bullet H(s)\,|_{S = j \bullet w} = \frac{-K_\phi \bullet K_{VCO}(1 + jw \bullet T2)}{w^2 C1 \bullet N(1 + jw \bullet T1)} \bullet \frac{T1}{T2} \quad (4)$$

From *Equation (3)* we can see that the phase term will be dependent on the single pole and zero such that the phase margin is determined in *Equation (1)*.

$$\phi(\omega) = \tan^{-1}(\omega \bullet T2) - \tan^{-1}(\omega \bullet T1) + 180^\circ C \quad (5)$$

A plot of the magnitude and phase of G(s) H(s) for a stable loop, is shown in *Equation (4)* with a solid trace. The parameter $\phi_p$ shows the amount of phase margin that exists at the point the gain drops below zero (the cutoff frequency wp of the loop). In a critically damped system, the amount of phase margin would be approximately 45 degrees.

If we were now to redefine the cut off frequency, wp', as double the frequency which gave us our original loop bandwidth, wp, the loop response time would be approximately halved. Because the filter attenuation at the comparison frequency also diminishes, the spurs would have increased by approximately 6 dB. In the proposed Fastlock scheme, the higher spur levels and wider loop filter conditions would exist only during the initial lock-on phase — just long enough to reap the benefits of locking faster. The objective would be to open up the loop bandwidth but not introduce any additional complications or compromises related to our original design criteria. We would ideally like to momentarily shift the curve *Figure 4* over to a different cutoff frequency, illustrated by dotted line, without affecting the relative open loop gain and phase relationships. To maintain the same gain/phase relationship at twice the original cutoff frequency, other terms in the gain and phase equations 4 and 5 will have to compensate by the corresponding "1/w" or "$1/w^2$" factor. Examination of equations 3 and 5 indicates the damping resistor variable R2 could be chosen to compensate with "w" terms for the phase margin. This implies that another resistor of equal value to R2 will need to be switched in parallel with R2 during the initial lock period. We must also insure that the magnitude of the open loop gain, H(s)G(s) is equal to zero at wp' = 2 wp. $K_{VCO}$, Kϕ, N, or the net product of these terms can be changed by a factor of 4, to counteract with $w^2$ term present in the denominator of equation 3. The Kϕ term was chosen to complete the transformation because it can readily be switched between 1X and 4X values. This is accomplished by increasing the charge pump output current from 1 mA in the standard mode to 4 mA in Fastlock.

## Application Information (Continued)

### Fastlock Circuit Implementation

A diagram of the Fastlock scheme as implemented in National Semiconductors LMX2335L/36L PLL is shown in *Figure 5*. When a new frequency is loaded, and the RF1 $I_{CPo}$ bit is set high, the charge pump circuit receives an input to deliver 4 times the normal current per unit phase error while an open drain NMOS on chip device switches in a second R2 resistor element to ground. The user calculates the loop filter component values for the normal steady state considerations. The device configuration ensures that as long as a second identical damping resistor is wired in appropriately, the loop will lock faster without any additional stability considerations to account for. Once locked on the correct frequency, the user can return the PLL to standard low noise operation by sending a MICROWIRE instruction with the RF1 $I_{CPo}$ bit set low. This transition does not affect the charge on the loop filter capacitors and is enacted synchronous with the charge pump output. This creates a nearly seamless change between Fastlock and standard mode.

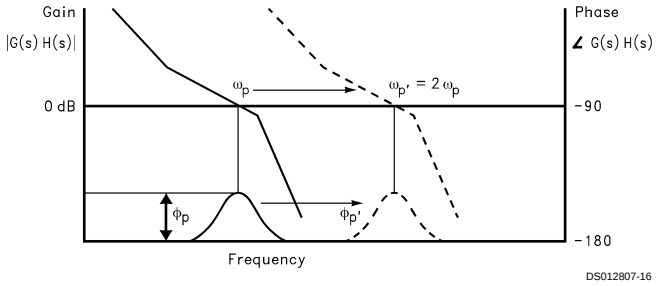



**FIGURE 4. Open Loop Response Bode Plot**

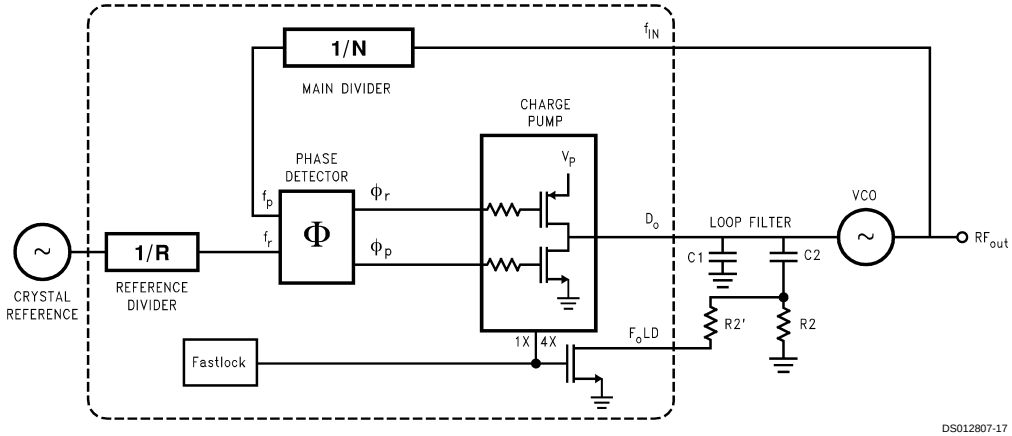
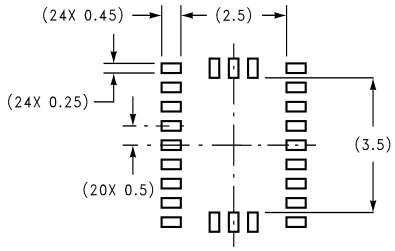


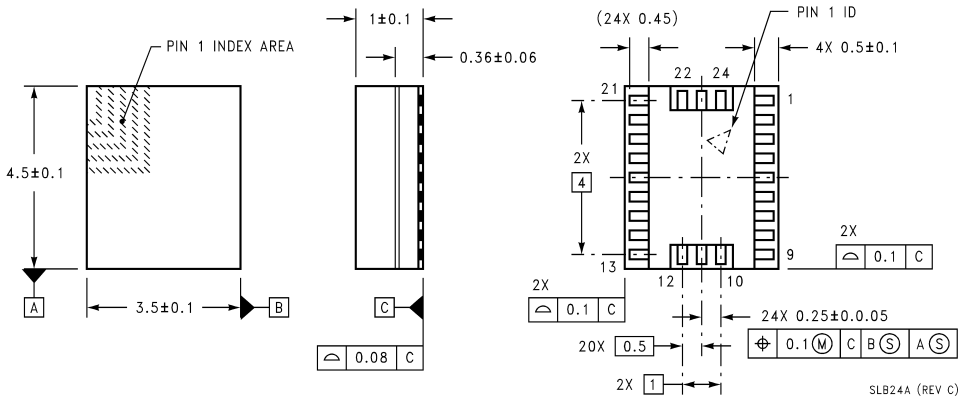

**FIGURE 5. Fastlock PLL Architecture**

## Physical Dimensions inches (millimeters) unless otherwise noted



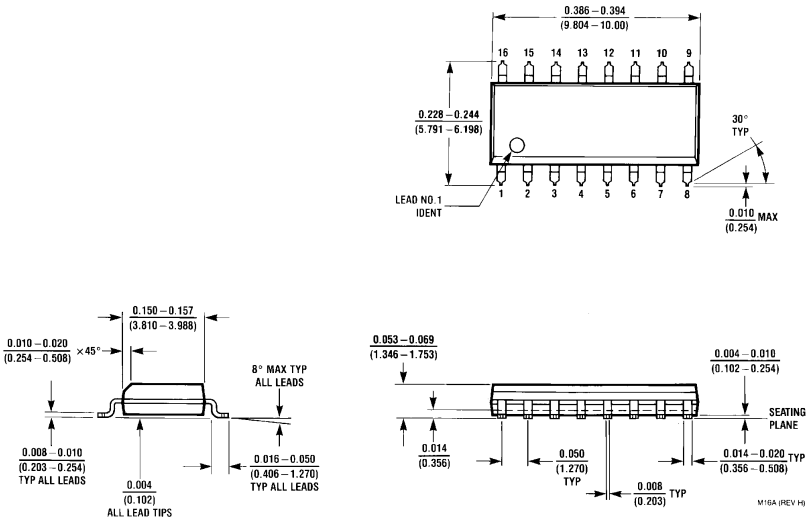

DIMENSIONS ARE IN MILLIMETERS

**RECOMMENDED LAND PATTERN**
1:1 RATIO WITH PACKAGE SOLDER PADS



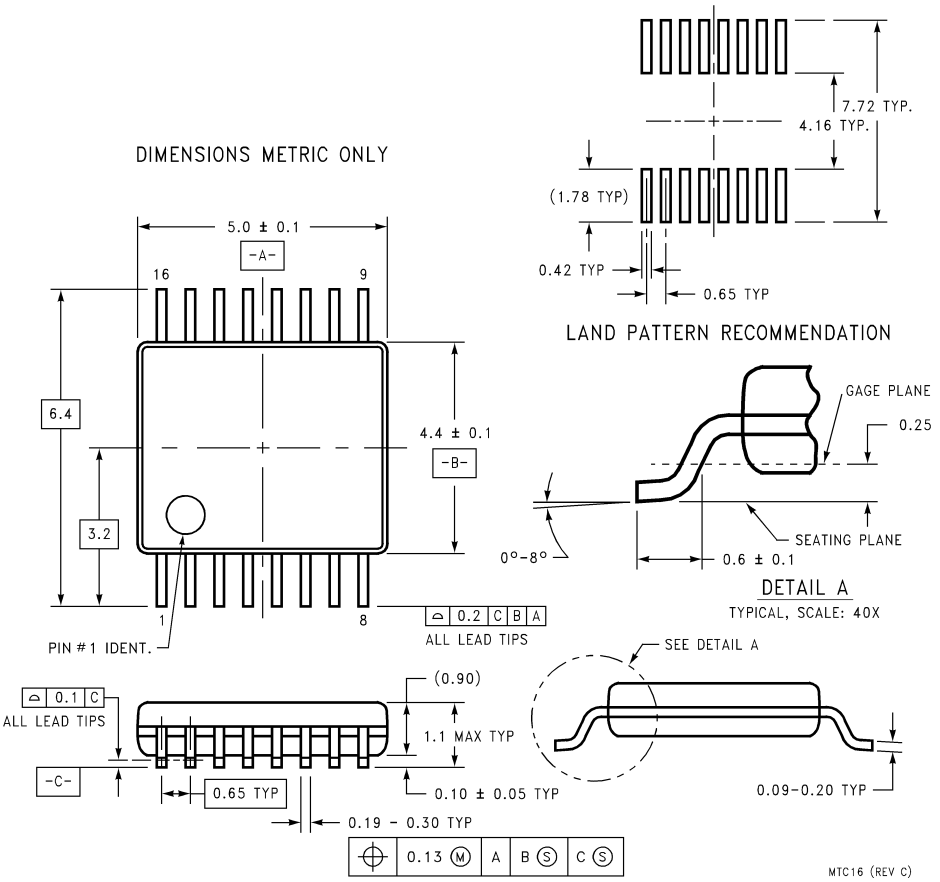

**24-Pin Chip Scale Package**
**Order Number LMX2336LSLB**
***For Tape and Reel (2500 Units Per Reel)**
**Order Number LMX2336LSLBX**
**NS Package Number SLB24A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



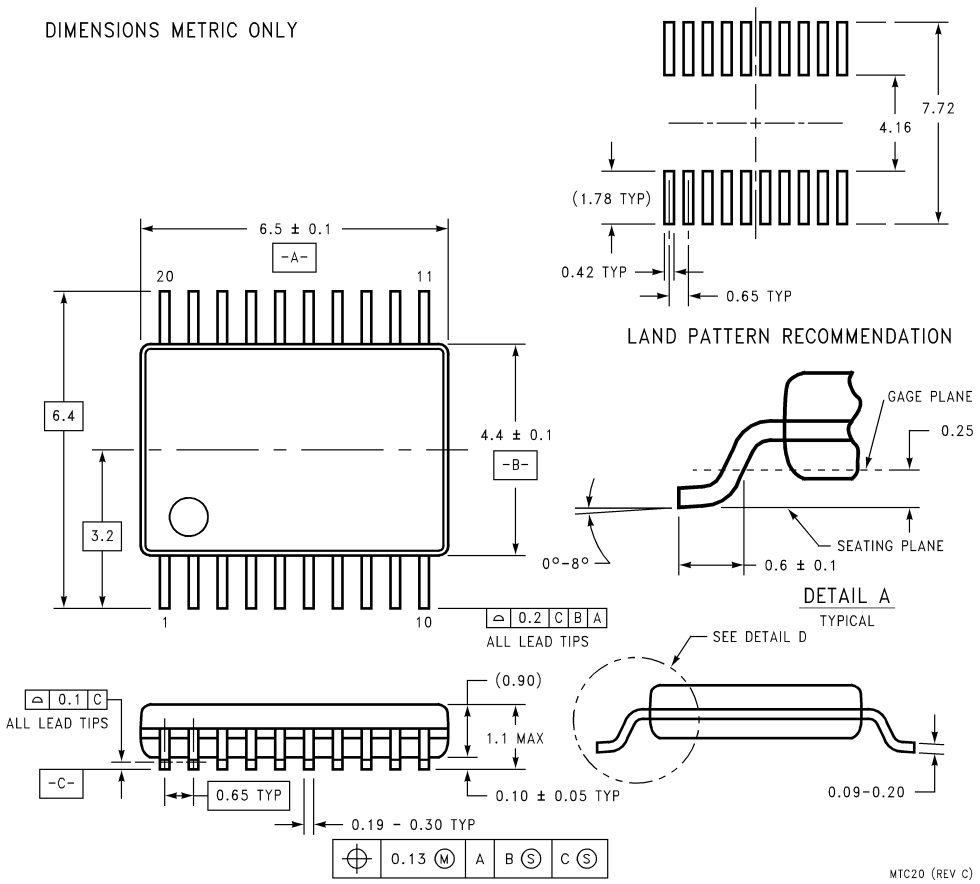

**JEDEC 16-Lead (0.150" Wide) Small Outline Molded Package (M)**
**Order Number LMX2335LM**
***For Tape and Reel (2500 Units Per Reel)**
**Order Number LMX2335LMX**
**NS Package Number M16A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



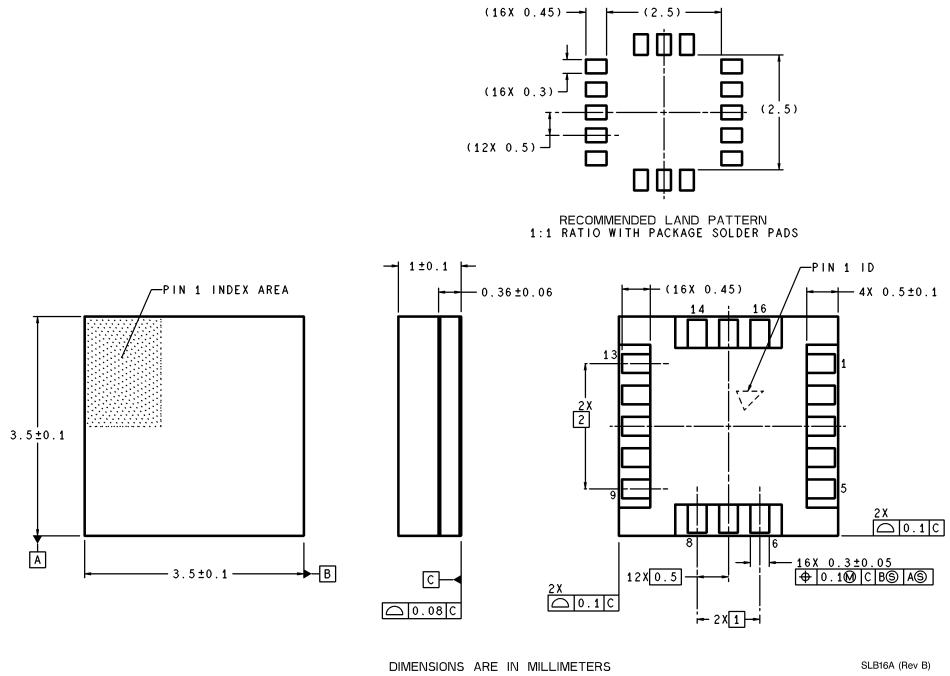

**16-Lead Thin Shrink Small Outline Package (TM)**
**Order Number LMX2335LTM**
***For Tape and Reel (2500 Units Per Reel)**
**Order Number LMX2335LTMX**
**NS Package Number MTC16**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**20-Lead (0.173" Wide) Thin Shrink Small Outline Package (TM)**
**Order Number LMX2336LTM**
***For Tape and Reel (2500 Units Per Reel)**
**Order Number LMX2336LTMX**
**NS Package Number MTC20**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**16-Pin Chip Scale Package**
**Order Number LMX2335LSLB**
***For Tape and Reel (2500 Units Per Reel)**
**Order Number LMX2335LSLBX**
**NS Package Number SLB16A**

### LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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