

- Low Supply-Voltage Range, 1.8 V . . . 3.6 V
- Ultralow-Power Consumption:
 - Active Mode: 200 μ A at 1 MHz, 2.2 V
 - Standby Mode: 0.7 μ A
 - Off Mode (RAM Retention): 0.1 μ A
- Five Power-Saving Modes
- Wake-Up From Standby Mode in less than 6 μ s
- Frequency-Locked Loop, FLL+
- 16-Bit RISC Architecture, 125-ns Instruction Cycle Time
- 16-Bit Timer_A With Three[†] or Five[‡] Capture/Compare Registers
- Integrated LCD Driver for 96 Segments
- On-Chip Comparator
- Brownout Detector
- Supply Voltage Supervisor/Monitor - Programmable Level Detection on MSP430F415/417 devices only
- Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse
- Bootstrap Loader in Flash Devices
- Family Members Include:
 - MSP430C412: 4KB ROM, 256B RAM
 - MSP430C413: 8KB ROM, 256B RAM
 - MSP430F412: 4KB + 256B Flash 256B RAM
 - MSP430F413: 8KB + 256B Flash 256B RAM
 - MSP430F415: 16KB + 256B Flash 512B RAM
 - MSP430F417: 32KB + 256B Flash 1KB RAM
- Available in 64-Pin Quad Flat Pack (QFP) and 64-pin QFN
- For Complete Module Descriptions, Refer to the *MSP430x4xx Family User's Guide*, Literature Number SLAU056

[†] 'x412 and 'x413 devices

[‡] 'F415 and 'F417 devices

description

The Texas Instruments MSP430 family of ultralow power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that attribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6 μ s.

The MSP430x41x series are microcontroller configurations with one or two built-in 16-bit timers, a comparator, 96 LCD segment drive capability, and 48 I/O pins.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and process the data and transmit them to a host system. The comparator and timer make the configurations ideal for industrial meters, counter applications, handheld meters, etc.

AVAILABLE OPTIONS

| T _A | PACKAGED DEVICES | |
|----------------|--|--|
| | PLASTIC 64-PIN QFP (PM) | PLASTIC 64-PIN QFN (RTD) |
| –40°C to 85°C | MSP430C412IPM MSP430C413IPM MSP430F412IPM MSP430F413IPM MSP430F415IPM MSP430F417IPM | MSP430C412IRTD [§] MSP430C413IRTD [§] MSP430F412IRTD MSP430F413IRTD MSP430F415IRTD [§] MSP430F417IRTD [§] |

[§] Preliminary



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



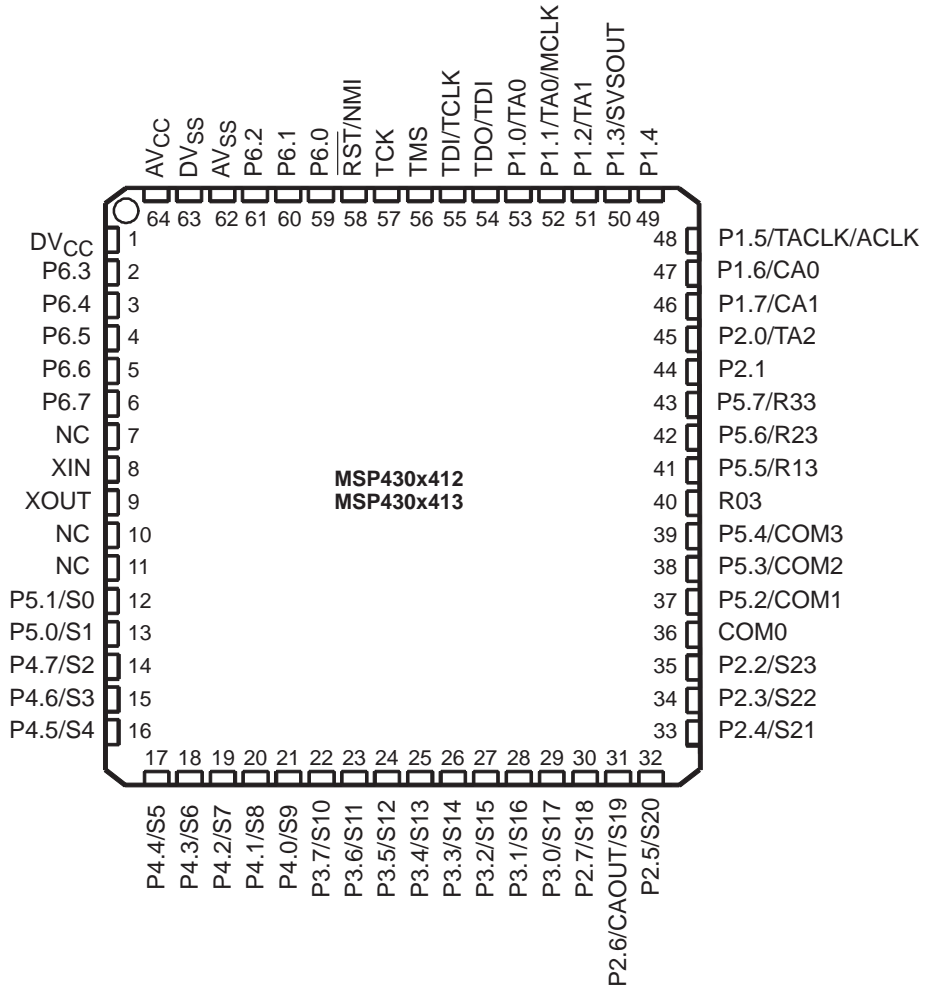
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2001 – 2004, Texas Instruments Incorporated

MSP430x41x MIXED SIGNAL MICROCONTROLLER

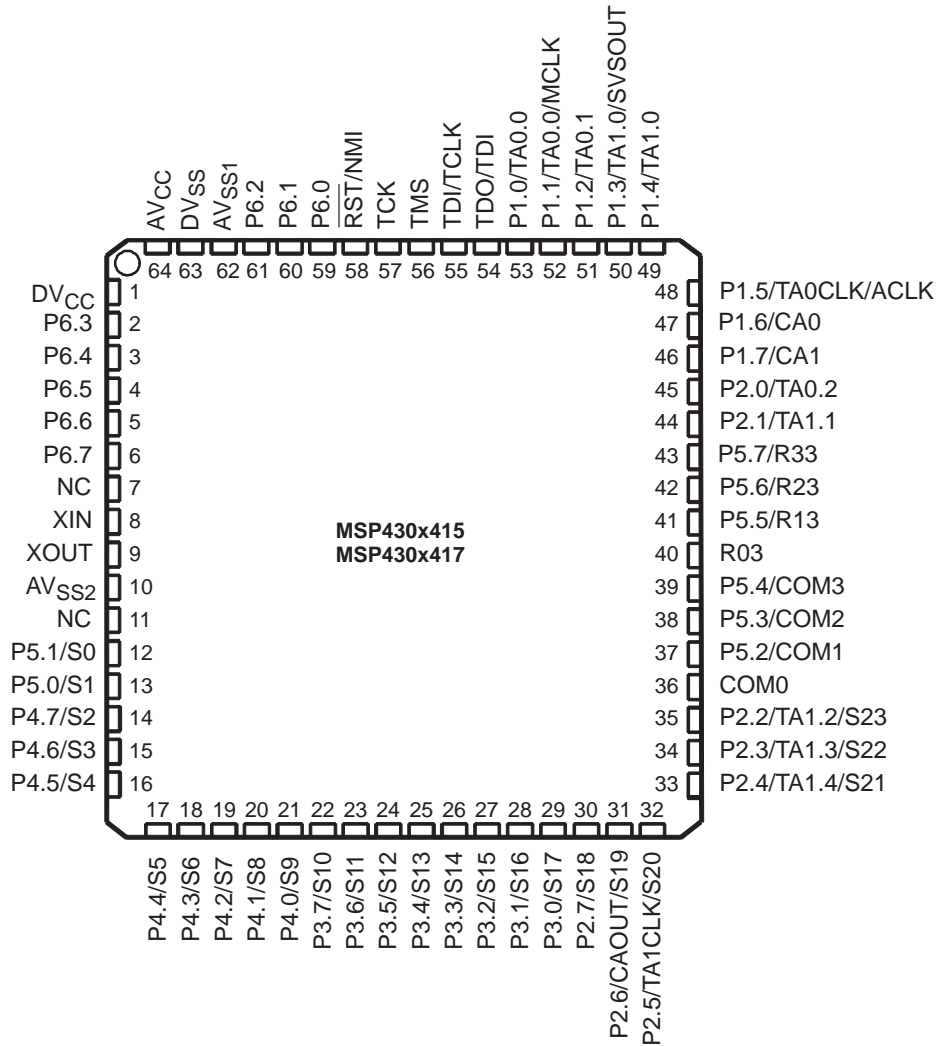
SLAS340G – MAY 2001 – REVISED JUNE 2004

pin designation, MSP430x412, MSP430x413



NC – No internal connection. External connection to V_{SS} recommended.

pin designation, MSP430x415, MSP430x417

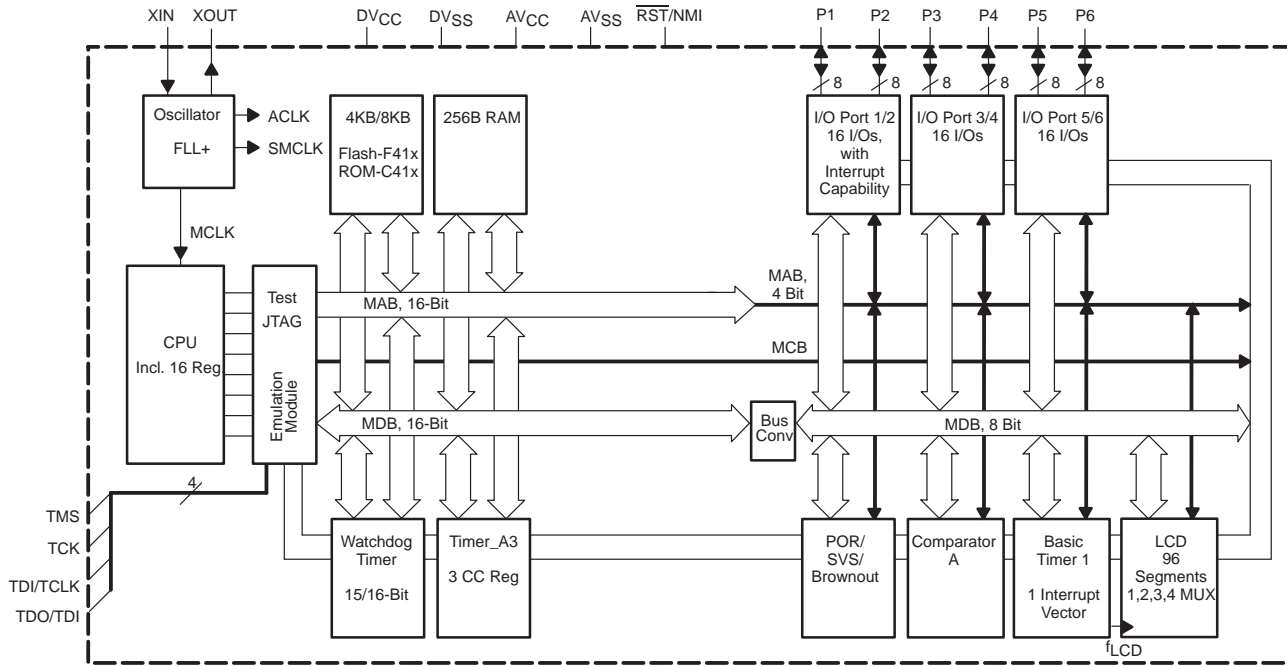


NC – No internal connection. External connection to V_{SS} recommended.

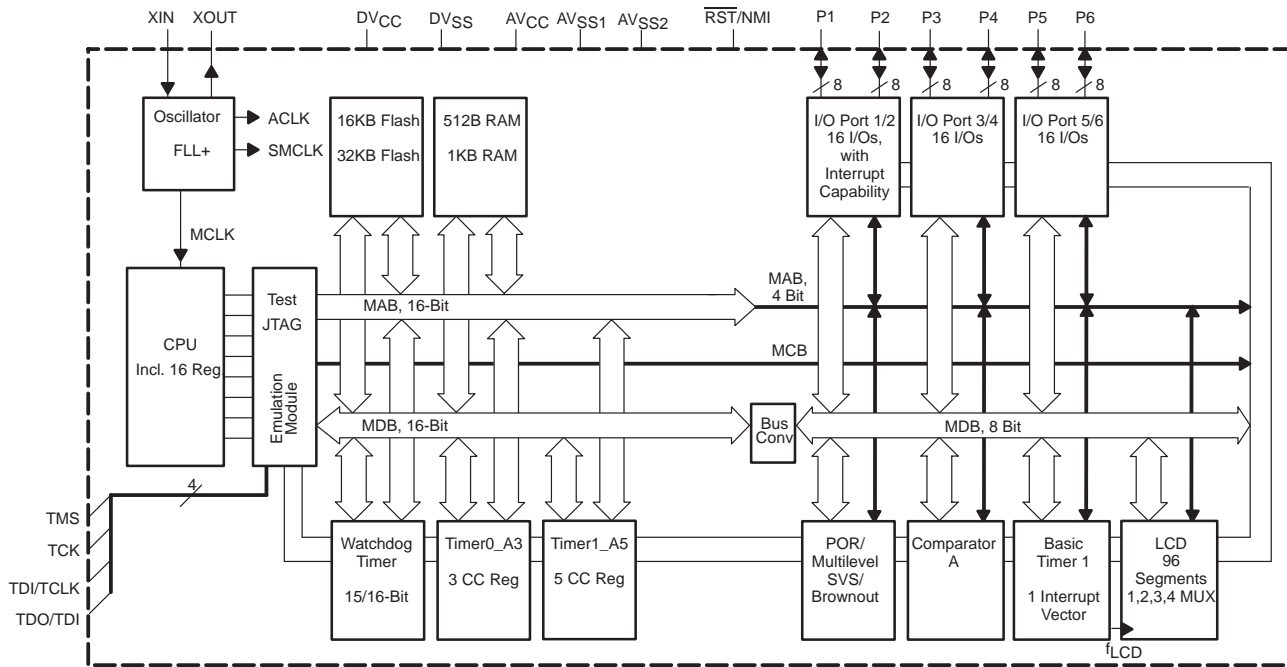
MSP430x41x MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

functional block diagram, MSP430x412, MSP430x413



functional block diagram, MSP430x415, MSP430x417



Terminal Functions

MSP430x412, MSP430x413

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|------------------|-----------|-----|---|
| AV _{CC} | 64 | | Positive terminal that supplies SVS, brownout, oscillator, FLL+, comparator_A, port 1, and LCD resistive divider circuitry; must not power up prior to DV _{CC} . |
| AV _{SS} | 62 | | Negative terminal that supplies SVS, brownout, oscillator, FLL+, comparator_A. Needs to be externally connected to DV _{SS} . |
| DV _{CC} | 1 | | Digital supply voltage, positive terminal. Supplies all parts, except those which are supplied via AV _{CC} . |
| DV _{SS} | 63 | | Digital supply voltage, negative terminal. Supplies all digital parts, except those which are supplied via AV _{CC} /AV _{SS} . |
| NC | 7, 10, 11 | | Not internally connected. Connection to V _{SS} recommended. |
| P1.0/TA0 | 53 | I/O | General-purpose digital I/O/Timer_A. Capture: CCI0A input, compare: Out0 output/BSL transmit |
| P1.1/TA0/MCLK | 52 | I/O | General-purpose digital I/O/Timer_A. Capture: CCI0B input/MCLK output. Note: TA0 is only an input on this pin/BSL receive |
| P1.2/TA1 | 51 | I/O | General-purpose digital I/O/Timer_A, capture: CCI1A input, compare: Out1 output |
| P1.3/SVSOUT | 50 | I/O | General-purpose digital I/O/SVS: output of SVS comparator |
| P1.4 | 49 | I/O | General-purpose digital I/O |
| P1.5/TACLK/ ACLK | 48 | I/O | General-purpose digital I/O/input of Timer_A clock/output of ACLK |
| P1.6/CA0 | 47 | I/O | General-purpose digital I/O/Comparator_A input |
| P1.7/CA1 | 46 | I/O | General-purpose digital I/O/Comparator_A input |
| P2.0/TA2 | 45 | I/O | General-purpose digital I/O/ Timer_A capture: CCI2A input, compare: Out2 output |
| P2.1 | 44 | I/O | General-purpose digital I/O |
| P2.2/S23 | 35 | I/O | General-purpose digital I/O/LCD segment output 23 (see Note 1) |
| P2.3/S22 | 34 | I/O | General-purpose digital I/O/LCD segment output 22 (see Note 1) |
| P2.4/S21 | 33 | I/O | General-purpose digital I/O/LCD segment output 21 (see Note 1) |
| P2.5/S20 | 32 | I/O | General-purpose digital I/O/LCD segment output 20 (see Note 1) |
| P2.6/CAOUT/S19 | 31 | I/O | General-purpose digital I/O/Comparator_A output/LCD segment output 19 (see Note 1) |
| P2.7/S18 | 30 | I/O | General-purpose digital I/O/LCD segment output 18 (see Note 1) |
| P3.0/S17 | 29 | I/O | General-purpose digital I/O/ LCD segment output 17 (see Note 1) |
| P3.1/S16 | 28 | I/O | General-purpose digital I/O/ LCD segment output 16 (see Note 1) |
| P3.2/S15 | 27 | I/O | General-purpose digital I/O/ LCD segment output 15 (see Note 1) |
| P3.3/S14 | 26 | I/O | General-purpose digital I/O/ LCD segment output 14 (see Note 1) |
| P3.4/S13 | 25 | I/O | General-purpose digital I/O/LCD segment output 13 (see Note 1) |
| P3.5/S12 | 24 | I/O | General-purpose digital I/O/LCD segment output 12 (see Note 1) |
| P3.6/S11 | 23 | I/O | General-purpose digital I/O/LCD segment output 11 (see Note 1) |
| P3.7/S10 | 22 | I/O | General-purpose digital I/O/LCD segment output 10 (see Note 1) |

NOTE 1: LCD function selected automatically when applicable LCD module control bits are set, not with PxSEL bits.

MSP430x41x MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

Terminal Functions (Continued)

MSP430x412, MSP430x413 (continued)

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|---------------|-----|-----|---|
| P4.0/S9 | 21 | I/O | General-purpose digital I/O/LCD segment output 9 (see Note 1) |
| P4.1/S8 | 20 | I/O | General-purpose digital I/O/LCD segment output 8 (see Note 1) |
| P4.2/S7 | 19 | I/O | General-purpose digital I/O/LCD segment output 7 (see Note 1) |
| P4.3/S6 | 18 | I/O | General-purpose digital I/O/LCD segment output 6 (see Note 1) |
| P4.4/S5 | 17 | I/O | General-purpose digital I/O/LCD segment output 5 (see Note 1) |
| P4.5/S4 | 16 | I/O | General-purpose digital I/O/LCD segment output 4 (see Note 1) |
| P4.6/S3 | 15 | I/O | General-purpose digital I/O/LCD segment output 3 (see Note 1) |
| P4.7/S2 | 14 | I/O | General-purpose digital I/O/LCD segment output 2 (see Note 1) |
| P5.0/S1 | 13 | I/O | General-purpose digital I/O/LCD segment output 1 (see Note 1) |
| P5.1/S0 | 12 | I/O | General-purpose digital I/O/LCD segment output 0 (see Note 1) |
| COM0 | 36 | O | Common output. COM0–3 are used for LCD backplanes |
| P5.2/COM1 | 37 | I/O | General-purpose digital I/O/common output. COM0–3 are used for LCD backplanes |
| P5.3/COM2 | 38 | I/O | General-purpose digital I/O/common output. COM0–3 are used for LCD backplanes |
| P5.4/COM3 | 39 | I/O | General-purpose digital I/O/common output. COM0–3 are used for LCD backplanes |
| R03 | 40 | I | Input port of fourth positive (lowest) analog LCD level (V5) |
| P5.5/R13 | 41 | I/O | General-purpose digital I/O/input port of third most positive analog LCD level (V4 or V3) |
| P5.6/R23 | 42 | I/O | General-purpose digital I/O/input port of second most positive analog LCD level (V2) |
| P5.7/R33 | 43 | I/O | General-purpose digital I/O/output port of most positive analog LCD level (V1) |
| P6.0 | 59 | I/O | General-purpose digital I/O |
| P6.1 | 60 | I/O | General-purpose digital I/O |
| P6.2 | 61 | I/O | General-purpose digital I/O |
| P6.3 | 2 | I/O | General-purpose digital I/O |
| P6.4 | 3 | I/O | General-purpose digital I/O |
| P6.5 | 4 | I/O | General-purpose digital I/O |
| P6.6 | 5 | I/O | General-purpose digital I/O |
| P6.7 | 6 | I/O | General-purpose digital I/O |
| RST/NMI | 58 | I | Reset input or nonmaskable interrupt input port |
| TCK | 57 | I | Test clock. TCK is the clock input port for device programming and test. |
| TDI/TCLK | 55 | I | Test data input or test clock input. The device protection fuse is connected to TDI. |
| TDO/TDI | 54 | I/O | Test data output port. TDO/TDI data output or programming data input terminal. |
| TMS | 56 | I | Test mode select. TMS is used as an input port for device programming and test. |
| XIN | 8 | I | Input port for crystal oscillator XT1. Standard or watch crystals can be connected. |
| XOUT | 9 | O | Output terminal of crystal oscillator XT1. |
| QFN Pad | NA | NA | QFN package pad connection to V_{SS} recommended. |

NOTE 1: LCD function selected automatically when applicable LCD module control bits are set, not with PxSEL bits.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Terminal Functions (Continued)

MSP430x415, MSP430x417

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|-----------------------|-------|-----|---|
| AV _{CC} | 64 | | Positive terminal that supplies SVS, brownout, oscillator, FLL+, comparator_A, port 1, and LCD resistive divider circuitry; must not power up prior to DV _{CC} . |
| AV _{SS1} | 62 | | Negative terminal that supplies SVS, brownout, oscillator, FLL+, comparator_A. Needs to be externally connected to DV _{SS} . |
| DV _{CC} | 1 | | Digital supply voltage, positive terminal. Supplies all parts, except those which are supplied via AV _{CC} . |
| DV _{SS} | 63 | | Digital supply voltage, negative terminal. Supplies all digital parts, except those which are supplied via AV _{CC} /AV _{SS} . |
| AV _{SS2} | 10 | | Negative terminal that supplies SVS, brownout, oscillator, FLL+, comparator_A. Needs to be externally connected to DV _{SS} . |
| NC | 7, 11 | | Not internally connected. Connection to V _{SS} recommended. |
| P1.0/TA0.0 | 53 | I/O | General-purpose digital I/O/Timer0_A. Capture: CCI0A input, compare: Out0 output/BSL transmit |
| P1.1/TA0.0/MCLK | 52 | I/O | General-purpose digital I/O/Timer0_A. Capture: CCI0B input/MCLK output. Note: TA0 is only an input on this pin/BSL receive |
| P1.2/TA0.1 | 51 | I/O | General-purpose digital I/O/Timer0_A, capture: CCI1A input, compare: Out1 output |
| P1.3/TA1.0/ SVSOUT | 50 | I/O | General-purpose digital I/O/Timer1_A, capture: CCI0B input/SVS: output of SVS comparator |
| P1.4/TA1.0 | 49 | I/O | General-purpose digital I/O/Timer1_A, capture: CCI0A input, compare: Out0 output |
| P1.5/TA0CLK/ ACLK | 48 | I/O | General-purpose digital I/O/input of Timer0_A clock/output of ACLK |
| P1.6/CA0 | 47 | I/O | General-purpose digital I/O/Comparator_A input |
| P1.7/CA1 | 46 | I/O | General-purpose digital I/O/Comparator_A input |
| P2.0/TA0.2 | 45 | I/O | General-purpose digital I/O/ Timer0_A capture: CCI2A input, compare: Out2 output |
| P2.1/TA1.1 | 44 | I/O | General-purpose digital I/O/Timer1_A, capture: CCI1A input, compare: Out1 output |
| P2.2/TA1.2/S23 | 35 | I/O | General-purpose digital I/O/Timer1_A, capture: CCI2A input, compare: Out2 output/LCD segment output 23 (see Note 1) |
| P2.3/TA1.3/S22 | 34 | I/O | General-purpose digital I/O/Timer1_A, capture: CCI3A input, compare: Out3 output/LCD segment output 22 (see Note 1) |
| P2.4/TA1.4/S21 | 33 | I/O | General-purpose digital I/O/Timer1_A, capture: CCI4A input, compare: Out4 output/LCD segment output 21 (see Note 1) |
| P2.5/TA1CLK/S20 | 32 | I/O | General-purpose digital I/O/input of Timer1_A clock/LCD segment output 20 (see Note 1) |
| P2.6/CAOUT/S19 | 31 | I/O | General-purpose digital I/O/Comparator_A output/LCD segment output 19 (see Note 1) |
| P2.7/S18 | 30 | I/O | General-purpose digital I/O/LCD segment output 18 (see Note 1) |
| P3.0/S17 | 29 | I/O | General-purpose digital I/O/ LCD segment output 17 (see Note 1) |
| P3.1/S16 | 28 | I/O | General-purpose digital I/O/ LCD segment output 16 (see Note 1) |
| P3.2/S15 | 27 | I/O | General-purpose digital I/O/ LCD segment output 15 (see Note 1) |
| P3.3/S14 | 26 | I/O | General-purpose digital I/O/ LCD segment output 14 (see Note 1) |
| P3.4/S13 | 25 | I/O | General-purpose digital I/O/LCD segment output 13 (see Note 1) |
| P3.5/S12 | 24 | I/O | General-purpose digital I/O/LCD segment output 12 (see Note 1) |
| P3.6/S11 | 23 | I/O | General-purpose digital I/O/LCD segment output 11 (see Note 1) |
| P3.7/S10 | 22 | I/O | General-purpose digital I/O/LCD segment output 10 (see Note 1) |

NOTE 1: LCD function selected automatically when applicable LCD module control bits are set, not with PxSEL bits.

MSP430x41x MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

Terminal Functions (Continued)

MSP430x415, MSP430x417 (continued)

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|---------------|-----|-----|---|
| P4.0/S9 | 21 | I/O | General-purpose digital I/O/LCD segment output 9 (see Note 1) |
| P4.1/S8 | 20 | I/O | General-purpose digital I/O/LCD segment output 8 (see Note 1) |
| P4.2/S7 | 19 | I/O | General-purpose digital I/O/LCD segment output 7 (see Note 1) |
| P4.3/S6 | 18 | I/O | General-purpose digital I/O/LCD segment output 6 (see Note 1) |
| P4.4/S5 | 17 | I/O | General-purpose digital I/O/LCD segment output 5 (see Note 1) |
| P4.5/S4 | 16 | I/O | General-purpose digital I/O/LCD segment output 4 (see Note 1) |
| P4.6/S3 | 15 | I/O | General-purpose digital I/O/LCD segment output 3 (see Note 1) |
| P4.7/S2 | 14 | I/O | General-purpose digital I/O/LCD segment output 2 (see Note 1) |
| P5.0/S1 | 13 | I/O | General-purpose digital I/O/LCD segment output 1 (see Note 1) |
| P5.1/S0 | 12 | I/O | General-purpose digital I/O/LCD segment output 0 (see Note 1) |
| COM0 | 36 | O | Common output. COM0–3 are used for LCD backplanes |
| P5.2/COM1 | 37 | I/O | General-purpose digital I/O/common output. COM0–3 are used for LCD backplanes |
| P5.3/COM2 | 38 | I/O | General-purpose digital I/O/common output. COM0–3 are used for LCD backplanes |
| P5.4/COM3 | 39 | I/O | General-purpose digital I/O/common output. COM0–3 are used for LCD backplanes |
| R03 | 40 | I | Input port of fourth positive (lowest) analog LCD level (V5) |
| P5.5/R13 | 41 | I/O | General-purpose digital I/O/input port of third most positive analog LCD level (V4 or V3) |
| P5.6/R23 | 42 | I/O | General-purpose digital I/O/input port of second most positive analog LCD level (V2) |
| P5.7/R33 | 43 | I/O | General-purpose digital I/O/output port of most positive analog LCD level (V1) |
| P6.0 | 59 | I/O | General-purpose digital I/O |
| P6.1 | 60 | I/O | General-purpose digital I/O |
| P6.2 | 61 | I/O | General-purpose digital I/O |
| P6.3 | 2 | I/O | General-purpose digital I/O |
| P6.4 | 3 | I/O | General-purpose digital I/O |
| P6.5 | 4 | I/O | General-purpose digital I/O |
| P6.6 | 5 | I/O | General-purpose digital I/O |
| P6.7/SVSIN | 6 | I/O | General-purpose digital I/O/SVS, analog input |
| RST/NMI | 58 | I | Reset input or nonmaskable interrupt input port |
| TCK | 57 | I | Test clock. TCK is the clock input port for device programming and test. |
| TDI/TCLK | 55 | I | Test data input or test clock input. The device protection fuse is connected to TDI. |
| TDO/TDI | 54 | I/O | Test data output port. TDO/TDI data output or programming data input terminal. |
| TMS | 56 | I | Test mode select. TMS is used as an input port for device programming and test. |
| XIN | 8 | I | Input port for crystal oscillator XT1. Standard or watch crystals can be connected. |
| XOUT | 9 | O | Output terminal of crystal oscillator XT1. |
| QFN Pad | NA | NA | QFN package pad connection to V_{SS} recommended. |

NOTE 1: LCD function selected automatically when applicable LCD module control bits are set, not with PxSEL bits.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

short-form description

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

| | |
|--------------------------|-----------|
| Program Counter | PC/R0 |
| Stack Pointer | SP/R1 |
| Status Register | SR/CG1/R2 |
| Constant Generator | CG2/R3 |
| General-Purpose Register | R4 |
| General-Purpose Register | R5 |
| General-Purpose Register | R6 |
| General-Purpose Register | R7 |
| General-Purpose Register | R8 |
| General-Purpose Register | R9 |
| General-Purpose Register | R10 |
| General-Purpose Register | R11 |
| General-Purpose Register | R12 |
| General-Purpose Register | R13 |
| General-Purpose Register | R14 |
| General-Purpose Register | R15 |

Table 1. Instruction Word Formats

| | | |
|-----------------------------------|----------------|-------------------------|
| Dual operands, source-destination | e.g. ADD R4,R5 | R4 + R5 ----> R5 |
| Single operands, destination only | e.g. CALL R8 | PC --->(TOS), R8---> PC |
| Relative jump, un/conditional | e.g. JNE | Jump-on-equal bit = 0 |

Table 2. Address Mode Descriptions

| ADDRESS MODE | S | D | SYNTAX | EXAMPLE | OPERATION |
|------------------------|---|---|-----------------|------------------|-----------------------------------|
| Register | ● | ● | MOV Rs,Rd | MOV R10,R11 | R10 --> R11 |
| Indexed | ● | ● | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6) | M(2+R5)---> M(6+R6) |
| Symbolic (PC relative) | ● | ● | MOV EDE,TONI | | M(EDE) --> M(TONI) |
| Absolute | ● | ● | MOV &MEM,&TCDAT | | M(MEM) --> M(TCDAT) |
| Indirect | ● | | MOV @Rn,Y(Rm) | MOV @R10,Tab(R6) | M(R10) --> M(Tab+R6) |
| Indirect autoincrement | ● | | MOV @Rn+,Rm | MOV @R10+,R11 | M(R10) --> R11 R10 + 2---> R10 |
| Immediate | ● | | MOV #X,TONI | MOV #45,TONI | #45 --> M(TONI) |

NOTE: S = source D = destination

MSP430x41x

MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode AM;
 - All clocks are active
- Low-power mode 0 (LPM0);
 - CPU is disabled
ACLK and SMCLK remain active, MCLK is available to modules
FLL+ Loop control remains active
- Low-power mode 1 (LPM1);
 - CPU is disabled
ACLK and SMCLK remain active, MCLK is available to modules
FLL+ Loop control is disabled
- Low-power mode 2 (LPM2);
 - CPU is disabled
MCLK and FLL+ loop control and DCOCLK are disabled
DCO's dc-generator remains enabled
ACLK remains active
- Low-power mode 3 (LPM3);
 - CPU is disabled
MCLK, FLL+ loop control, and DCOCLK are disabled
DCO's dc-generator is disabled
ACLK remains active
- Low-power mode 4 (LPM4);
 - CPU is disabled
ACLK is disabled
MCLK, FLL+ loop control, and DCOCLK are disabled
DCO's dc-generator is disabled
Crystal oscillator is stopped



interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the ROM with an address range 0FFFFh – 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|--|---|---|--------------|-------------|
| Power-up External Reset Watchdog Flash memory | WDTIFG KEYV (see Note 1) | Reset | 0FFFEh | 15, highest |
| NMI Oscillator Fault Flash memory access violation | NMIIFG (see Notes 1 and 3) OFIFG (see Notes 1 and 3) ACCVIFG (see Notes 1 and 3) | (Non)maskable (Non)maskable (Non)maskable | 0FFFCh | 14 |
| Timer1_A5 (see Note 4) | TA1CCR0 CCIFG (see Note 2) | Maskable | 0FFFAh | 13 |
| Timer1_A5 (see Note 4) | TA1CCR1 to TA1CCR4 CCIFGs and TA1CTL TAIFG (see Notes 1 and 2) | Maskable | 0FFF8h | 12 |
| Comparator_A | CMPAIFG | Maskable | 0FFF6h | 11 |
| Watchdog Timer | WDTIFG | Maskable | 0FFF4h | 10 |
| | | | 0FFF2h | 9 |
| | | | 0FFF0h | 8 |
| | | | 0FFEEh | 7 |
| Timer_A3/Timer0_A3 | TACCR0/TA0CCR0 CCIFG (see Note 2) | Maskable | 0FFECCh | 6 |
| Timer_A3/Timer0_A3 | TACCR1/TA0CCR1 and TACCR2/TA0CCR2 CCIFGs, and TACL1/TA0CTL TAIFG (see Notes 1 and 2) | Maskable | 0FFEAh | 5 |
| I/O port P1 (eight flags) | P1IFG.0 to P1IFG.7 (see Notes 1 and 2) | Maskable | 0FFE8h | 4 |
| | | | 0FFE6h | 3 |
| | | | 0FFE4h | 2 |
| I/O port P2 (eight flags) | P2IFG.0 to P2IFG.7 (see Notes 1 and 2) | Maskable | 0FFE2h | 1 |
| Basic Timer1 | BTIFG | Maskable | 0FFE0h | 0, lowest |

- NOTES:
1. Multiple source flags
 2. Interrupt flags are located in the module.
 3. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt-enable cannot.
 4. Implemented in MSP430x415 and MSP430x417 devices only.

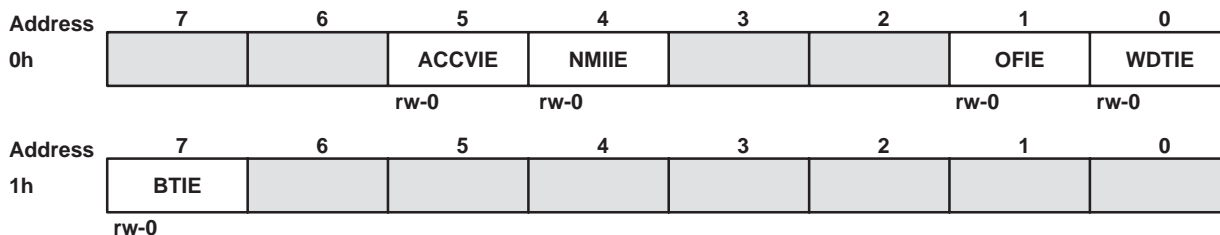
MSP430x41x MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

special function registers

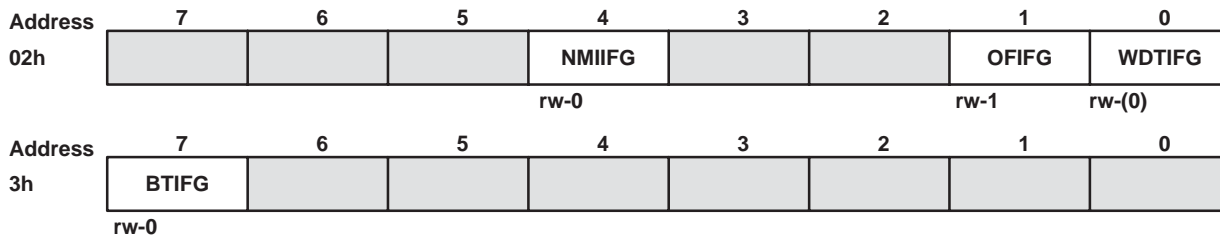
Most interrupt and module enable bits are collected into the lowest address space. Special function register bits that are not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

interrupt enable 1 and 2



- WDTIE: Watchdog-timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.
- OFIE: Oscillator-fault-interrupt enable
- NMIIE: Nonmaskable-interrupt enable
- ACCVIE: Flash access violation interrupt enable
- BTIE: Basic Timer1 interrupt enable

interrupt flag register 1 and 2



- WDTIFG: Set on watchdog-timer overflow (in watchdog mode) or security key violation. Reset with V_{CC} power-up, or a reset condition at the $\overline{RST/NMI}$ pin in reset mode.
- OFIFG: Flag set on oscillator fault
- NMIIFG: Set via $\overline{RST/NMI}$ pin
- BTIFG: Basic Timer1 interrupt flag

module enable registers 1 and 2



- Legend: rw: Bit Can Be Read and Written
 rw-0: Bit Can Be Read and Written. It Is Reset by PUC.
 []: SFR Bit Not Present in Device



memory organization

| | | MSP430F412 | MSP430F413 | MSP430F415 | MSP430F417 |
|--------------------|-----------|---------------------------|---------------------------|---------------------------|-----------------------|
| Memory | Size | 4KB | 8KB | 16KB | 32KB |
| Interrupt vector | Flash | 0FFFFh – 0FFE0h | 0FFFFh – 0FFE0h | 0FFFFh – 0FFE0h | 0FFFFh – 0FFE0h |
| Code memory | Flash | 0FFFFh – 0F000h | 0FFFFh – 0E000h | 0FFFFh – 0C000h | 0FFFFh – 08000h |
| Information memory | Size | 256 Byte | 256 Byte | 256 Byte | 256 Byte |
| | Flash | 010FFh – 01000h | 010FFh – 01000h | 010FFh – 01000h | 010FFh – 01000h |
| Boot memory | Size | 1KB | 1KB | 1KB | 1KB |
| | ROM | 0FFFh – 0C00h | 0FFFh – 0C00h | 0FFFh – 0C00h | 0FFFh – 0C00h |
| RAM | Size | 256 Byte 02FFh – 0200h | 256 Byte 02FFh – 0200h | 512 Byte 03FFh – 0200h | 1 KB 05FFh – 0200h |
| Peripherals | 16-bit | 01FFh – 0100h | 01FFh – 0100h | 01FFh – 0100h | 01FFh – 0100h |
| | 8-bit | 0FFh – 010h | 0FFh – 010h | 0FFh – 010h | 0FFh – 010h |
| | 8-bit SFR | 0Fh – 00h | 0Fh – 00h | 0Fh – 00h | 0Fh – 00h |

| | | MSP430C412 | MSP430C413 |
|--------------------|-----------|---------------------------|---------------------------|
| Memory | Size | 4KB | 8KB |
| Interrupt vector | ROM | 0FFFFh – 0FFE0h | 0FFFFh – 0FFE0h |
| Code memory | ROM | 0FFFFh – 0F000h | 0FFFFh – 0E000h |
| Information memory | Size | NA | NA |
| Boot memory | Size | NA | NA |
| RAM | Size | 256 Byte 02FFh – 0200h | 256 Byte 02FFh – 0200h |
| Peripherals | 16-bit | 01FFh – 0100h | 01FFh – 0100h |
| | 8-bit | 0FFh – 010h | 0FFh – 010h |
| | 8-bit SFR | 0Fh – 00h | 0Fh – 00h |

bootstrap loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the Application report *Features of the MSP430 Bootstrap Loader*, Literature Number SLAA089.

| BSL Function | PM, RTD Package Pins |
|---------------|----------------------|
| Data Transmit | 53 - P1.0 |
| Data Receive | 52 - P1.1 |

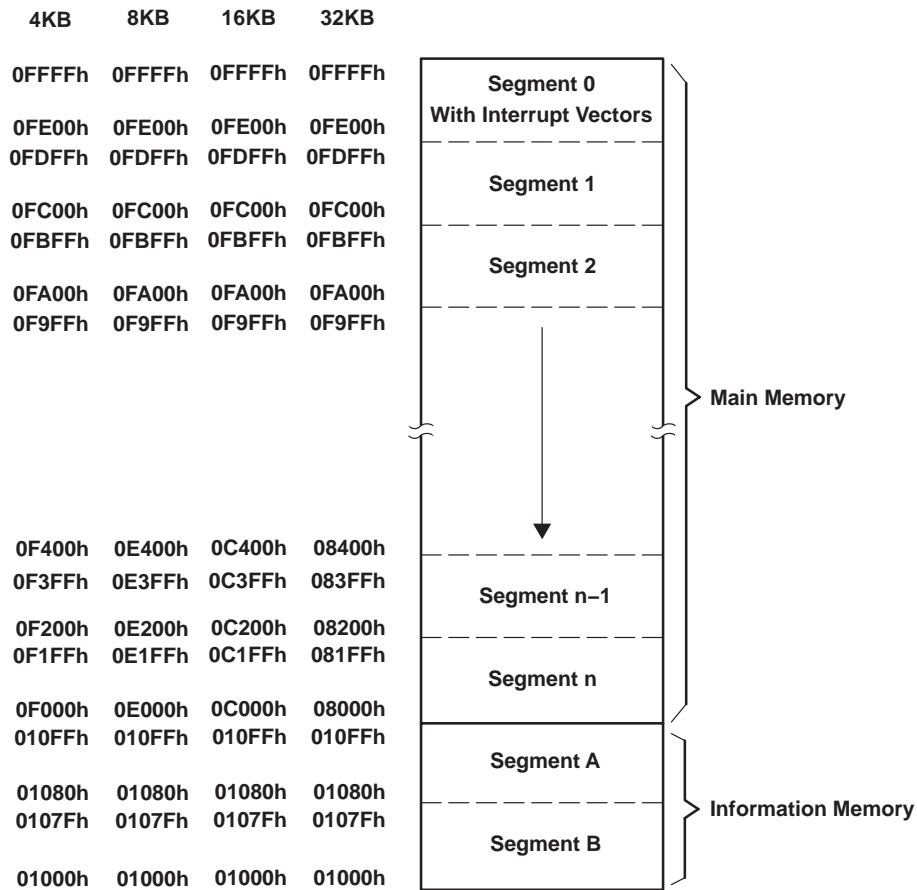
MSP430x41x MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0–n. Segments A and B are also called *information memory*.
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.



peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, refer to the *MSP430x4xx Family User's Guide*, literature number SLAU056.

oscillator and system clock

The clock system in the MSP430x41x family of devices is supported by the FLL+ module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and a high frequency crystal oscillator. The FLL+ clock module is designed to meet the requirements of both low system cost and low-power consumption. The FLL+ features a digital frequency locked loop (FLL) hardware which in conjunction with a digital modulator stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 μ s. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high frequency crystal.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8.

brownout, supply voltage supervisor

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The supply voltage supervisor (SVS) circuitry detects if the supply voltage drops below a fixed level or user selectable level (MSP430x415 & MSP430x417 only) and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must insure the default FLL+ settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

digital I/O

There are six 8-bit I/O ports implemented—ports P1 through P6:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.

Basic Timer1

The Basic Timer1 has two independent 8-bit timers which can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. The Basic Timer1 can be used to generate periodic interrupts and clock for the LCD module.

LCD drive

The LCD driver generates the segment and common signals required to drive an LCD display. The LCD controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral.

MSP430x41x MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

watchdog timer

The primary function of the watchdog timer (WDT) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

comparator_A

The primary function of the comparator_A module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

timer_A3/timer0_A3

Timer_A3/Timer0_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3/Timer0_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3/Timer0_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

| Timer_A3/Timer0_A3 Signal Connections | | | | | |
|---------------------------------------|----------------------------------|-------------------|--------------|----------------------|-------------------|
| Input Pin Number | Device Input Signal | Module Input Name | Module Block | Module Output Signal | Output Pin Number |
| 48 - P1.5 | TACLK/TA0CLK | TACLK | Timer | NA | |
| | ACLK | ACLK | | | |
| | SMCLK | SMCLK | | | |
| 48 - P1.5 | $\overline{\text{TACLK/TA0CLK}}$ | INCLK | | | |
| 53 - P1.0 | TA0/TA0.0 | CCI0A | CCR0 | TA0/TA0.0 | 53 - P1.0 |
| 52 - P1.1 | TA0/TA0.0 | CCI0B | | | |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |
| 51 - P1.2 | TA1/TA0.1 | CCI1A | CCR1 | TA1/TA0.1 | 51 - P1.2 |
| | CAOUT (internal) | CCI1B | | | |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |
| 45 - P2.0 | TA2/TA0.2 | CCI2A | CCR2 | TA2/TA0.2 | 45 - P2.0 |
| | ACLK (internal) | CCI2B | | | |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |

timer1_A5 (MSP430x415 and MSP430x417 only)

Timer1_A5 is a 16-bit timer/counter with five capture/compare registers. Timer1_A5 can support multiple capture/compares, PWM outputs, and interval timing. Timer1_A5 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

| Timer1_A5 Signal Connections | | | | | |
|------------------------------|----------------------------|-------------------|--------------|----------------------|-------------------|
| Input Pin Number | Device Input Signal | Module Input Name | Module Block | Module Output Signal | Output Pin Number |
| 32 - P2.5 | TA1CLK | TACLK | Timer | NA | |
| | ACLK | ACLK | | | |
| | SMCLK | SMCLK | | | |
| 32 - P2.5 | $\overline{\text{TA1CLK}}$ | INCLK | | | |
| 49 - P1.4 | TA1.0 | CCI0A | CCR0 | TA1.0 | 49 - P1.4 |
| 50 - P1.3 | TA1.0 | CCI0B | | | |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |
| 44 - P2.1 | TA1.1 | CCI1A | CCR1 | TA1.1 | 44 - P2.1 |
| | CAOUT (internal) | CCI1B | | | |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |
| 35 - P2.2 | TA1.2 | CCI2A | CCR2 | TA1.2 | 35 - P2.2 |
| | Not Connected | CCI2B | | | |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |
| 34 - P2.3 | TA1.3 | CCI3A | CCR3 | TA1.3 | 34 - P2.3 |
| | Not Connected | CCI3B | | | |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |
| 33 - P2.4 | TA1.4 | CCI4A | CCR4 | TA1.4 | 33 - P2.4 |
| | Not Connected | CCI4B | | | |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |

MSP430x41x MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

peripheral file map

| PERIPHERALS WITH WORD ACCESS | | | |
|---|-----------------------------------|------------------|-------|
| Watchdog | Watchdog Timer control | WDTCTL | 0120h |
| Timer1_A5 (MSP430x415 and MSP430x417 only) | Timer1_A interrupt vector | TA1IV | 011Eh |
| | Timer1_A control | TA1CTL | 0180h |
| | Capture/compare control 0 | TA1CCTL0 | 0182h |
| | Capture/compare control 1 | TA1CCTL1 | 0184h |
| | Capture/compare control 2 | TA1CCTL2 | 0186h |
| | Capture/compare control 3 | TA1CCTL3 | 0188h |
| | Capture/compare control 4 | TA1CCTL4 | 018Ah |
| | Reserved | | 018Ch |
| | Reserved | | 018Eh |
| | Timer1_A register | TA1R | 0190h |
| | Capture/compare register 0 | TA1CCR0 | 0192h |
| | Capture/compare register 1 | TA1CCR1 | 0194h |
| | Capture/compare register 2 | TA1CCR2 | 0196h |
| | Capture/compare register 3 | TA1CCR3 | 0198h |
| | Capture/compare register 4 | TA1CCR4 | 019Ah |
| | Reserved | | 019Ch |
| Reserved | | 019Eh | |
| Timer_A3/Timer0_A3 | Timer_A/Timer0_A interrupt vector | TAIV/TA0IV | 012Eh |
| | Timer_A/Timer0_A control | TACTL/TA0CTL | 0160h |
| | Capture/compare control 0 | TACCTL0/TA0CCTL0 | 0162h |
| | Capture/compare control 1 | TACCTL1/TA0CCTL1 | 0164h |
| | Capture/compare control 2 | TACCTL2/TA0CCTL2 | 0166h |
| | Reserved | | 0168h |
| | Reserved | | 016Ah |
| | Reserved | | 016Ch |
| | Reserved | | 016Eh |
| | Timer_A/Timer0_A register | TAR/TA0R | 0170h |
| | Capture/compare register 0 | TACCR0/TA0CCR0 | 0172h |
| | Capture/compare register 1 | TACCR1/TA0CCR1 | 0174h |
| | Capture/compare register 2 | TACCR2/TA0CCR2 | 0176h |
| | Reserved | | 0178h |
| | Reserved | | 017Ah |
| | Reserved | | 017Ch |
| Reserved | | 017Eh | |
| Flash | Flash control 3 | FCTL3 | 012Ch |
| | Flash control 2 | FCTL2 | 012Ah |
| | Flash control 1 | FCTL1 | 0128h |



peripheral file map (continued)

| PERIPHERALS WITH BYTE ACCESS | | | |
|-------------------------------------|-----------------------------------|----------|------|
| LCD | LCD memory 20 | LCDM20 | 0A4h |
| | : | : | : |
| | LCD memory 16 | LCDM16 | 0A0h |
| | LCD memory 15 | LCDM15 | 09Fh |
| | : | : | : |
| | LCD memory 1 | LCDM1 | 091h |
| | LCD control and mode | LCDCTL | 090h |
| Comparator_A | Comparator_A port disable | CAPD | 05Bh |
| | Comparator_A control2 | CACTL2 | 05Ah |
| | Comparator_A control1 | CACTL1 | 059h |
| Brownout, SVS | SVS control register | SVSCTL | 056h |
| FLL+ Clock | FLL+ Control1 | FLL_CTL1 | 054h |
| | FLL+ Control0 | FLL_CTL0 | 053h |
| | System clock frequency control | SCFQCTL | 052h |
| | System clock frequency integrator | SCFI1 | 051h |
| | System clock frequency integrator | SCFI0 | 050h |
| Basic Timer1 | BT counter2 | BTCNT2 | 047h |
| | BT counter1 | BTCNT1 | 046h |
| | BT control | BTCTL | 040h |
| Port P6 | Port P6 selection | P6SEL | 037h |
| | Port P6 direction | P6DIR | 036h |
| | Port P6 output | P6OUT | 035h |
| | Port P6 input | P6IN | 034h |
| Port P5 | Port P5 selection | P5SEL | 033h |
| | Port P5 direction | P5DIR | 032h |
| | Port P5 output | P5OUT | 031h |
| | Port P5 input | P5IN | 030h |
| Port P4 | Port P4 selection | P4SEL | 01Fh |
| | Port P4 direction | P4DIR | 01Eh |
| | Port P4 output | P4OUT | 01Dh |
| | Port P4 input | P4IN | 01Ch |
| Port P3 | Port P3 selection | P3SEL | 01Bh |
| | Port P3 direction | P3DIR | 01Ah |
| | Port P3 output | P3OUT | 019h |
| | Port P3 input | P3IN | 018h |
| Port P2 | Port P2 selection | P2SEL | 02Eh |
| | Port P2 interrupt enable | P2IE | 02Dh |
| | Port P2 interrupt-edge select | P2IES | 02Ch |
| | Port P2 interrupt flag | P2IFG | 02Bh |
| | Port P2 direction | P2DIR | 02Ah |
| | Port P2 output | P2OUT | 029h |
| | Port P2 input | P2IN | 028h |

MSP430x41x MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

peripheral file map (continued)

| PERIPHERALS WITH BYTE ACCESS (CONTINUED) | | | |
|--|-------------------------------|-------|------|
| Port P1 | Port P1 selection | P1SEL | 026h |
| | Port P1 interrupt enable | P1IE | 025h |
| | Port P1 interrupt-edge select | P1IES | 024h |
| | Port P1 interrupt flag | P1IFG | 023h |
| | Port P1 direction | P1DIR | 022h |
| | Port P1 output | P1OUT | 021h |
| | Port P1 input | P1IN | 020h |
| Special Functions | SFR module enable 2 | ME2 | 005h |
| | SFR module enable 1 | ME1 | 004h |
| | SFR interrupt flag2 | IFG2 | 003h |
| | SFR interrupt flag1 | IFG1 | 002h |
| | SFR interrupt enable2 | IE2 | 001h |
| | SFR interrupt enable1 | IE1 | 000h |

absolute maximum ratings†

| | |
|---|----------------------------|
| Voltage applied at V_{CC} to V_{SS} | -0.3 V to + 4.1 V |
| Voltage applied to any pin (see Note) | -0.3 V to $V_{CC} + 0.3$ V |
| Diode current at any device terminal | ± 2 mA |
| Storage temperature (unprogrammed device) | -55°C to 150°C |
| Storage temperature (programmed device) | -40°C to 85°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to V_{SS} . The JTAG fuse-blow voltage, V_{FB} , is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.



recommended operating conditions

| PARAMETER | | MIN | NOM | MAX | UNITS | |
|---|-------------------------|-------------------|-----|-------|-------|-----|
| Supply voltage during program execution, SVS disabled V_{CC} ($AV_{CC} = DV_{CC} = V_{CC}$) | MSP430x41x | 1.8 | | 3.6 | V | |
| Supply voltage during program execution, SVS enabled (see Note 1), V_{CC} ($AV_{CC} = DV_{CC} = V_{CC}$) | MSP430x41x | 2.2 | | 3.6 | V | |
| Supply voltage during programming of flash memory, V_{CC} ($AV_{CC} = DV_{CC} = V_{CC}$) | MSP430F41x | 2.7 | | 3.6 | V | |
| Supply voltage, V_{SS} ($AV_{SS}/1/2 = DV_{SS} = V_{SS}$) | | 0 | | 0 | V | |
| Operating free-air temperature range, T_A | MSP430x41x | -40 | | 85 | °C | |
| LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Note 2) | LF selected, XTS_FLL=0 | Watch crystal | | 32768 | Hz | |
| | XT1 selected, XTS_FLL=1 | Ceramic resonator | | 450 | 8000 | kHz |
| | XT1 selected, XTS_FLL=1 | Crystal | | 1000 | 8000 | kHz |
| Processor frequency (signal MCLK), $f_{(System)}$ | $V_{CC} = 1.8$ V | DC | | 4.15 | MHz | |
| | $V_{CC} = 3.6$ V | DC | | 8 | | |

- NOTES: 1. The minimum operating supply voltage is defined according to the trip point where POR is going active by decreasing supply voltage. POR is going inactive when the supply voltage is raised above minimum supply voltage plus the hysteresis of the SVS circuitry.
2. The LFXT1 oscillator in LF-mode requires a watch crystal.

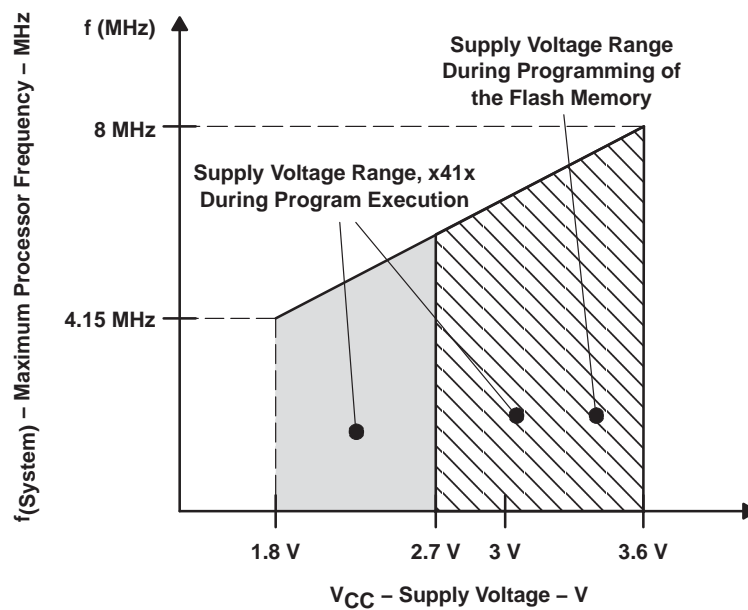


Figure 1. Frequency vs Supply Voltage

MSP430x41x MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

supply current into $AV_{CC} + DV_{CC}$ excluding external current, (see Note 1)

| PARAMETER | | TEST CONDITIONS | | MIN | NOM | MAX | UNIT | |
|--------------|---|-----------------|---|--------------------------------------|---------------------------|------|---------------|---------------|
| $I_{(AM)}$ | Active mode, $f_{(MCLK)} = f_{(SMCLK)} = 1 \text{ MHz}$, $f_{(ACLK)} = 32,768 \text{ Hz}$, XTS_FLL = 0 (F41x: Program executes in flash) | C41x | $T_A = -40^\circ\text{C}$ to 85°C | $V_{CC} = 2.2 \text{ V}$ | 160 | 200 | μA | |
| | | | | $V_{CC} = 3 \text{ V}$ | 240 | 300 | | |
| | | F41x | | $V_{CC} = 2.2 \text{ V}$ | 200 | 250 | | |
| | | | | $V_{CC} = 3 \text{ V}$ | 300 | 350 | | |
| $I_{(LPM0)}$ | Low-power mode, (LPM0) $f_{(MCLK)} = f_{(SMCLK)} = 0.5 \text{ MHz}$, $f_{(ACLK)} = 32,768 \text{ Hz}$, XTS_FLL = 0 FN_8=FN_4=FN_3=FN_2=0 | C41x | $T_A = -40^\circ\text{C}$ to 85°C | $V_{CC} = 2.2 \text{ V}$ | 32 | 45 | μA | |
| | | | | $V_{CC} = 3 \text{ V}$ | 55 | 70 | | |
| $I_{(LPM0)}$ | Low-power mode, (LPM0) $f_{(MCLK)} = f_{(SMCLK)} = 1 \text{ MHz}$, $f_{(ACLK)} = 32,768 \text{ Hz}$, XTS_FLL = 0 FN_8=FN_4=FN_3=FN_2=0 | F41x | $T_A = -40^\circ\text{C}$ to 85°C | $V_{CC} = 2.2 \text{ V}$ | 57 | 70 | μA | |
| | | | | $V_{CC} = 3 \text{ V}$ | 92 | 100 | | |
| $I_{(LPM2)}$ | Low-power mode, (LPM2) | | $T_A = -40^\circ\text{C}$ to 85°C | $V_{CC} = 2.2 \text{ V}$ | 11 | 14 | μA | |
| | | | | $V_{CC} = 3 \text{ V}$ | 17 | 22 | | |
| $I_{(LPM3)}$ | Low-power mode, (LPM3) (see Note 2) | | $T_A = -40^\circ\text{C}$ to 85°C | $V_{CC} = 2.2 \text{ V}$ | $T_A = -40^\circ\text{C}$ | 0.95 | 1.4 | μA |
| | | | | | $T_A = -10^\circ\text{C}$ | 0.8 | 1.3 | |
| | | | | | $T_A = 25^\circ\text{C}$ | 0.7 | 1.2 | |
| | | | | | $T_A = 60^\circ\text{C}$ | 0.95 | 1.4 | |
| | | | | | $T_A = 85^\circ\text{C}$ | 1.6 | 2.3 | |
| | | | | $V_{CC} = 3 \text{ V}$ | $T_A = -40^\circ\text{C}$ | 1.1 | 1.7 | |
| | | | | | $T_A = -10^\circ\text{C}$ | 1.0 | 1.6 | |
| | | | | | $T_A = 25^\circ\text{C}$ | 0.9 | 1.5 | |
| | | | | | $T_A = 60^\circ\text{C}$ | 1.1 | 1.7 | |
| | | | | | $T_A = 85^\circ\text{C}$ | 2.0 | 2.6 | |
| $I_{(LPM4)}$ | Low-power mode, (LPM4) | | $T_A = -40^\circ\text{C}$ to 85°C | $V_{CC} = 2.2 \text{ V}/3 \text{ V}$ | $T_A = -40^\circ\text{C}$ | 0.1 | 0.5 | μA |
| | | | | | $T_A = 25^\circ\text{C}$ | 0.1 | 0.5 | |
| | | | | | $T_A = 85^\circ\text{C}$ | 0.8 | 2.5 | |

- NOTES: 1. All inputs are tied to 0 V or V_{CC} . Outputs do not source or sink any current. The current consumption is measured with active Basic Timer1 and LCD (ACLK selected).
The current consumption of the Comparator_A and the SVS module are specified in the respective sections.
2. The LPM3 currents are characterized with a KDS Daishinku DT-38 (6 pF) crystal.

current consumption of active mode versus system frequency, F version

$$I_{(AM)} = I_{(AM)} [1 \text{ MHz}] \times f_{(\text{System})} [\text{MHz}]$$

current consumption of active mode versus supply voltage, F version

$$I_{(AM)} = I_{(AM)} [3 \text{ V}] + 140 \mu\text{A/V} \times (V_{CC} - 3 \text{ V})$$

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Schmitt-trigger inputs – Ports P1, P2, P3, P4, P5, and P6

| PARAMETER | | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------|---|-----------------|------|-----|-----|------|
| V _{IT+} | Positive-going input threshold voltage | 2.2 V | 1.1 | | 1.5 | V |
| | | 3 V | 1.5 | | 1.9 | |
| V _{IT-} | Negative-going input threshold voltage | 2.2 V | 0.4 | | 0.9 | V |
| | | 3 V | 0.9 | | 1.3 | |
| V _{hys} | Input voltage hysteresis (V _{IT+} – V _{IT-}) | 2.2 V | 0.3 | | 1.1 | V |
| | | 3 V | 0.45 | | 1 | |

standard inputs – \overline{RST}/NMI ; JTAG: TCK, TMS, TDI/TCLK, TDO/TDI

| PARAMETER | | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------|--------------------------|-----------------|---------------------|-----|----------------------|------|
| V _{IL} | Low-level input voltage | 2.2 V/3 V | V _{SS} | | V _{SS} +0.6 | V |
| V _{IH} | High-level input voltage | | 0.8×V _{CC} | | V _{CC} | V |

inputs P_{x.x}, TAx/TAx.x

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------------|---|---|-----------------|-----|-----|-----|-------|
| t _(int) | External interrupt timing | Port P1, P2: P1.x to P2.x, External trigger signal for the interrupt flag, (see Note 1) | 2.2 V/3 V | 1.5 | | | cycle |
| | | | 2.2 V | 62 | | | ns |
| | | | 3 V | 50 | | | |
| t _(cap) | Timer_A, capture timing | TAx/TAx.y | 2.2 V | 62 | | | ns |
| | | | 3 V | 50 | | | |
| f _(TAext) | Timer_A clock frequency externally applied to pin | TACLK/TAxCLK, INCLK t _(H) = t _(L) | 2.2 V | | | 8 | MHz |
| | | | 3 V | | | 10 | |
| f _(TAint) | Timer_A clock frequency | SMCLK or ACLK signal selected | 2.2 V | | | 8 | MHz |
| | | | 3 V | | | 10 | |

NOTES: 1. The external signal sets the interrupt flag every time the minimum t_(int) cycle and time parameters are met. It may be set even with trigger signals shorter than t_(int). Both the cycle and timing specifications must be met to ensure the flag is set. t_(int) is measured in MCLK cycles.

leakage current (see Note 1)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | NOM | MAX | UNIT |
|-------------------------|-----------------|-----------------|-----------------|-----|-----|-----|------|
| I _{lkg} (P1.x) | Leakage current | Port P1 | 2.2 V/3 V | | | ±50 | nA |
| I _{lkg} (P6.x) | | Port P6 | | | | ±50 | |

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as an input.

MSP430x41x MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs – Ports P1, P2, P3, P4, P5, and P6

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|-----------------------|-----|-----------------------|------|
| V _{OH} High-level output voltage | I _{OH(max)} = -1.5 mA, V _{CC} = 2.2 V, See Note 1 | V _{CC} -0.25 | | V _{CC} | V |
| | I _{OH(max)} = -6 mA, V _{CC} = 2.2 V, See Note 2 | V _{CC} -0.6 | | V _{CC} | |
| | I _{OH(max)} = -1.5 mA, V _{CC} = 3 V, See Note 1 | V _{CC} -0.25 | | V _{CC} | |
| | I _{OH(max)} = -6 mA, V _{CC} = 3 V, See Note 2 | V _{CC} -0.6 | | V _{CC} | |
| V _{OL} Low-level output voltage | I _{OL(max)} = 1.5 mA, V _{CC} = 2.2 V, See Note 1 | V _{SS} | | V _{SS} +0.25 | V |
| | I _{OL(max)} = 6 mA, V _{CC} = 2.2 V, See Note 2 | V _{SS} | | V _{SS} +0.6 | |
| | I _{OL(max)} = 1.5 mA, V _{CC} = 3 V, See Note 1 | V _{SS} | | V _{SS} +0.25 | |
| | I _{OL(max)} = 6 mA, V _{CC} = 3 V, See Note 2 | V _{SS} | | V _{SS} +0.6 | |

- NOTES: 1. The maximum total current, I_{OH(max)} and I_{OL(max)}, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.
 2. The maximum total current, I_{OH(max)} and I_{OL(max)}, for all outputs combined, should not exceed ±24 mA to satisfy the maximum specified voltage drop.

output frequency

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---------------|---------------|---------------|
| f _{Px.y} (1 ≤ x ≤ 6, 0 ≤ y ≤ 7) | C _L = 20 pF, I _L = ±1.5mA | V _{CC} = 2.2 V | DC | 10 | MHz |
| | | V _{CC} = 3 V | DC | 12 | |
| f _{ACLK} , f _{MCLK} , f _{SMCLK} P1.1/TA0/MCLK, P1.5/TACLK/ACLK | C _L = 20 pF | V _{CC} = 2.2 V | | 8 | MHz |
| | | V _{CC} = 3 V | | 12 | |
| t _{Xdc} Duty cycle of output frequency | P1.5/TACLK/ACLK, C _L = 20 pF V _{CC} = 2.2 V / 3 V | f _{ACLK} = f _{LFXT1} = f _{XT1} | 40% | 60% | |
| | | f _{ACLK} = f _{LFXT1} = f _{LF} | 30% | 70% | |
| | | f _{ACLK} = f _{LFXT1} /n | 50% | | |
| | P1.1/TA0/MCLK, C _L = 20 pF, V _{CC} = 2.2 V / 3 V | f _{MCLK} = f _{LFXT1} /n | 50%– 15 ns | 50% | 50%+ 15 ns |
| f _{MCLK} = f _{DCOCLK} | | 50%– 15 ns | 50% | 50%+ 15 ns | |



electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

MSP430x412, MSP430x413 outputs – Ports P1, P2, P3, P4, P5, and P6 (see Note)

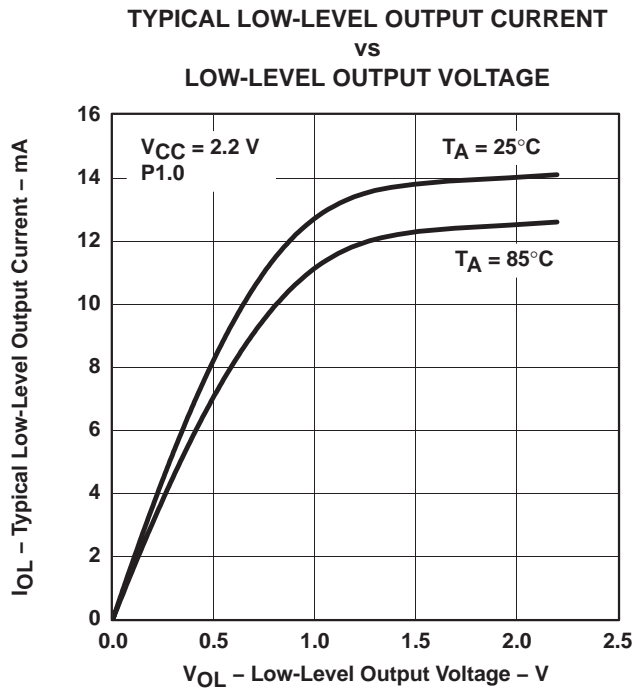


Figure 2

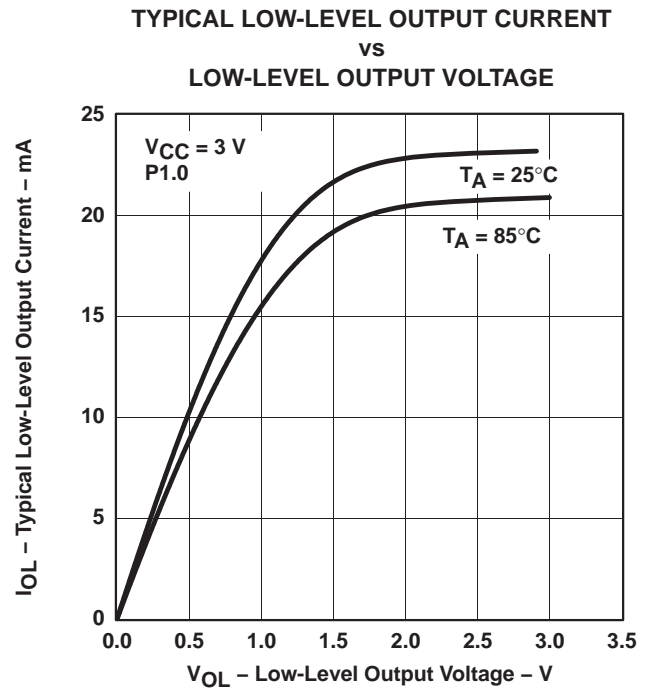


Figure 3

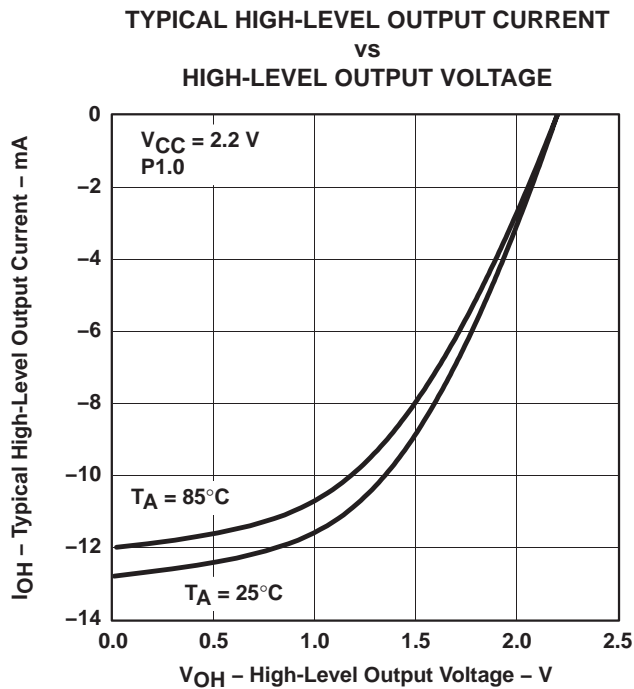


Figure 4

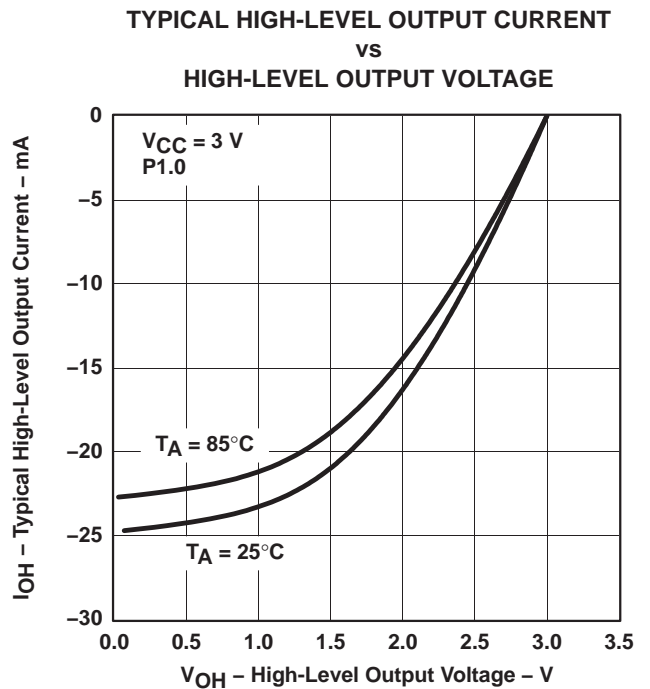


Figure 5

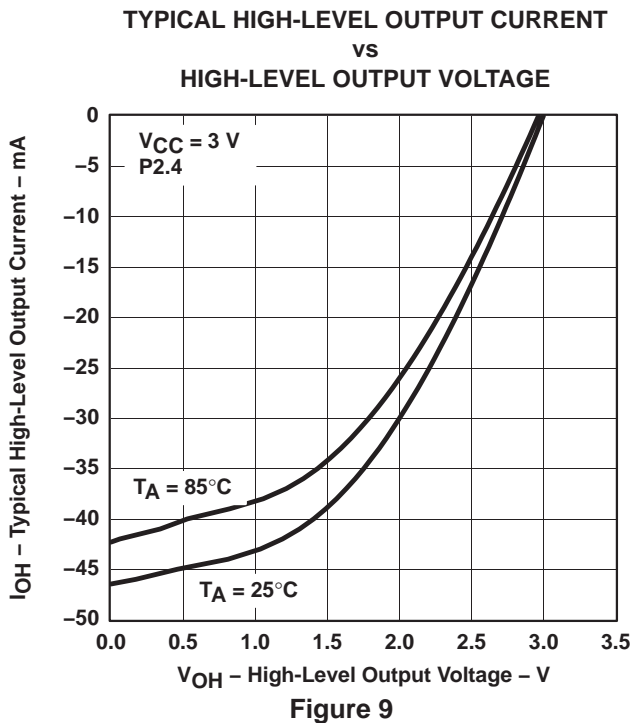
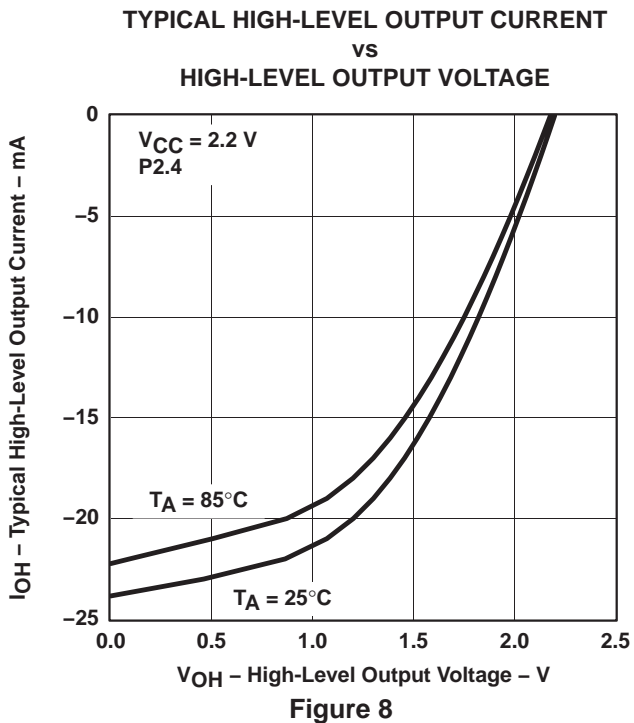
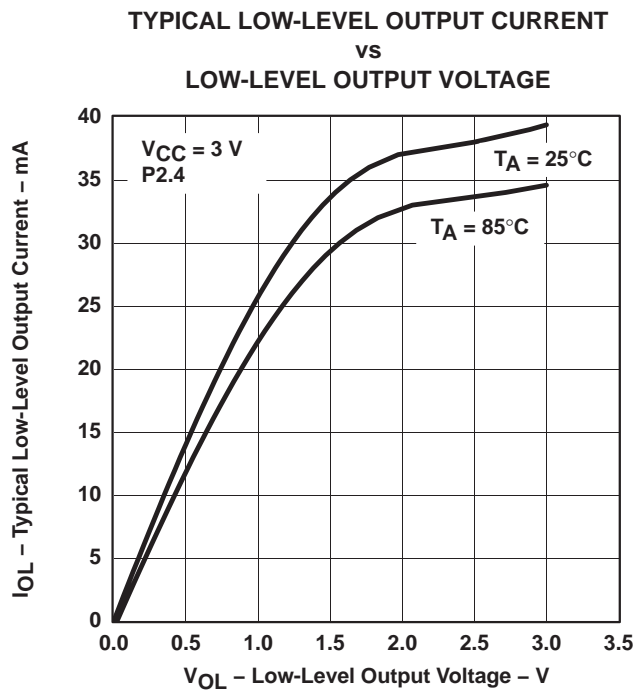
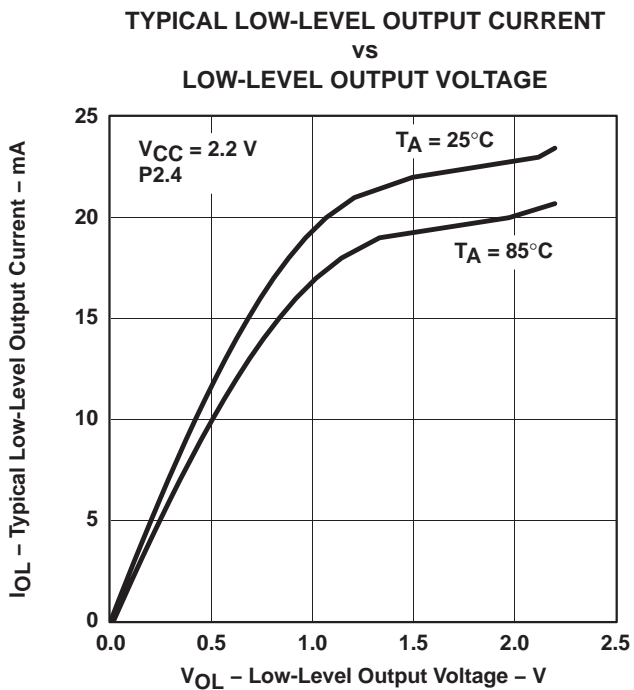
NOTE A: One output loaded at a time

MSP430x41x MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

MSP430x415, MSP430x417 outputs – Ports P1, P2, P3, P4, P5, and P6 (see Note)



NOTE B: One output loaded at a time



electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

wake-up LPM3

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---------------------------------|-----------------|-----------------------------|-----|-----|-----|------|
| t _{d(LPM3)} Delay time | f = 1 MHz | V _{CC} = 2.2 V/3 V | | | 6 | μs |
| | f = 2 MHz | | | | 6 | |
| | f = 3 MHz | | | | 6 | |

RAM (see Note 1)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|-------------------------|-----|-----|-----|------|
| V _{RAMh} | CPU halted (see Note 1) | 1.6 | | | V |

NOTE 1: This parameter defines the minimum supply voltage when the data in the program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

LCD

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT | | |
|---------------------------------------|----------------------|---|--|-----|-----------------------|------|-------------------------|--|
| V ₍₃₃₎ | Analog voltage | Voltage at P5.7/R33 | 2.5 | | V _{CC} + 0.2 | V | | |
| V ₍₂₃₎ | | Voltage at P5.6/R23 | | | | | V _{CC} = 3 V | (V ₍₃₃₎ - V ₍₀₃₎) × 2/3 + V ₍₀₃₎ |
| V ₍₁₃₎ | | Voltage at P5.5/R13 | | | | | | (V ₍₃₃₎ - V ₍₀₃₎) × 1/3 + V ₍₀₃₎ |
| V ₍₃₃₎ - V ₍₀₃₎ | | Voltage at R33/R03 | | | | | 2.5 | V _{CC} + 0.2 |
| I _(R03) | Input leakage | R03 = V _{SS} | No load at all segment and common lines, V _{CC} = 3 V | | ±20 | nA | | |
| I _(R13) | | P5.5/R13 = V _{CC} /3 | | | | | ±20 | |
| I _(R23) | | P5.6/R23 = 2 × V _{CC} /3 | | | | | ±20 | |
| V _(Sxx0) | Segment line voltage | I _(Sxx) = -3 μA, V _{CC} = 3 V | | | | V | | |
| V _(Sxx1) | | | | | | | V ₍₀₃₎ | V ₍₀₃₎ - 0.1 |
| V _(Sxx2) | | | | | | | V ₍₁₃₎ | V ₍₁₃₎ - 0.1 |
| V _(Sxx3) | | | | | | | V ₍₂₃₎ | V ₍₂₃₎ - 0.1 |
| | | | | | | | V ₍₃₃₎ + 0.1 | |

MSP430x41x MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Comparator_A (see Note 1)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|-----------------------|--|-------------------------------|------|----------------------|------|----|
| I(CC) | CAON = 1, CARSEL = 0, CAREF = 0 | V _{CC} = 2.2 V | 25 | 40 | μA | |
| | | V _{CC} = 3 V | 45 | 60 | | |
| I(Refladder/RefDiode) | CAON = 1, CARSEL = 0, CAREF = 1/2/3, No load at P1.6/CA0 and P1.7/CA1 | V _{CC} = 2.2 V | 30 | 50 | μA | |
| | | V _{CC} = 3 V | 45 | 71 | | |
| V(Ref025) | $\frac{\text{Voltage @ } 0.25 V_{CC} \text{ node}}{V_{CC}}$ PCA0 = 1, CARSEL = 1, CAREF = 1, No load at P1.6/CA0 and P1.7/CA1 | V _{CC} = 2.2 V / 3 V | 0.23 | 0.24 | 0.25 | |
| V(Ref050) | $\frac{\text{Voltage @ } 0.5 V_{CC} \text{ node}}{V_{CC}}$ PCA0 = 1, CARSEL = 1, CAREF = 2, No load at P1.6/CA0 and P1.7/CA1 | V _{CC} = 2.2V / 3 V | 0.47 | 0.48 | 0.50 | |
| V(RefVT) | (see Figure 10 and Figure 11) PCA0 = 1, CARSEL = 1, CAREF = 3, No load at P1.6/CA0 and P1.7/CA1; T _A = 85°C | V _{CC} = 2.2 V | 390 | 480 | 540 | mV |
| | | V _{CC} = 3.0 V | 400 | 490 | 550 | |
| V(IC) | Common-mode input voltage range CAON = 1 | V _{CC} = 2.2V/3 V | 0 | V _{CC} -1.0 | V | |
| V(offset) | Offset voltage See Note 2 | V _{CC} = 2.2 V/3 V | -30 | 30 | mV | |
| Vhys | Input hysteresis CAON = 1 | V _{CC} = 2.2 V / 3 V | 0 | 0.7 | 1.4 | mV |
| t(response LH) | T _A = 25°C, Overdrive 10 mV, without filter: CAF = 0 | V _{CC} = 2.2 V | 160 | 210 | 300 | ns |
| | | V _{CC} = 3 V | 80 | 150 | 240 | |
| | T _A = 25°C Overdrive 10 mV, with filter: CAF = 1 | V _{CC} = 2.2 V | 1.4 | 1.9 | 3.4 | μs |
| | | V _{CC} = 3 V | 0.9 | 1.5 | 2.6 | |
| t(response HL) | T _A = 25°C Overdrive 10 mV, without filter: CAF = 0 | V _{CC} = 2.2 V | 130 | 210 | 300 | ns |
| | | V _{CC} = 3 V | 80 | 150 | 240 | |
| | T _A = 25°C, Overdrive 10 mV, with filter: CAF = 1 | V _{CC} = 2.2 V | 1.4 | 1.9 | 3.4 | μs |
| | | V _{CC} = 3.0 V | 0.9 | 1.5 | 2.6 | |

- NOTES: 1. The leakage current for the Comparator_A terminals is identical to I_{kg}(P_{x,x}) specification.
 2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.



electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

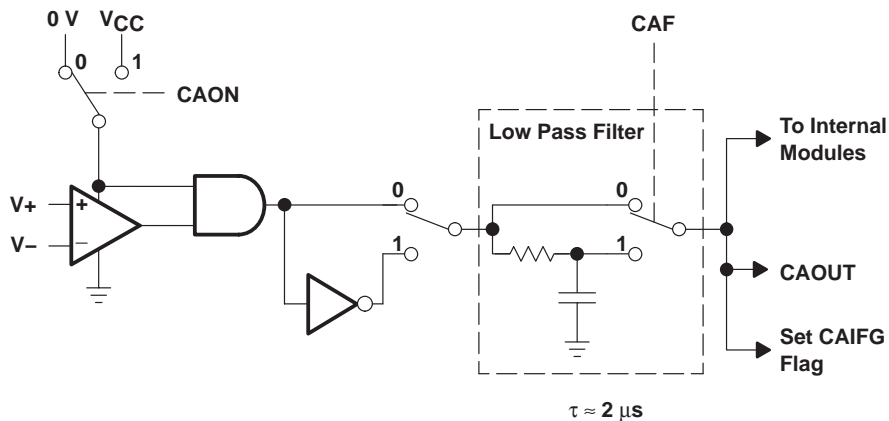
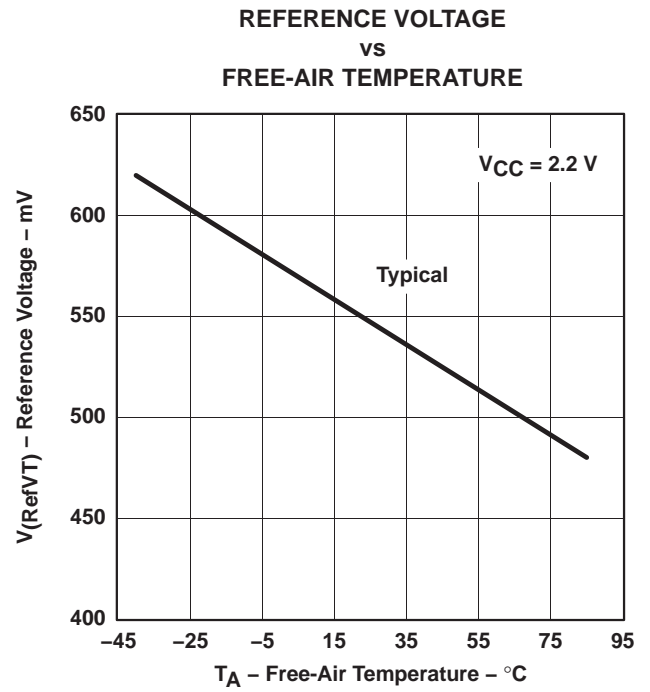
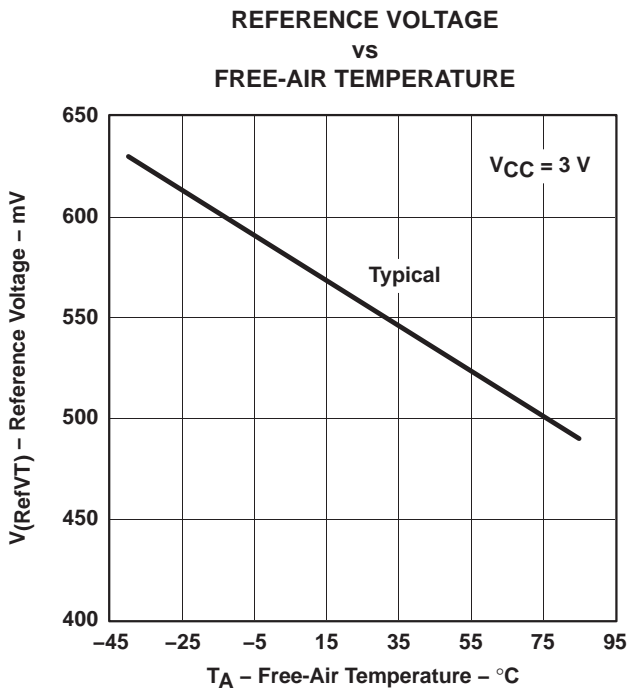
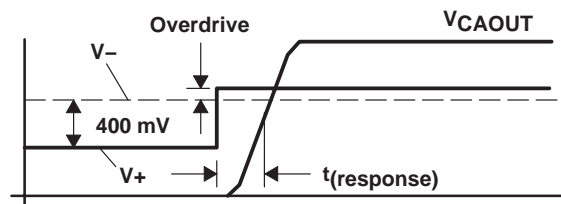


Figure 12. Block Diagram of Comparator_A Module



MSP430x41x MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

POR brownout, reset (see Notes 1 and 2)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|--|-----|-------------------------------|------|---------------|
| $t_d(\text{BOR})$ | | | | 2000 | μs |
| $V_{\text{CC}}(\text{start})$ | $dV_{\text{CC}}/dt \leq 3 \text{ V/s}$ (see Figure 14) | | $0.7 \times V(\text{B_IT-})$ | | V |
| $V(\text{B_IT-})$ | $dV_{\text{CC}}/dt \leq 3 \text{ V/s}$ (see Figure 14, Figure 15, Figure 16) | | | 1.71 | V |
| $V_{\text{hys}}(\text{B_IT-})$ | $dV_{\text{CC}}/dt \leq 3 \text{ V/s}$ (see Figure 14) | 70 | 130 | 180 | mV |
| $t(\text{reset})$ | Pulse length needed at $\overline{\text{RST/NMI}}$ pin to accepted reset internally, $V_{\text{CC}} = 2.2 \text{ V}/3 \text{ V}$ | 2 | | | μs |

- NOTES: 1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V(\text{B_IT-}) + V_{\text{hys}}(\text{B_IT-})$ is $\leq 1.8 \text{ V}$.
2. During power up, the CPU begins code execution following a period of $t_d(\text{BOR})$ after $V_{\text{CC}} = V(\text{B_IT-}) + V_{\text{hys}}(\text{B_IT-})$. The default FLL+ settings must not be changed until $V_{\text{CC}} \geq V_{\text{CC}}(\text{min})$. See the *MSP430x4xx Family User's Guide* (SLAU056) for more information on the brownout/SVS circuit.

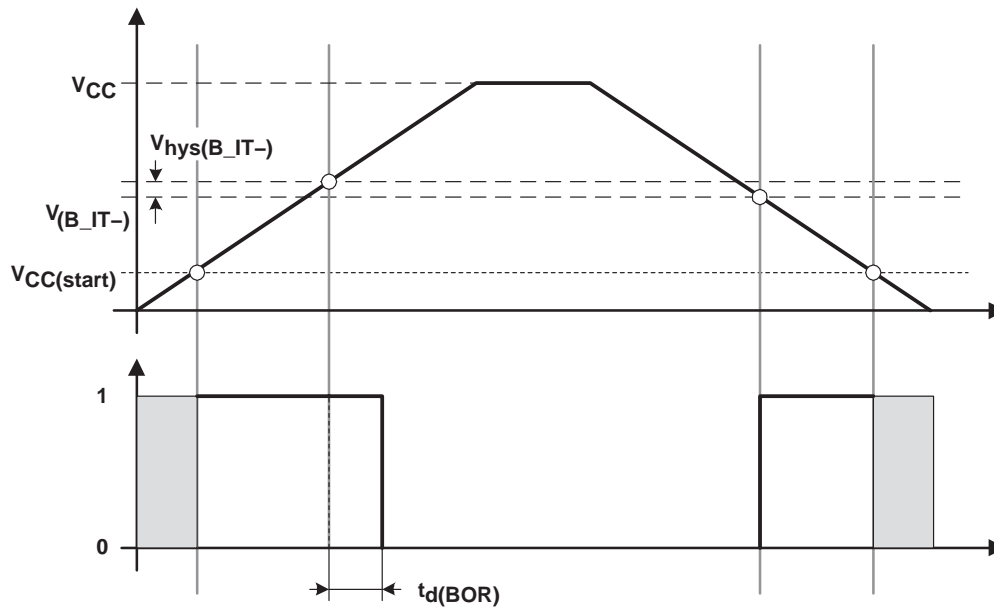


Figure 14. POR/Brownout Reset (BOR) vs Supply Voltage

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

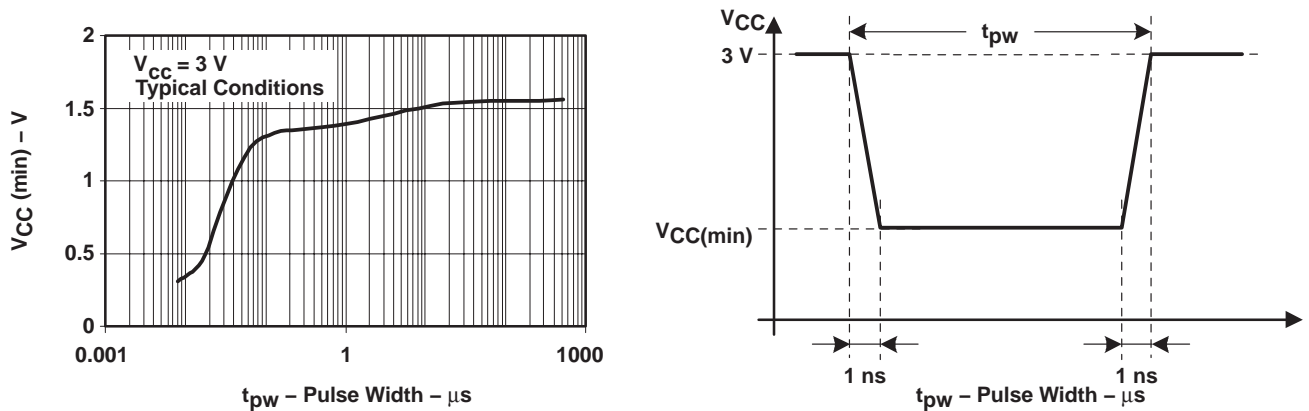


Figure 15. $V_{CC(min)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

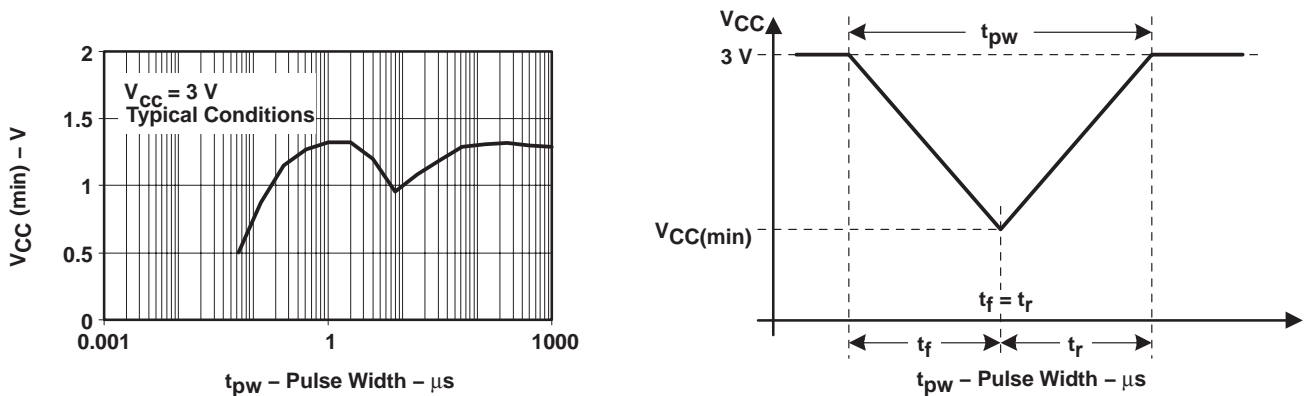


Figure 16. $V_{CC(min)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

SVS (supply voltage supervisor/monitor, see Notes 1 and 2) MSP430x412, MSP430x413 only

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|--|-----|------|------|---------|
| $t_d(SVSR)$ | $dV_{CC}/dt > 30V/ms$ (see Note 2) | 5 | | 150 | μs |
| | $dV_{CC}/dt \leq 30V/ms$ (see Note 2) | | | 2000 | μs |
| $t_d(SV_{Son})$ | SV _{Son} , switch from 0 to 1, $V_{CC} = 3V$ (see Note 2) | 20 | | 150 | μs |
| $V(SV_{Sstart})$ | $dV_{CC}/dt \leq 3V/s$ (see Figure 17) | | 1.55 | 1.7 | V |
| $V(SV_{S_IT-})$ | $dV_{CC}/dt \leq 3V/s$ (see Figure 17) | 1.8 | 1.95 | 2.2 | V |
| $V_{hys}(SV_{S_IT-})$ | $dV_{CC}/dt \leq 3V/s$ (see Figure 17) | 70 | 100 | 155 | mV |
| $I_{CC}(SVS)$ (see Note 1) | $VLD \neq 0$ (VLD bits are in SVSCTL register), $V_{CC} = 2.2V/3V$ | | 10 | 15 | μA |

- NOTES: 1. The current consumption of the SVS module is not included in the I_{CC} current consumption data.
2. The SVS is not active at power up.

MSP430x41x MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

SVS (supply voltage supervisor/monitor, see Notes 1 and 2) MSP430x415, MSP430x417 only

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT | |
|---------------------------------------|--|---------------|-----------------------------------|------------------|-----------------------------------|----|
| t _d (SVSR) | dV _{CC} /dt > 30 V/ms (see Figure 17) | 5 | | 150 | μs | |
| | dV _{CC} /dt ≤ 30 V/ms | | | 2000 | μs | |
| t _d (SVSon) | SVSon, switch from VLD=0 to VLD ≠ 0, V _{CC} = 3 V | 20 | | 150 | μs | |
| t _{settle} | VLD ≠ 0 [†] | | | 12 | μs | |
| V _(SVSstart) | VLD ≠ 0, V _{CC} /dt ≤ 3 V/s (see Figure 17) | | 1.55 | 1.7 | V | |
| V _{hys} (SVS_IT-) | V _{CC} /dt ≤ 3 V/s (see Figure 17) | VLD = 1 | 70 | 120 | 155 | mV |
| | | VLD = 2 .. 14 | V _(SVS_IT-) x 0.004 | | V _(SVS_IT-) x 0.008 | |
| | V _{CC} /dt ≤ 3 V/s (see Figure 17), external voltage applied on SVSIN | VLD = 15 | 4.4 | | 10.4 | mV |
| V _(SVS_IT-) | V _{CC} /dt ≤ 3 V/s (see Figure 17) | VLD = 1 | 1.8 | 1.9 | 2.05 | V |
| | | VLD = 2 | 1.94 | 2.1 | 2.25 | |
| | | VLD = 3 | 2.05 | 2.2 | 2.37 | |
| | | VLD = 4 | 2.14 | 2.3 | 2.48 | |
| | | VLD = 5 | 2.24 | 2.4 | 2.6 | |
| | | VLD = 6 | 2.33 | 2.5 | 2.71 | |
| | | VLD = 7 | 2.46 | 2.65 | 2.86 | |
| | | VLD = 8 | 2.58 | 2.8 | 3 | |
| | | VLD = 9 | 2.69 | 2.9 | 3.13 | |
| | | VLD = 10 | 2.83 | 3.05 | 3.29 | |
| | | VLD = 11 | 2.94 | 3.2 | 3.42 | |
| | | VLD = 12 | 3.11 | 3.35 | 3.61 [‡] | |
| | | VLD = 13 | 3.24 | 3.5 | 3.76 [‡] | |
| | | VLD = 14 | 3.43 | 3.7 [‡] | 3.99 [‡] | |
| | V _{CC} /dt ≤ 3 V/s (see Figure 17), external voltage applied on SVSIN | VLD = 15 | 1.1 | 1.2 | 1.3 | |
| I _{CC} (SVS) (see Note 1) | VLD ≠ 0, V _{CC} = 2.2 V/3 V | | 10 | 15 | μA | |

[†] The recommended operating voltage range is limited to 3.6 V.

[‡] t_{settle} is the settling time that the comparator o/p needs to have a stable level after VLD is switched VLD ≠ 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be > 50 mV.

NOTES: 1. The current consumption of the SVS module is not included in the I_{CC} current consumption data.
2. The SVS is not active at power up.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

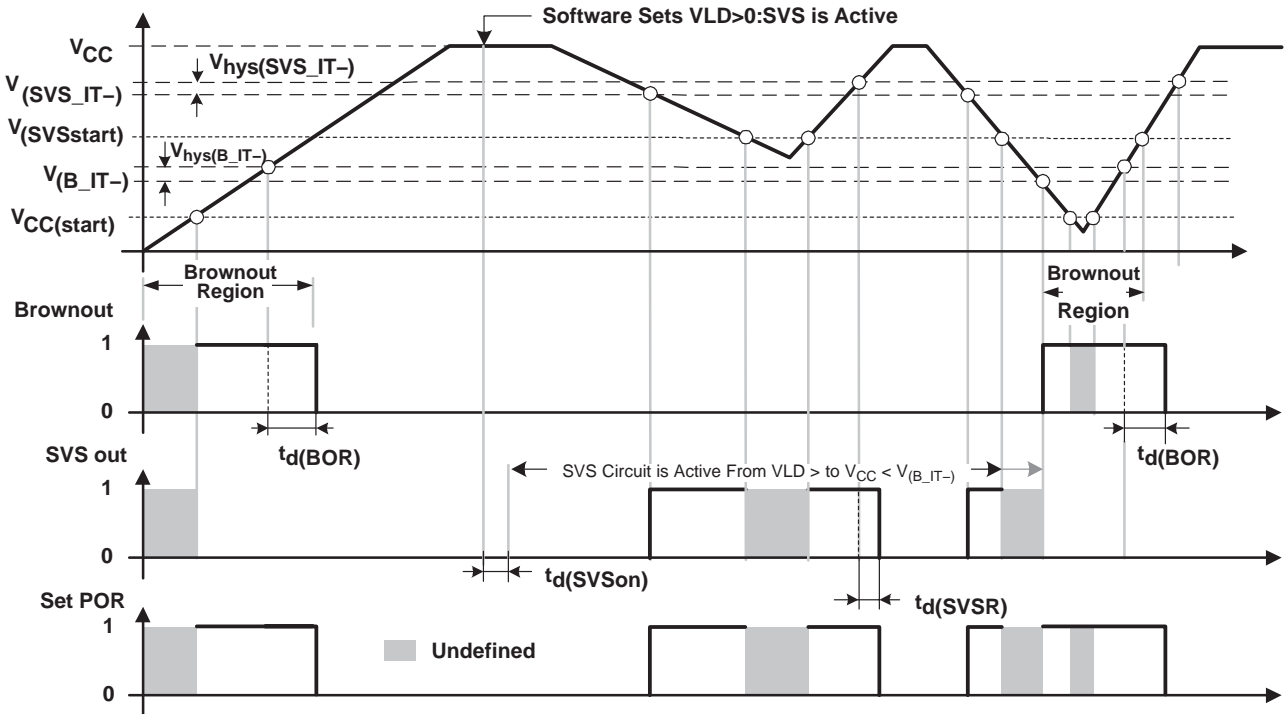


Figure 17. SVS Reset (SVSR) vs Supply Voltage

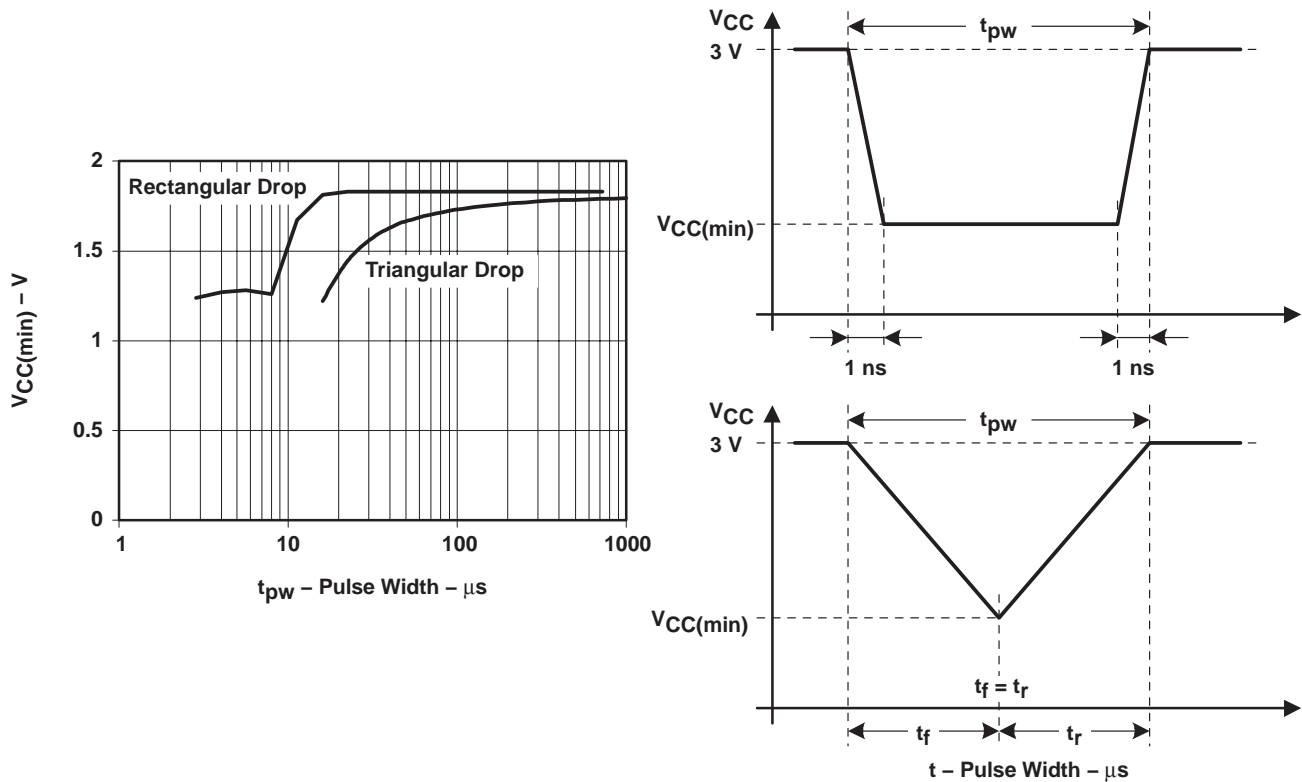


Figure 18. $V_{CC(min)}$ With a Square Voltage Drop and a Triangle Voltage Drop to Generate an SVS Signal

MSP430x41x MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

DCO

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------|---|-----------------|------|------|------|-------------------|
| f(DCOCLK) | N(DCO)=01E0h, FN_8=FN_4=FN_3=FN_2=0, D = 2; DCOPLUS= 0 | 2.2 V/3 V | | 1 | | MHz |
| f(DCO2) | FN_8=FN_4=FN_3=FN_2=0 ; DCOPLUS = 1 | 2.2 V | 0.3 | 0.65 | 1.25 | MHz |
| | | 3 V | 0.3 | 0.7 | 1.3 | |
| f(DCO27) | FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1, (see Note 1) | 2.2 V | 2.5 | 5.6 | 10.5 | MHz |
| | | 3 V | 2.7 | 6.1 | 11.3 | |
| f(DCO2) | FN_8=FN_4=FN_3=0, FN_2=1; DCOPLUS = 1 | 2.2 V | 0.7 | 1.3 | 2.3 | MHz |
| | | 3 V | 0.8 | 1.5 | 2.5 | |
| f(DCO27) | FN_8=FN_4=FN_3=0, FN_2=1; DCOPLUS = 1, (see Note 1) | 2.2 V | 5.7 | 10.8 | 18 | MHz |
| | | 3 V | 6.5 | 12.1 | 20 | |
| f(DCO2) | FN_8=FN_4=0, FN_3= 1, FN_2=x; DCOPLUS = 1 | 2.2 V | 1.2 | 2 | 3 | MHz |
| | | 3 V | 1.3 | 2.2 | 3.5 | |
| f(DCO27) | FN_8=FN_4=0, FN_3= 1, FN_2=x; DCOPLUS = 1, (see Note 1) | 2.2 V | 9 | 15.5 | 25 | MHz |
| | | 3 V | 10.3 | 17.9 | 28.5 | |
| f(DCO2) | FN_8=0, FN_4= 1, FN_3= FN_2=x; DCOPLUS = 1 | 2.2 V | 1.8 | 2.8 | 4.2 | MHz |
| | | 3 V | 2.1 | 3.4 | 5.2 | |
| f(DCO27) | FN_8=0, FN_4=1, FN_3= FN_2=x; DCOPLUS = 1, (see Note 1) | 2.2 V | 13.5 | 21.5 | 33 | MHz |
| | | 3 V | 16 | 26.6 | 41 | |
| f(DCO2) | FN_8=1, FN_4=FN_3=FN_2=x; DCOPLUS = 1 | 2.2 V | 2.8 | 4.2 | 6.2 | MHz |
| | | 3 V | 4.2 | 6.3 | 9.2 | |
| f(DCO27) | FN_8=1, FN_4=FN_3=FN_2=x; DCOPLUS = 1, (see Note 1) | 2.2 V | 21 | 32 | 46 | MHz |
| | | 3 V | 30 | 46 | 70 | |
| S _n | Step size between adjacent DCO taps: S _n = f(DCO(Tap n+1)) / f(DCO(Tap n)), (see Figure 20 for taps 21 to 27) | 1 < TAP ≤ 20 | 1.06 | | 1.11 | |
| | | TAP = 27 | 1.07 | | 1.17 | |
| D _t | Temperature drift, N(DCO) = 01E0h, FN_8=FN_4=FN_3=FN_2=0 D = 2; DCOPLUS = 0, (see Note 2) | 2.2 V | -0.2 | -0.3 | -0.4 | %/ ^o C |
| | | 3 V | -0.2 | -0.3 | -0.4 | |
| D _V | Drift with V _{CC} variation, N(DCO) = 01E0h, FN_8=FN_4=FN_3=FN_2=0 D = 2; DCOPLUS = 0 (see Note 2) | | 0 | 5 | 15 | %/V |

NOTES: 1. Do not exceed the maximum system frequency.
2. This parameter is not production tested.

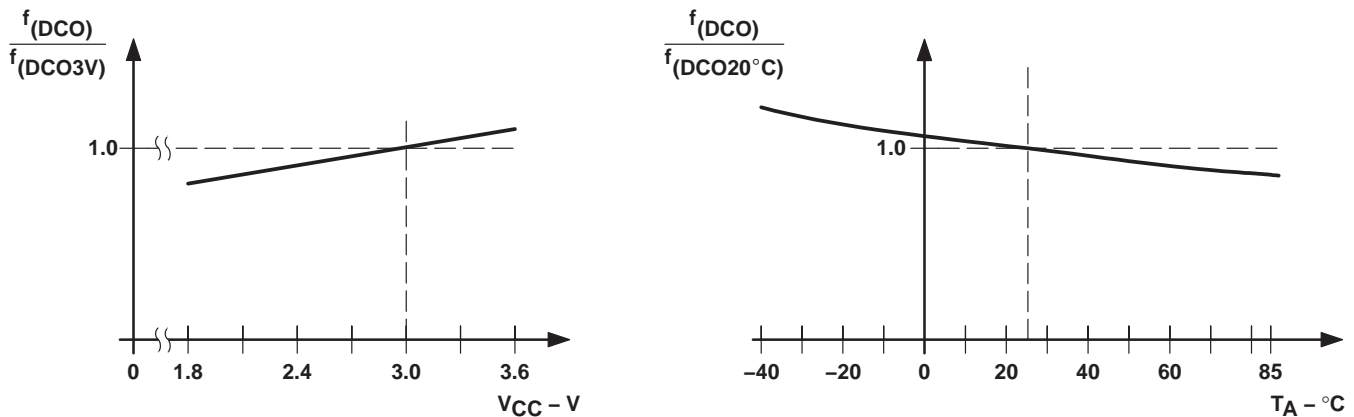


Figure 19. DCO Frequency vs Supply Voltage V_{CC} and vs Ambient Temperature



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

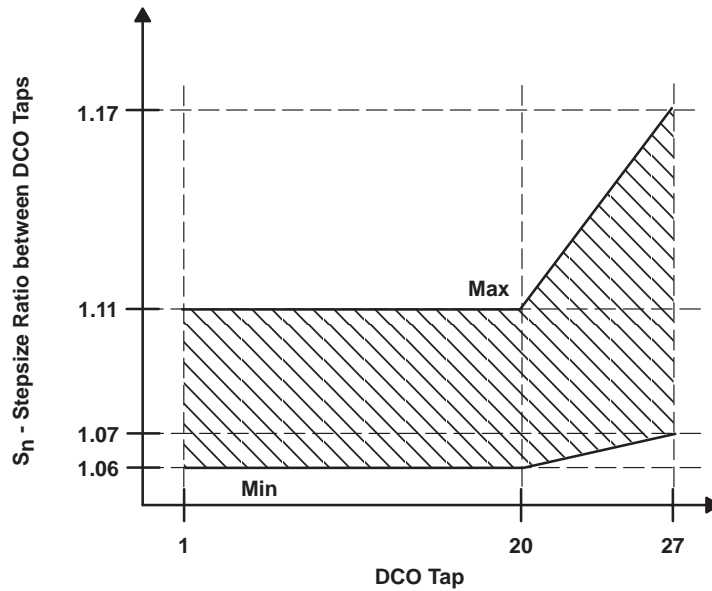


Figure 20. DCO Tap Step Size

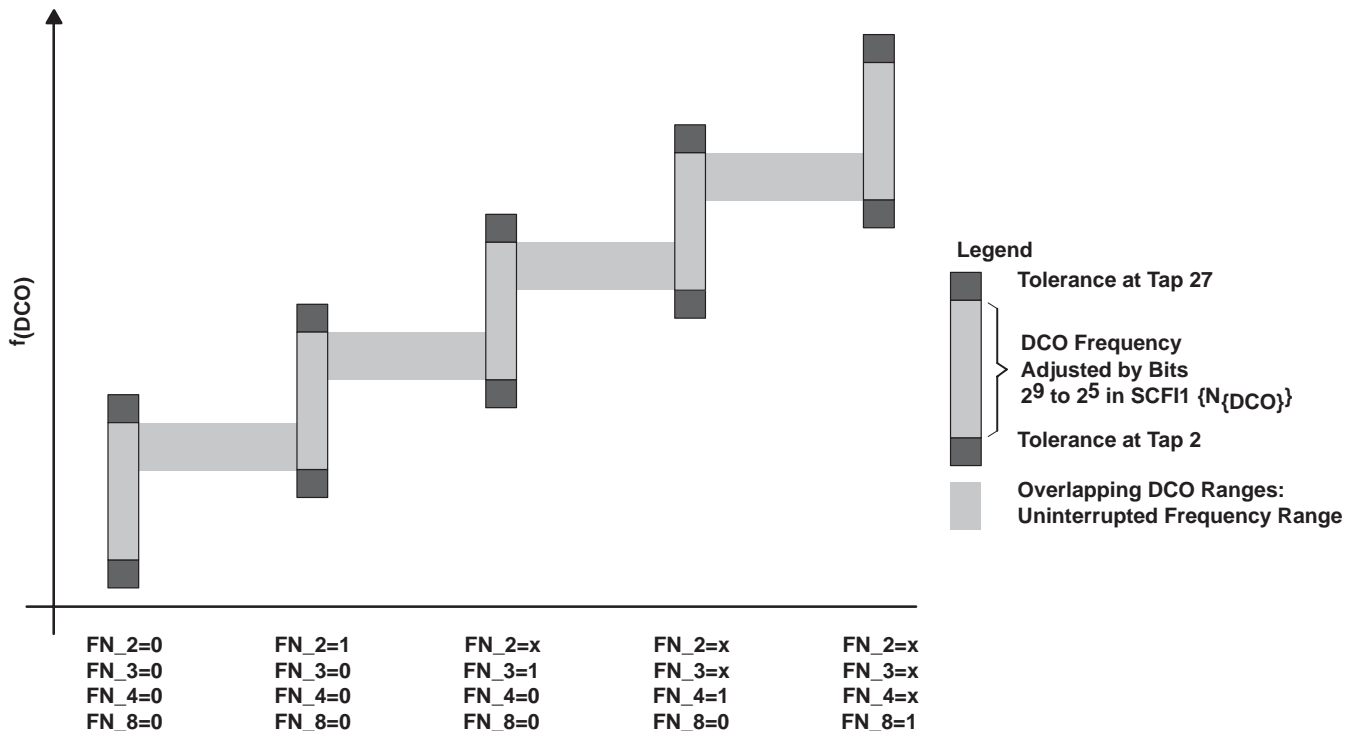


Figure 21. Five Overlapping DCO Ranges Controlled by FN_x Bits

MSP430x41x MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, LFXT1 oscillator (see Notes 1 and 2)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------|-----------------------------|-----------------|-----------------|---------------------|-----|---------------------|------|
| C _{XIN} | Integrated load capacitance | OSCCAPx = 0h | 2.2 V/3 V | | 0 | | pF |
| | | OSCCAPx = 1h | 2.2 V/3 V | | 10 | | |
| | | OSCCAPx = 2h | 2.2 V/3 V | | 14 | | |
| | | OSCCAPx = 3h | 2.2 V/3 V | | 18 | | |
| C _{XOUT} | Integrated load capacitance | OSCCAPx = 0h | 2.2 V/3 V | | 0 | | pF |
| | | OSCCAPx = 1h | 2.2 V/3 V | | 10 | | |
| | | OSCCAPx = 2h | 2.2 V/3 V | | 14 | | |
| | | OSCCAPx = 3h | 2.2 V/3 V | | 18 | | |
| V _{IL} | Input levels at XIN | see Note 3 | 2.2 V/3 V | V _{SS} | | 0.2×V _{CC} | V |
| V _{IH} | | | | 0.8×V _{CC} | | V _{CC} | |

- NOTES:
- The parasitic capacitance from the package and board may be estimated to be 2pF. The effective load capacitor for the crystal is $(C_{XIN} \times C_{XOUT}) / (C_{XIN} + C_{XOUT})$. It is independent of XTS_FLL.
 - To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines must be observed:
 - Keep as short a trace as possible between the 'x41x and the crystal.
 - Design a good ground plane around oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - Avoid running PCB traces underneath or adjacent to XIN and XOUT pins.
 - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
 - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
 - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
 - Applies only when using an external logic-level clock source. XTS_FLL must be set. Not applicable when using a crystal or resonator.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Flash Memory

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | NOM | MAX | UNIT |
|-----------------------------|---|-----------------------|-----------------|-----------------|-----------------|------|------------------|
| V _{CC} (PGM/ERASE) | Program and Erase supply voltage | | | 2.7 | | 3.6 | V |
| f _{FTG} | Flash Timing Generator frequency | | | 257 | | 476 | kHz |
| I _{PGM} | Supply current from DV _{CC} during program | | 2.7 V/ 3.6 V | | 3 | 5 | mA |
| I _{ERASE} | Supply current from DV _{CC} during erase | | 2.7 V/ 3.6 V | | 3 | 7 | mA |
| t _{CPT} | Cumulative program time | see Note 1 | 2.7 V/ 3.6 V | | | 4 | ms |
| t _{CMErase} | Cumulative mass erase time | see Note 2 | 2.7 V/ 3.6 V | 200 | | | ms |
| | Program/Erase endurance | | | 10 ⁴ | 10 ⁵ | | cycles |
| t _{Retention} | Data retention duration | T _J = 25°C | | 100 | | | years |
| t _{Word} | Word or byte program time | see Note 3 | | | | 35 | t _{FTG} |
| t _{Block, 0} | Block program time for 1 st byte or word | | | | | 30 | |
| t _{Block, 1-63} | Block program time for each additional byte or word | | | | | 21 | |
| t _{Block, End} | Block program end-sequence wait time | | | | | 6 | |
| t _{Mass Erase} | Mass erase time | | | | | 5297 | |
| t _{Seq Erase} | Segment erase time | | | | | 4819 | |

- NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
 2. The mass erase duration generated by the flash timing generator is at least 11.1ms (= 5297x1/f_{FTG,max} = 5297x1/476kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
 3. These values are hardwired into the Flash Controller's state machine (t_{FTG} = 1/f_{FTG}).

JTAG Interface

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | NOM | MAX | UNIT |
|-----------------------|---|-----------------|-----------------|-----|-----|-----|------|
| f _{TCK} | TCK input frequency | see Note 1 | 2.2 V | 0 | | 5 | MHz |
| | | | 3 V | 0 | | 10 | MHz |
| R _{Internal} | Internal pull-up resistance on TMS, TCK, TDI/TCLK | see Note 2 | 2.2 V/ 3 V | 25 | 60 | 90 | kΩ |

- NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.
 2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

JTAG Fuse (see Note 1)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | NOM | MAX | UNIT |
|----------------------|---|-----------------------|-----------------|-----|-----|-----|------|
| V _{CC} (FB) | Supply voltage during fuse-blow condition | T _A = 25°C | | 2.5 | | | V |
| V _{FB} | Voltage level on TDI/TCLK for fuse-blow - 'C41x | | | 3.5 | | 3.9 | V |
| | Voltage level on TDI/TCLK for fuse-blow - 'F41x | | | 6 | | 7 | V |
| I _{FB} | Supply current into TDI/TCLK during fuse blow | | | | | 100 | mA |
| t _{FB} | Time to blow fuse | | | | | 1 | ms |

- NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

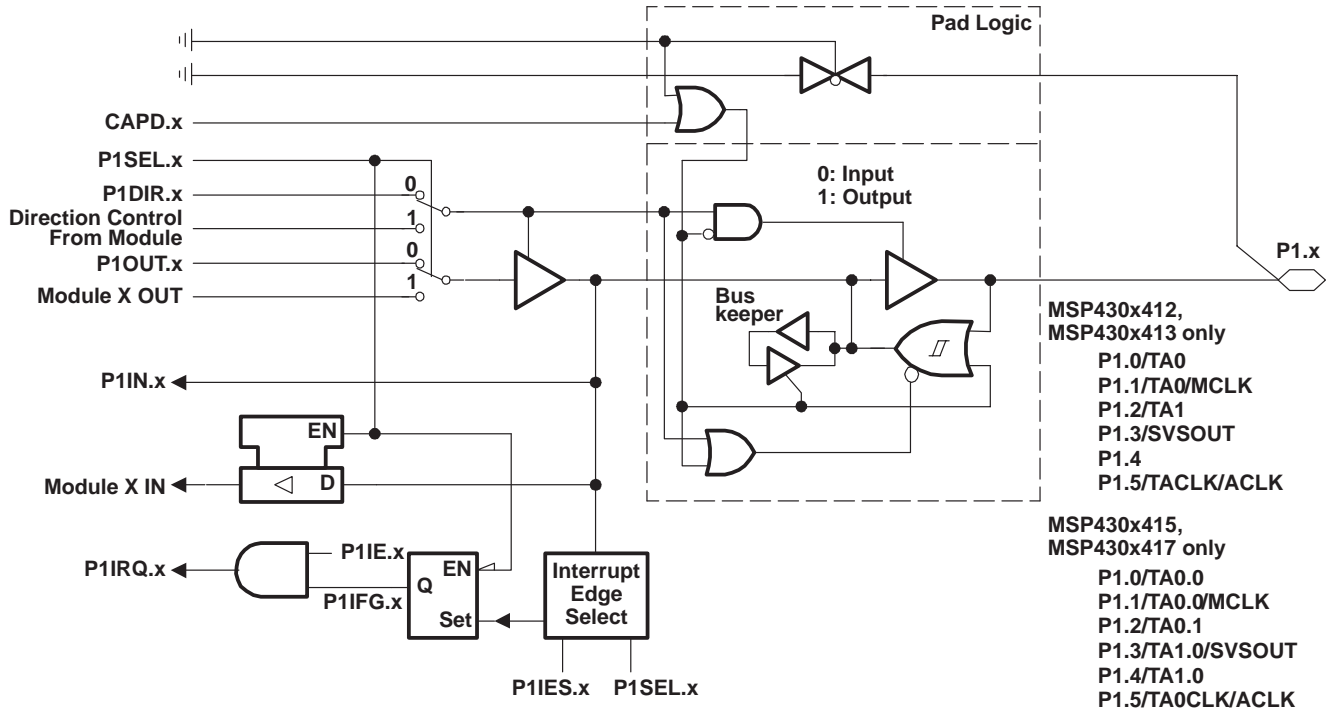
MSP430x41x MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

APPLICATION INFORMATION

input/output schematic

Port P1, P1.0 to P1.5, input/output with Schmitt-trigger



NOTE: $0 \leq x \leq 5$.
Port Function is Active if CAPD.x = 0

| PnSEL.x | PnDIR.x | Direction Control From Module | PnOUT.x | Module X OUT | PnIN.x | Module X IN | PnIE.x | PnIFG.x | PnIES.x |
|---------|---------|-------------------------------|---------|---|--------|---|--------|---------|---------|
| P1SEL.0 | P1DIR.0 | P1DIR.0 | P1OUT.0 | Out0 Sig. [†] | P1IN.0 | CCI0A [†] | P1IE.0 | P1IFG.0 | P1IES.0 |
| P1SEL.1 | P1DIR.1 | P1DIR.1 | P1OUT.1 | MCLK | P1IN.1 | CCI0B [†] | P1IE.1 | P1IFG.1 | P1IES.1 |
| P1SEL.2 | P1DIR.2 | P1DIR.2 | P1OUT.2 | Out1 Sig. [†] | P1IN.2 | CCI1A [†] | P1IE.2 | P1IFG.2 | P1IES.2 |
| P1SEL.3 | P1DIR.3 | P1DIR.3 | P1OUT.3 | SVSOUT | P1IN.3 | Unused | P1IE.3 | P1IFG.3 | P1IES.3 |
| P1SEL.4 | P1DIR.4 | P1DIR.4 | P1OUT.4 | DVSS [§] Out0 Sig. [‡] | P1IN.4 | Unused [§] CCI0A [†] | P1IE.4 | P1IFG.4 | P1IES.4 |
| P1SEL.5 | P1DIR.5 | P1DIR.5 | P1OUT.5 | ACLK | P1IN.5 | TACLK [†] | P1IE.5 | P1IFG.5 | P1IES.5 |

[†] Timer_A3/Timer0_A3

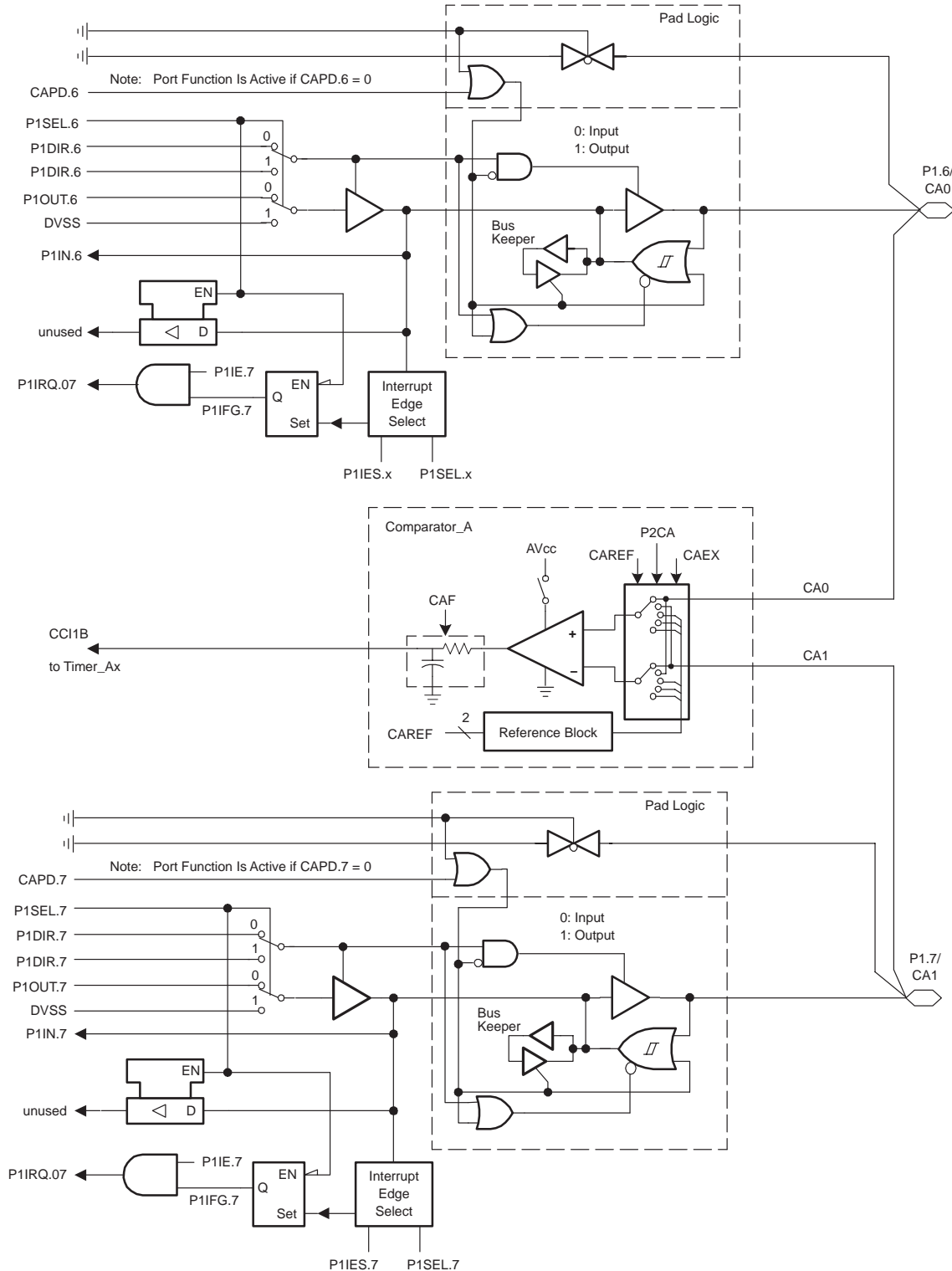
[‡] Timer1_A5 (MSP430x415, MSP430x417 only)

[§] MSP430x412, MSP430x413 only

APPLICATION INFORMATION

input/output schematic (continued)

Port P1, P1.6, P1.7 input/output with Schmitt-trigger

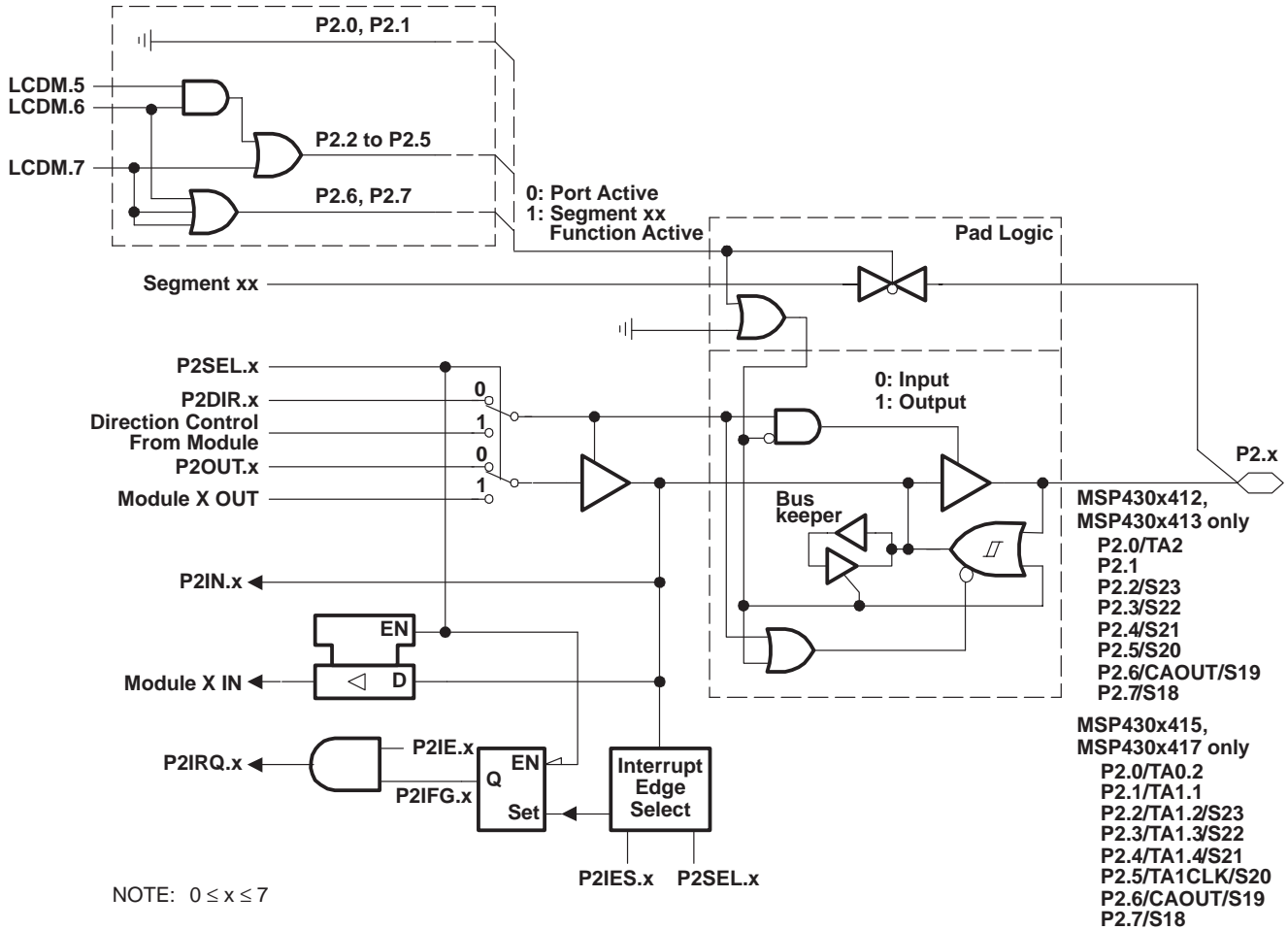


MSP430x41x MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

APPLICATION INFORMATION

input/output schematic (continued)
port P2, P2.0 to P2.7, input/output with Schmitt-trigger



| PnSEL.x | PnDIR.x | Direction Control From Module | PnOUT.x | Module X OUT | PnIN.x | Module X IN | PnIE.x | PnIFG.x | PnIES.x |
|---------|---------|-------------------------------|---------|---------------------|--------|--------------------|--------|---------|---------|
| P2SEL.0 | P2DIR.0 | P2DIR.0 | P2OUT.0 | Out2 Sig.† | P2IN.0 | CCI2A† | P2IE.0 | P2IFG.0 | P2IES.0 |
| P2SEL.1 | P2DIR.1 | P2DIR.1 | P2OUT.1 | DVSS§ Out1 Sig.‡ | P2IN.1 | Unused§ CCI1A† | P2IE.1 | P2IFG.1 | P2IES.1 |
| P2SEL.2 | P2DIR.2 | P2DIR.2 | P2OUT.2 | DVSS§ Out2 Sig.‡ | P2IN.2 | Unused§ CCI2A† | P2IE.2 | P2IFG.2 | P2IES.2 |
| P2SEL.3 | P2DIR.3 | P2DIR.3 | P2OUT.3 | DVSS§ Out3 Sig.‡ | P2IN.3 | Unused§ CCI3A† | P2IE.3 | P2IFG.3 | P2IES.3 |
| P2SEL.4 | P2DIR.4 | P2DIR.4 | P2OUT.4 | DVSS§ Out4 Sig.‡ | P2IN.4 | Unused§ CCI4A† | P2IE.4 | P2IFG.4 | P2IES.4 |
| P2SEL.5 | P2DIR.5 | P2DIR.5 | P2OUT.5 | DVSS | P2IN.5 | Unused§ TA1CLK† | P2IE.5 | P2IFG.5 | P2IES.5 |
| P2SEL.6 | P2DIR.6 | P2DIR.6 | P2OUT.6 | CAOUT | P2IN.6 | Unused | P2IE.6 | P2IFG.6 | P2IES.6 |
| P2SEL.7 | P2DIR.7 | P2DIR.7 | P2OUT.7 | DVSS | P2IN.7 | Unused | P2IE.7 | P2IFG.7 | P2IES.7 |

† Timer_A3/Timer0_A3

‡ Timer1_A5 (MSP430x415, MSP430x417 only)

§ MSP430x412, MSP430x413 only

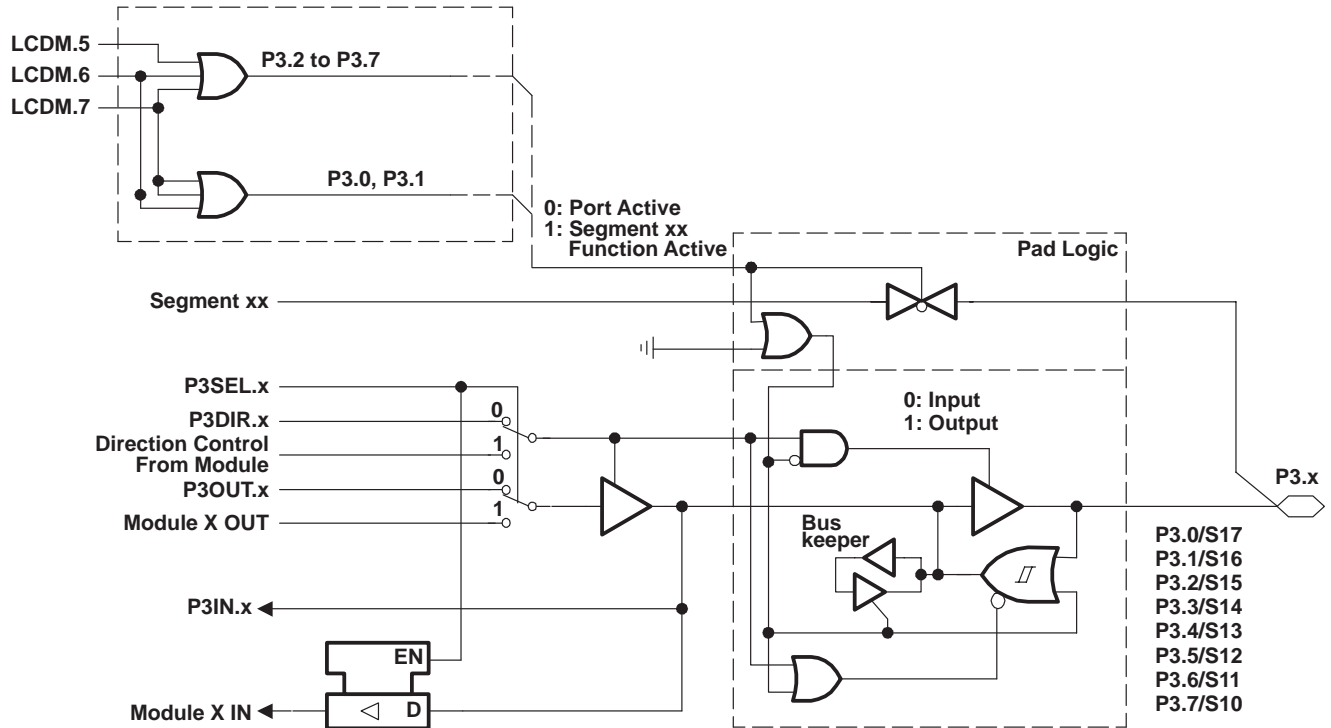


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

APPLICATION INFORMATION

input/output schematic (continued)

port P3, P3.0, P3.7, input/output with Schmitt-trigger



NOTE: $0 \leq x \leq 7$

| PnSEL.x | PnDIR.x | Direction Control From Module | PnOUT.x | Module X OUT | PnIN.x | Module X IN |
|---------|---------|-------------------------------|---------|--------------|--------|-------------|
| P3SEL.0 | P3DIR.0 | P3DIR.0 | P3OUT.0 | DVSS | P3IN.0 | Unused |
| P3SEL.1 | P3DIR.1 | P3DIR.1 | P3OUT.1 | DVSS | P3IN.1 | Unused |
| P3SEL.2 | P3DIR.2 | P3DIR.2 | P3OUT.2 | DVSS | P3IN.2 | Unused |
| P3SEL.3 | P3DIR.3 | P3DIR.3 | P3OUT.3 | DVSS | P3IN.3 | Unused |
| P3SEL.4 | P3DIR.4 | P3DIR.4 | P3OUT.4 | DVSS | P3IN.4 | Unused |
| P3SEL.5 | P3DIR.5 | P3DIR.5 | P3OUT.5 | DVSS | P3IN.5 | Unused |
| P3SEL.6 | P3DIR.6 | P3DIR.6 | P3OUT.6 | DVSS | P3IN.6 | Unused |
| P3SEL.7 | P3DIR.7 | P3DIR.7 | P3OUT.7 | DVSS | P3IN.7 | Unused |

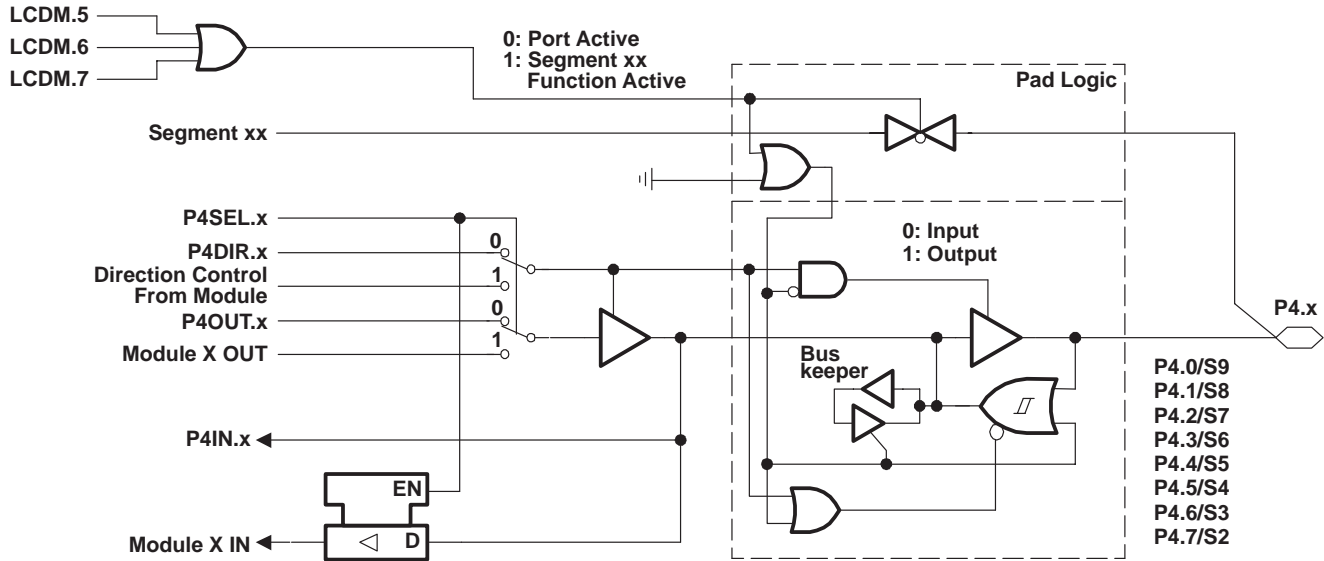
MSP430x41x MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

APPLICATION INFORMATION

input/output schematic (continued)

port P4, P4.0 to P4.7, input/output with Schmitt-trigger



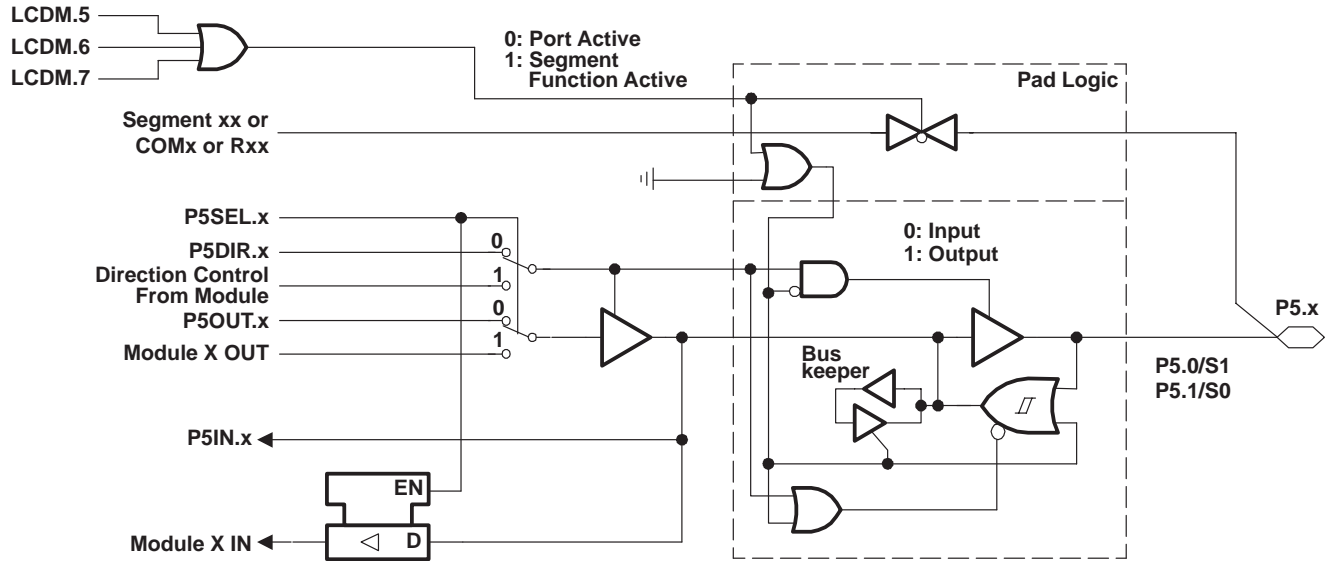
NOTE: $0 \leq x \leq 7$

| PnSEL.x | PnDIR.x | Direction Control From Module | PnOUT.x | Module X OUT | PnIN.x | Module X IN |
|---------|---------|-------------------------------|---------|--------------|--------|-------------|
| P4SEL.0 | P4DIR.0 | P4DIR.0 | P4OUT.0 | DVSS | P4IN.0 | Unused |
| P4SEL.1 | P4DIR.1 | P4DIR.1 | P4OUT.1 | DVSS | P4IN.1 | Unused |
| P4SEL.2 | P4DIR.2 | P4DIR.2 | P4OUT.2 | DVSS | P4IN.2 | Unused |
| P4SEL.3 | P4DIR.3 | P4DIR.3 | P4OUT.3 | DVSS | P4IN.3 | Unused |
| P4SEL.4 | P4DIR.4 | P4DIR.4 | P4OUT.4 | DVSS | P4IN.4 | Unused |
| P4SEL.5 | P4DIR.5 | P4DIR.5 | P4OUT.5 | DVSS | P4IN.5 | Unused |
| P4SEL.6 | P4DIR.6 | P4DIR.6 | P4OUT.6 | DVSS | P4IN.6 | Unused |
| P4SEL.7 | P4DIR.7 | P4DIR.7 | P4OUT.7 | DVSS | P4IN.7 | Unused |

APPLICATION INFORMATION

input/output schematic (continued)

port P5, P5.0, P5.1, input/output with Schmitt-trigger



NOTE: x = 0, 1

| PnSEL.x | PnDIR.x | Direction Control From Module | PnOUT.x | Module X OUT | PnIN.x | Module X IN | Segment |
|---------|---------|-------------------------------|---------|--------------|--------|-------------|---------|
| P5SEL.0 | P5DIR.0 | P5DIR.0 | P5OUT.0 | DVSS | P5IN.0 | Unused | S1 |
| P5SEL.1 | P5DIR.1 | P5DIR.1 | P5OUT.1 | DVSS | P5IN.1 | Unused | S0 |

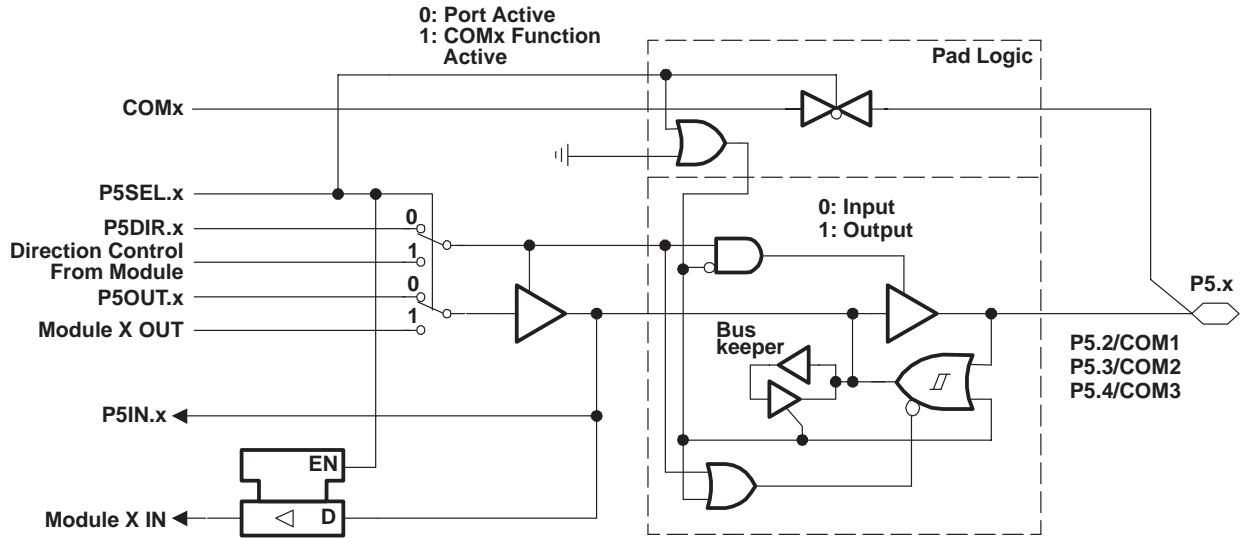
MSP430x41x MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

APPLICATION INFORMATION

input/output schematic (continued)

port P5, P5.2, P5.4, input/output with Schmitt-trigger



NOTE: $2 \leq x \leq 4$

| PnSEL.x | PnDIR.x | Direction Control From Module | PnOUT.x | Module X OUT | PnIN.x | Module X IN | COMx |
|---------|---------|-------------------------------|---------|--------------|--------|-------------|------|
| P5SEL.2 | P5DIR.2 | P5DIR.2 | P5OUT.2 | DVSS | P5IN.2 | Unused | COM1 |
| P5SEL.3 | P5DIR.3 | P5DIR.3 | P5OUT.3 | DVSS | P5IN.3 | Unused | COM2 |
| P5SEL.4 | P5DIR.4 | P5DIR.4 | P5OUT.4 | DVSS | P5IN.4 | Unused | COM3 |

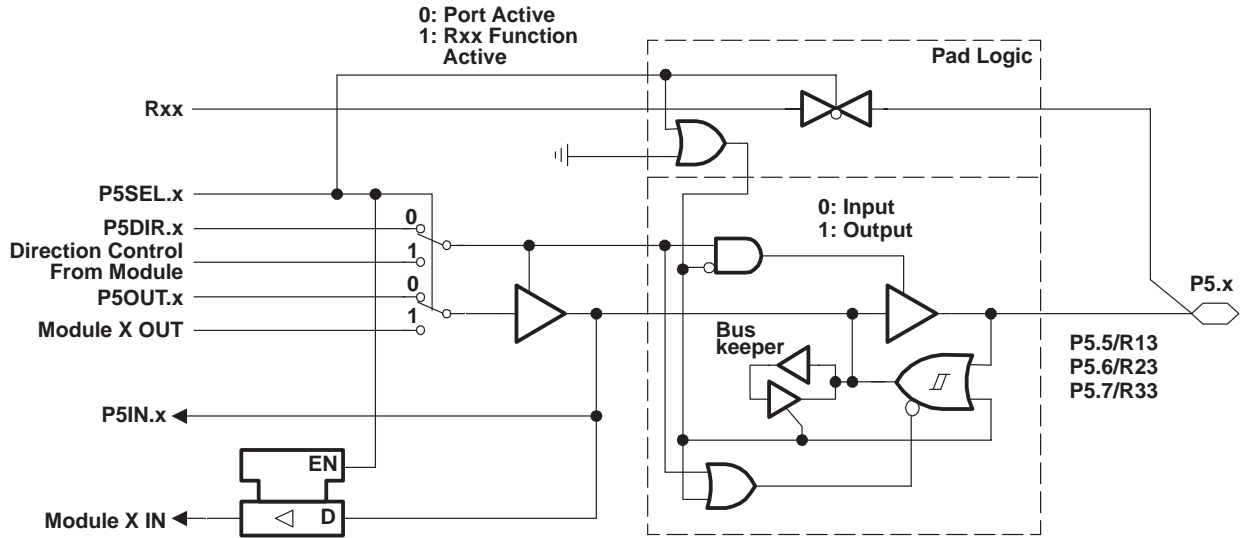
NOTE:

The direction control bits P5SEL.2, P5SEL.3, and P5SEL.4 are used to distinguish between port and common functions. Note that a 4MUX LCD requires all common signals COM3 to COM0, a 3MUX LCD requires COM2 to COM0, 2MUX LCD requires COM1 to COM0, and a static LCD requires only COM0.

APPLICATION INFORMATION

input/output schematic (continued)

port P5, P5.5 to P5.7, input/output with Schmitt-trigger



NOTE: $5 \leq x \leq 7$

| PnSEL.x | PnDIR.x | Direction Control From Module | PnOUT.x | Module X OUT | PnIN.x | Module X IN | Rxx |
|---------|---------|-------------------------------|---------|--------------|--------|-------------|-----|
| P5SEL.5 | P5DIR.5 | P5DIR.5 | P5OUT.5 | DVSS | P5IN.5 | Unused | R13 |
| P5SEL.6 | P5DIR.6 | P5DIR.6 | P5OUT.6 | DVSS | P5IN.6 | Unused | R23 |
| P5SEL.7 | P5DIR.7 | P5DIR.7 | P5OUT.7 | DVSS | P5IN.7 | Unused | R33 |

NOTE:

The direction control bits P5SEL.5, P5SEL.6, and P5SEL.7 are used to distinguish between port and LCD analog level functions. Note that 4MUX and 3MUX LCDs require all Rxx signals R33 to R03, a 2MUX LCD requires R33, R13, and R03, and a static LCD requires only R33 and R03.

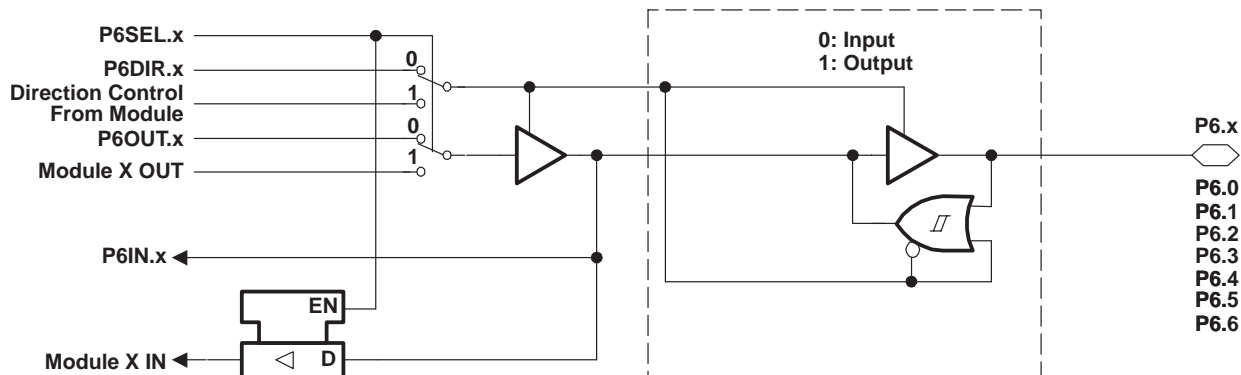
MSP430x41x MIXED SIGNAL MICROCONTROLLER

SLAS340G – MAY 2001 – REVISED JUNE 2004

APPLICATION INFORMATION

input/output schematic (continued)

port P6, P6.0 to P6.6, input/output with Schmitt-trigger

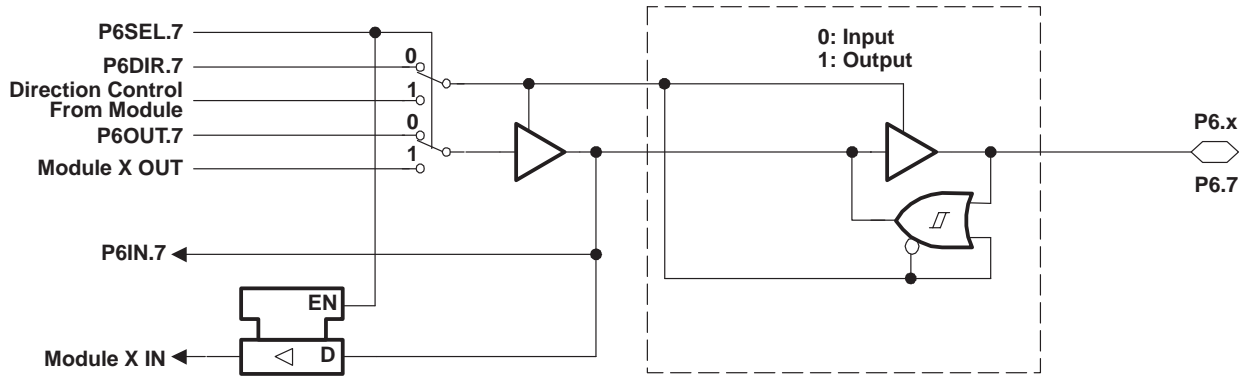


NOTE: $0 \leq x \leq 6$

| PnSEL.x | PnDIR.x | Direction Control From Module | PnOUT.x | Module X OUT | PnIN.x | Module X IN |
|---------|---------|-------------------------------|---------|--------------|--------|-------------|
| P6SEL.0 | P6DIR.0 | P6DIR.0 | P6OUT.0 | DVSS | P6IN.0 | Unused |
| P6SEL.1 | P6DIR.1 | P6DIR.1 | P6OUT.1 | DVSS | P6IN.1 | Unused |
| P6SEL.2 | P6DIR.2 | P6DIR.2 | P6OUT.2 | DVSS | P6IN.2 | Unused |
| P6SEL.3 | P6DIR.3 | P6DIR.3 | P6OUT.3 | DVSS | P6IN.3 | Unused |
| P6SEL.4 | P6DIR.4 | P6DIR.4 | P6OUT.4 | DVSS | P6IN.4 | Unused |
| P6SEL.5 | P6DIR.5 | P6DIR.5 | P6OUT.5 | DVSS | P6IN.5 | Unused |
| P6SEL.6 | P6DIR.6 | P6DIR.6 | P6OUT.6 | DVSS | P6IN.6 | Unused |

APPLICATION INFORMATION

input/output schematic (continued)
port P6, P6.7 input/output with Schmitt-trigger
MSP430x412/413 only



| PnSEL.x | PnDIR.x | Direction Control From Module | PnOUT.x | Module X OUT | PnIN.x | Module X IN |
|---------|---------|-------------------------------|---------|--------------|--------|-------------|
| P6SEL.7 | P6DIR.7 | P6DIR.7 | P6OUT.7 | DVSS | P6IN.7 | Unused |

MSP430x41x MIXED SIGNAL MICROCONTROLLER

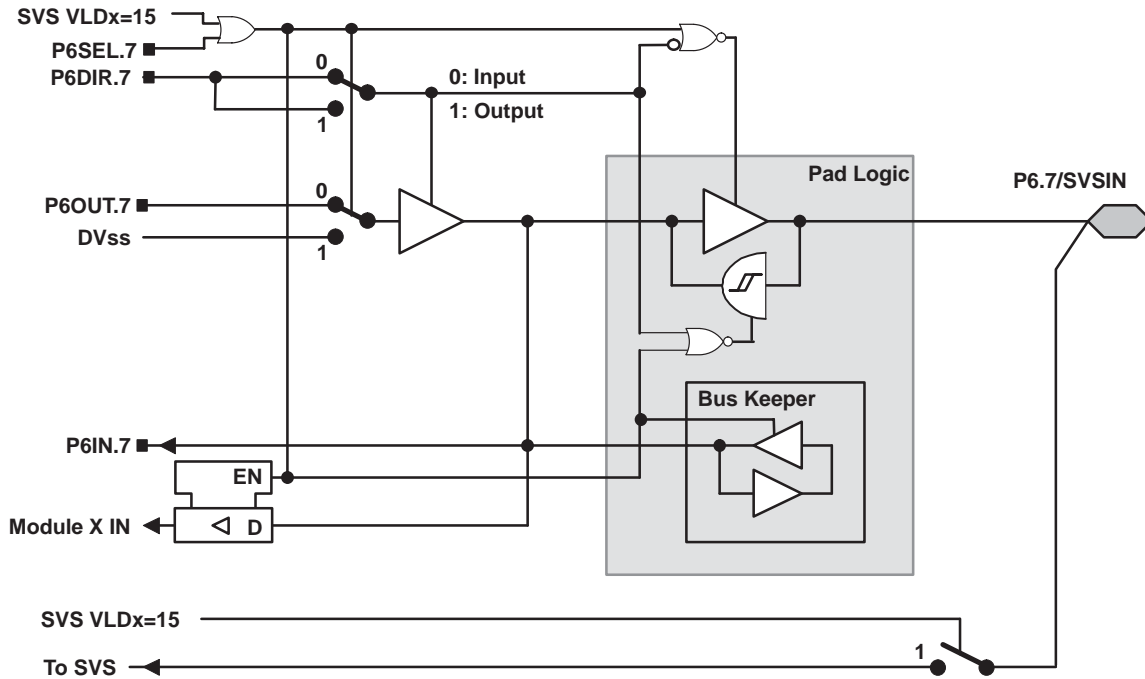
SLAS340G – MAY 2001 – REVISED JUNE 2004

APPLICATION INFORMATION

input/output schematic (continued)

port P6, P6.7 input/output with Schmitt-trigger

MSP430F415/417 only



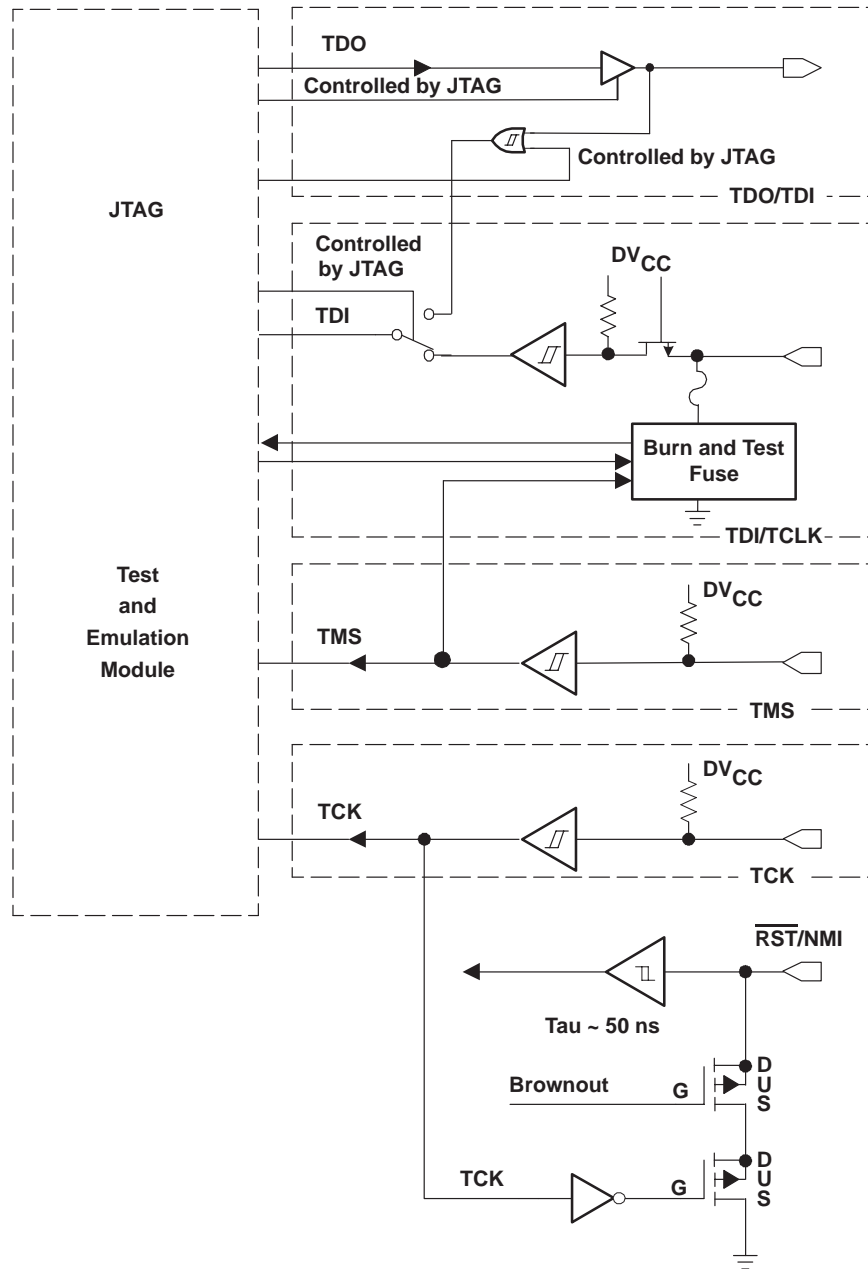
NOTE: Analog signals applied to digital gates can cause current flow from the positive to the negative terminal. The throughput current flows if the analog signal is in the range of transitions 0→1 or 1→0. The value of the throughput current depends on the driving capability of the gate. For MSP430, it is approximately 100 μ A.

Use P6SEL.x=1 to prevent throughput current. P6SEL.x should be set, if an analog signal is applied to the pin.

| SVS VLDx = 15 | P6SEL.7 | P6DIR.7 | Port Function |
|---------------|---------|---------|---------------|
| 0 | 0 | 0 | P6.7 Input |
| 0 | 0 | 1 | P6.7 Output |
| 0 | 1 | X | Undefined |
| 1 | X | X | SVSIN |

APPLICATION INFORMATION

JTAG pins TMS, TCK, TDI/TCLK, TDO/TDI, input/output with Schmitt-trigger or output



APPLICATION INFORMATION

JTAG fuse check mode

MSP430 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF} , of 1.8 mA at 3 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current only flows when the fuse check mode is active and the TMS pin is in a low state (see Figure 22). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

The JTAG pins are terminated internally, and therefore do not require external termination.

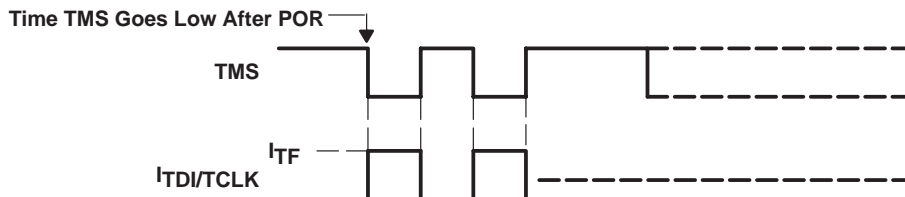
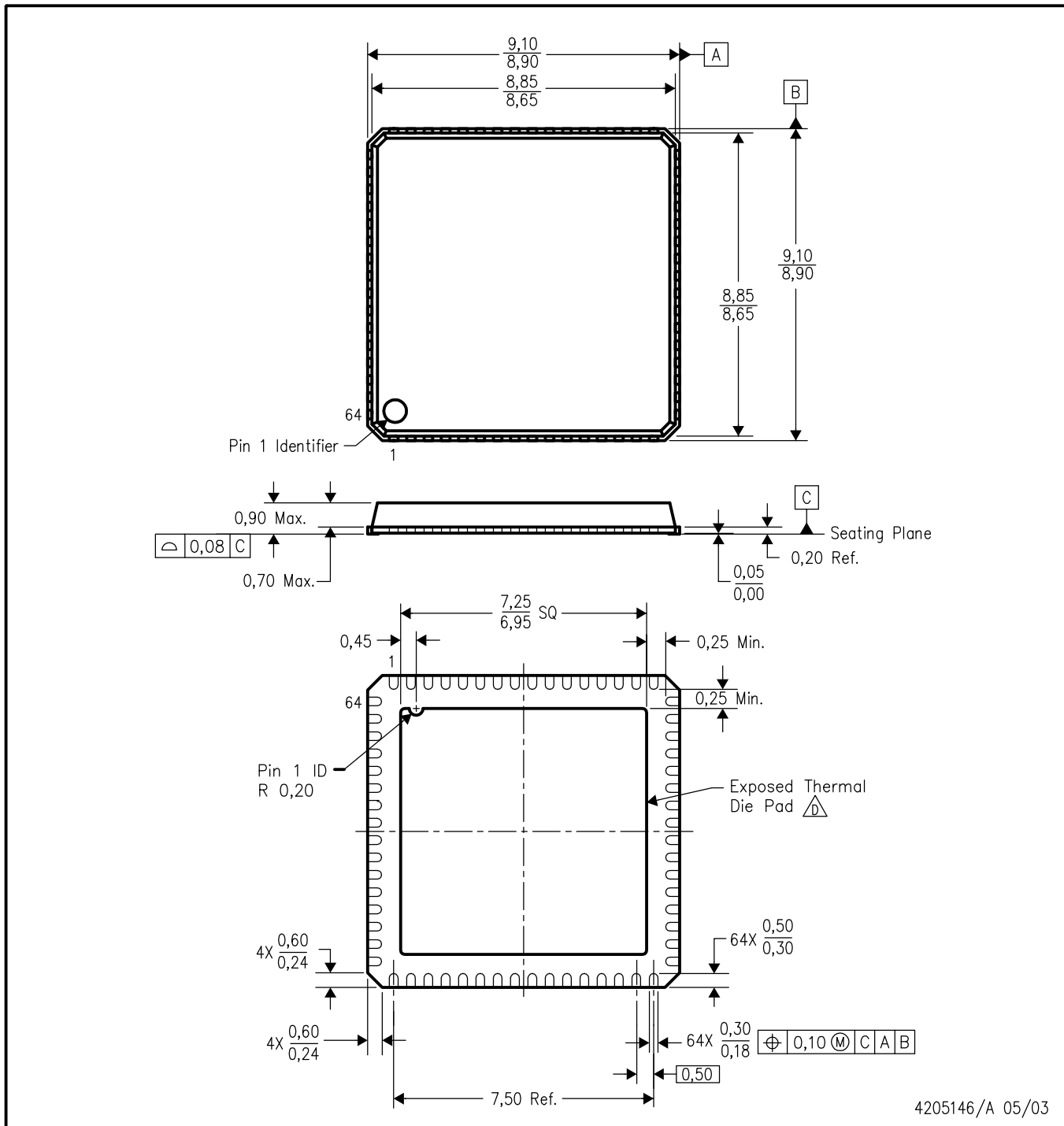


Figure 22. Fuse Check Mode Current, MSP430C41x, MSP430F41x

RTD (S-PQFP-N64)

PLASTIC QUAD FLATPACK

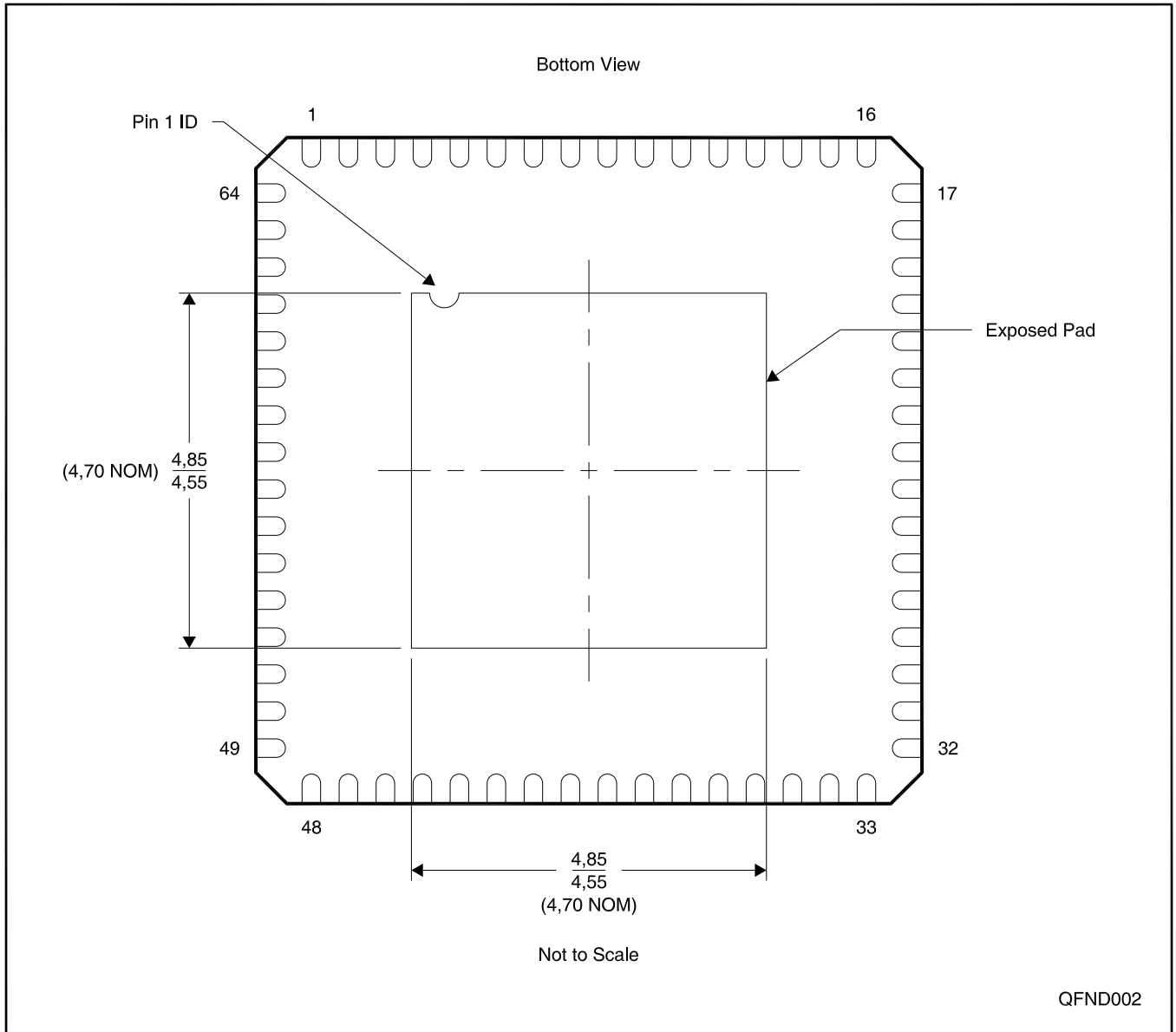


4205146/A 05/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 - △ The Package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad may be electrically connected to ground.

RTD (S-PQFP-N64)

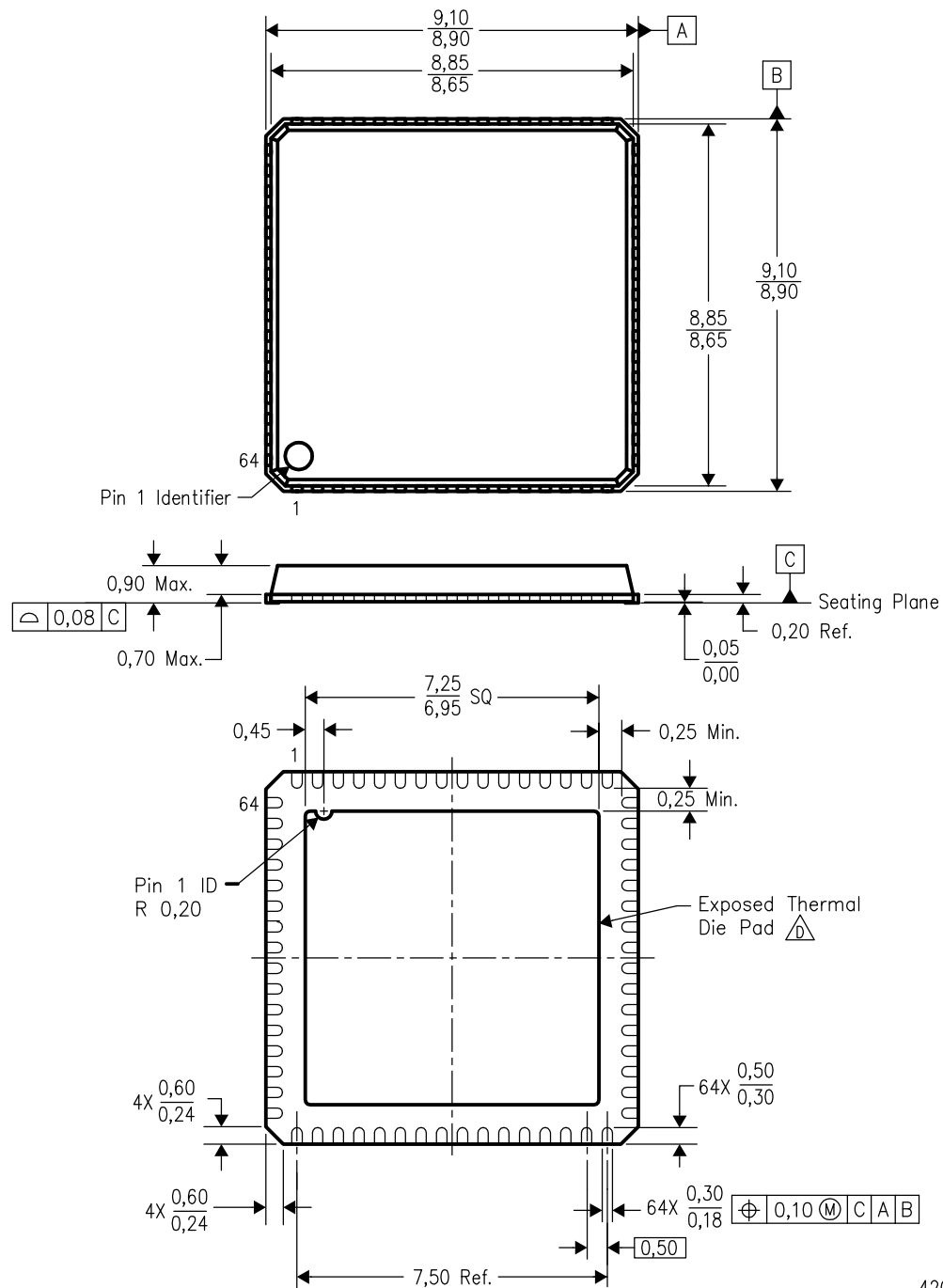
PLASTIC QUAD FLATPACK




- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration
 - D. Soldering the Heat Slug to the printed board surface is recommended.

RTD (S-PQFP-N64)

PLASTIC QUAD FLATPACK

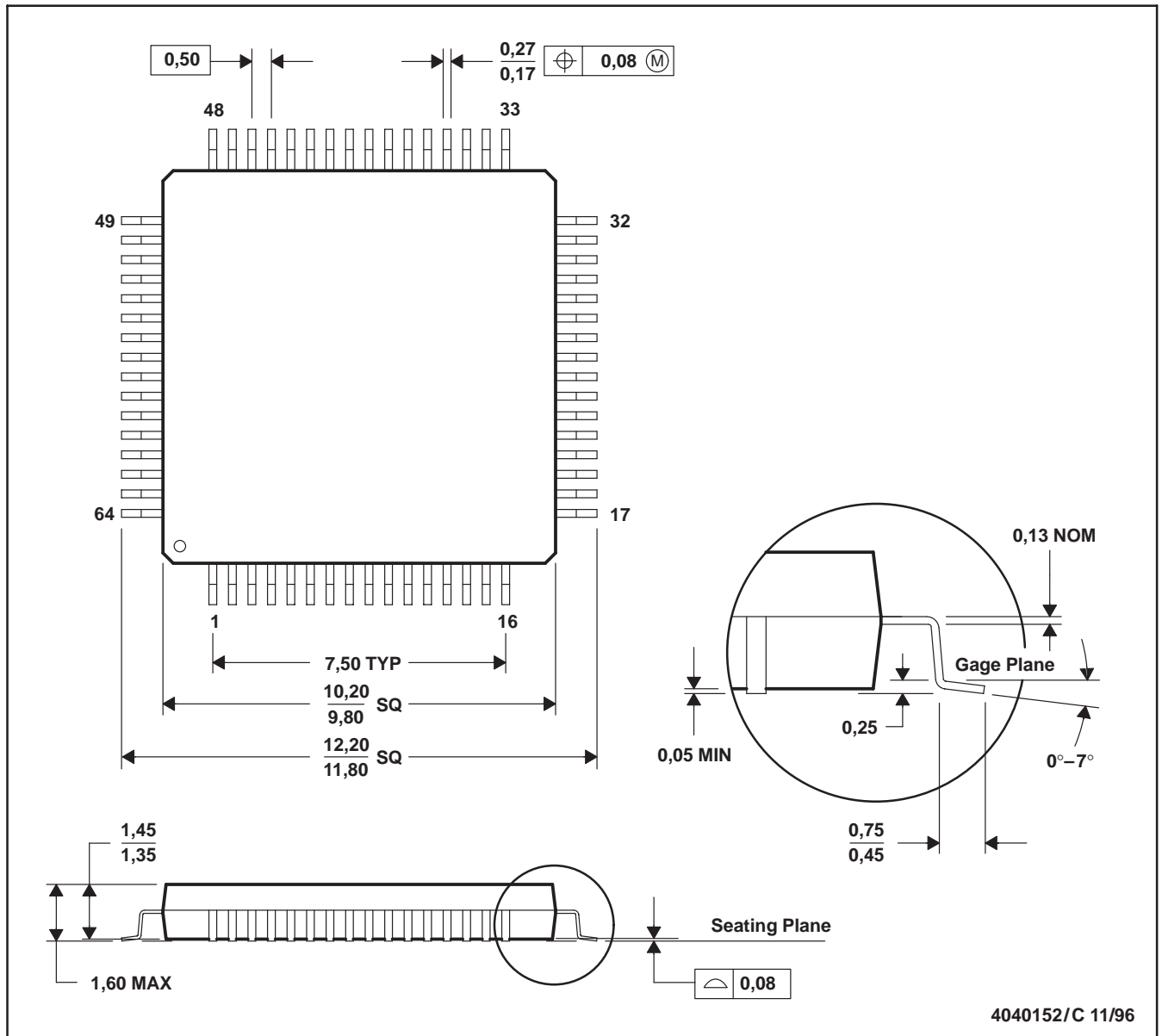


4205146/A 05/03

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) Package configuration.
-  The Package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad may be electrically connected to ground.

PM (S-PQFP-G64)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026
 D. May also be thermally enhanced plastic with leads connected to the die pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| Products | | Applications | |
|------------------|--|---------------------|--|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DSP | dsp.ti.com | Broadband | www.ti.com/broadband |
| Interface | interface.ti.com | Digital Control | www.ti.com/digitalcontrol |
| Logic | logic.ti.com | Military | www.ti.com/military |
| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| | | Telephony | www.ti.com/telephony |
| | | Video & Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265