

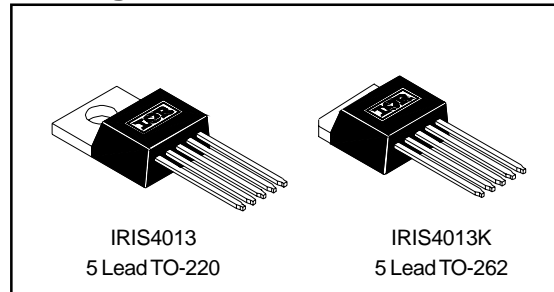
IRIS4013(K)

INTEGRATED SWITCHER

Features

- Primary current mode control, and secondary voltage mode control
- Vcc Over-voltage protection (latched)
- Over-current & over-temperature protection
- Quasi resonant, variable frequency operation
- 5 pin TO-220 and TO-262 package
- 1.95Ω Rds(on) max/ 650V MOSFET
- **Fully Characterized Avalanche Energy**

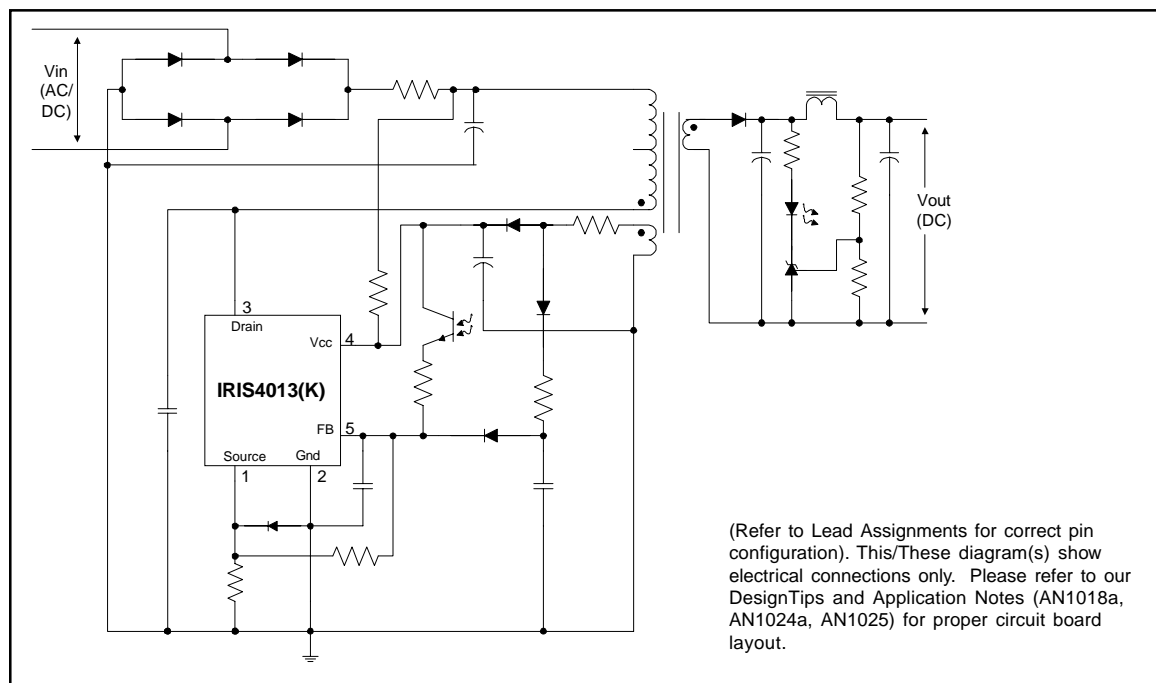
Packages



Descriptions

The IRIS4013(K) is a dual mode voltage and current controller combined with a MOSFET in a single package. The IRIS4013(K) is designed for use in AC/DC switching power supplies up to 230VAC nominal input, and is capable of powers up to 120W for a universal input. The device operates on a quasi-resonant or Pulse Ratio Control (PRC) basis, and thereby variable frequency operation.

Typical Connection Diagram



Absolute Maximum Ratings

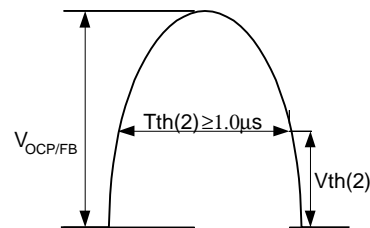
Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to terminals stated, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol | Definition | Terminals | Max. Ratings | Units | Note |
|-------------|--|-----------|--------------|--------------|--|
| I_{Dpeak} | Peak drain current | 3-1 | 12.8 | A | Single pulse |
| I_{Dmax} | Maximum switching current | 3-1 | 5.1 | | $V_{2-3} = 0.78V$ $T_a = -20 \sim +125^\circ C$ |
| E_{AS} | Single pulse avalanche energy | 3-1 | 397 | mJ | single pulse $I_{Lpeak} = 5.1A$ |
| V_{CC} | Power supply voltage | 4-3 | 35 | V | |
| V_{TH} | OCP/FB terminal voltage | 5-2 | 6 | | |
| P_{D1} | Power dissipation for MOSFET | 3-1 | 179 | W | With infinite heatsink |
| | | | 1.3 | | Without heatsink |
| P_{D2} | Power dissipation for control part (MIC) | 4-2 | 0.8 | | Specified by $V_{IN} \times I_{IN}$ |
| R_{thJC} | Thermal resistance, junction to case | — | 0.7 | $^\circ C/W$ | |
| T_J | Junction temperature | — | -40-125 | °C | |
| T_S | Storage temperature | — | -40-125 | | |
| T_f | Internal frame temperature in operation | — | -20-125 | | Refer to recommended operating temperature |
| T_{OP} | Ambient operating temperature | — | -20-125 | | |
| T_L | Lead temp. (soldering, 10 seconds) | — | 300 | | |
| | | | | | |

Recommended Operating Conditions

Time for input of quasi resonant signals.

For the Quasi resonant signal inputted to the $V_{OCP/FB}$ terminal at the time of quasi resonant operation, the signal should be wider than $T_{th}(2)$



Electrical Characteristics (for Control IC)

$V_{CC} = 18V$, ($T_A = 25^{\circ}C$) unless otherwise specified.

| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|-----------------|---|------|------|------|-------------|----------------------|
| V_{CCUV+} | V_{CC} supply undervoltage positive going threshold | 14.4 | 16 | 17.6 | V | |
| V_{CCHYS} | V_{CC} supply undervoltage lockout hysteresis | 5.4 | 6.0 | 6.6 | | |
| I_{QCCUV} | UVLO mode quiescent current | — | — | 100 | μA | $V_{CC} < V_{CCUV+}$ |
| I_{QCC} | Quiescent operating V_{CC} supply current | — | — | 30 | mA | |
| $T_{OFF(MAX)}$ | Maximum OFF time | 40 | — | 60 | μsec | |
| $T_{TH(2)}$ | Minimum input pulse width for quasi resonant signals | — | — | 1.0 | | |
| $T_{OFF(MIN)}$ | Minimum OFF time | — | — | 1.5 | | |
| $V_{TH(1)}$ | OCP/FB terminal threshold voltage 1 | 0.68 | 0.73 | 0.78 | V | |
| $V_{TH(2)}$ | OCP/FB terminal threshold voltage 2 | 1.3 | 1.45 | 1.6 | | |
| $I_{OCP/FB}$ | OCP/FB terminal sink current | 1.1 | 1.35 | 1.7 | mA | |
| $V_{CC(OVP)}$ | V_{CC} overvoltage protection limit | 20.5 | 22.5 | 24.5 | V | |
| $I_{IN(H)}$ | Latch circuit sustaining current | — | — | 400 | μA | |
| $V_{IN(LaOFF)}$ | Latch circuit reset voltage | 6.6 | — | 8.4 | V | |
| $T_{J(TSD)}$ | Thermal shutdown activation temperature | 140 | — | — | $^{\circ}C$ | |

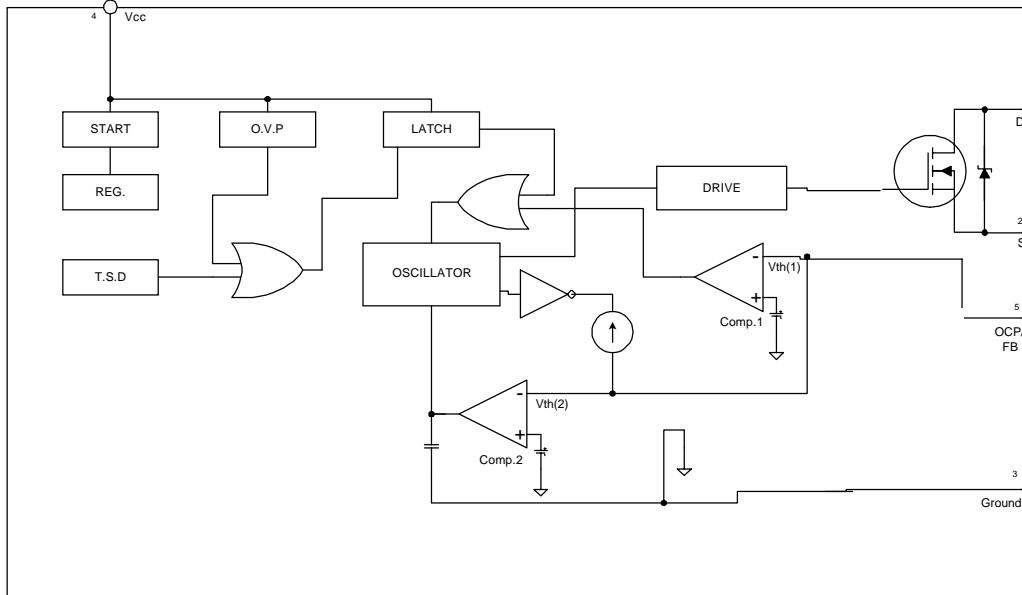
Electrical Characteristics (for MOSFET)

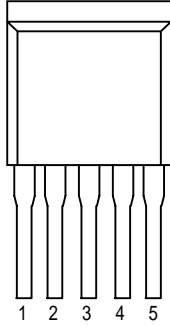
($T_A = 25^{\circ}C$) unless otherwise specified.

| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|----------------|-----------------------------------|------|------|------|---------------|---------------------------|
| V_{DSS} | Drain-to-source breakdown voltage | 650 | — | — | V | |
| I_{DSS} | Drain leakage current | — | — | 300 | μA | $V_{ds}=650V, V_{GS}=0V$ |
| $R_{DS(ON)}$ | On-resistance | — | — | 1.95 | Ω | $V_{3-1}=10V, I_D=5.1A$ |
| t_r | Rise time (10% to 90%) | — | — | 250 | ns | |
| θ_{J-C} | Thermal resistance | — | — | 0.7 | $^{\circ}C/W$ | Between junction and case |

IRIS4013(K)

Block Diagram



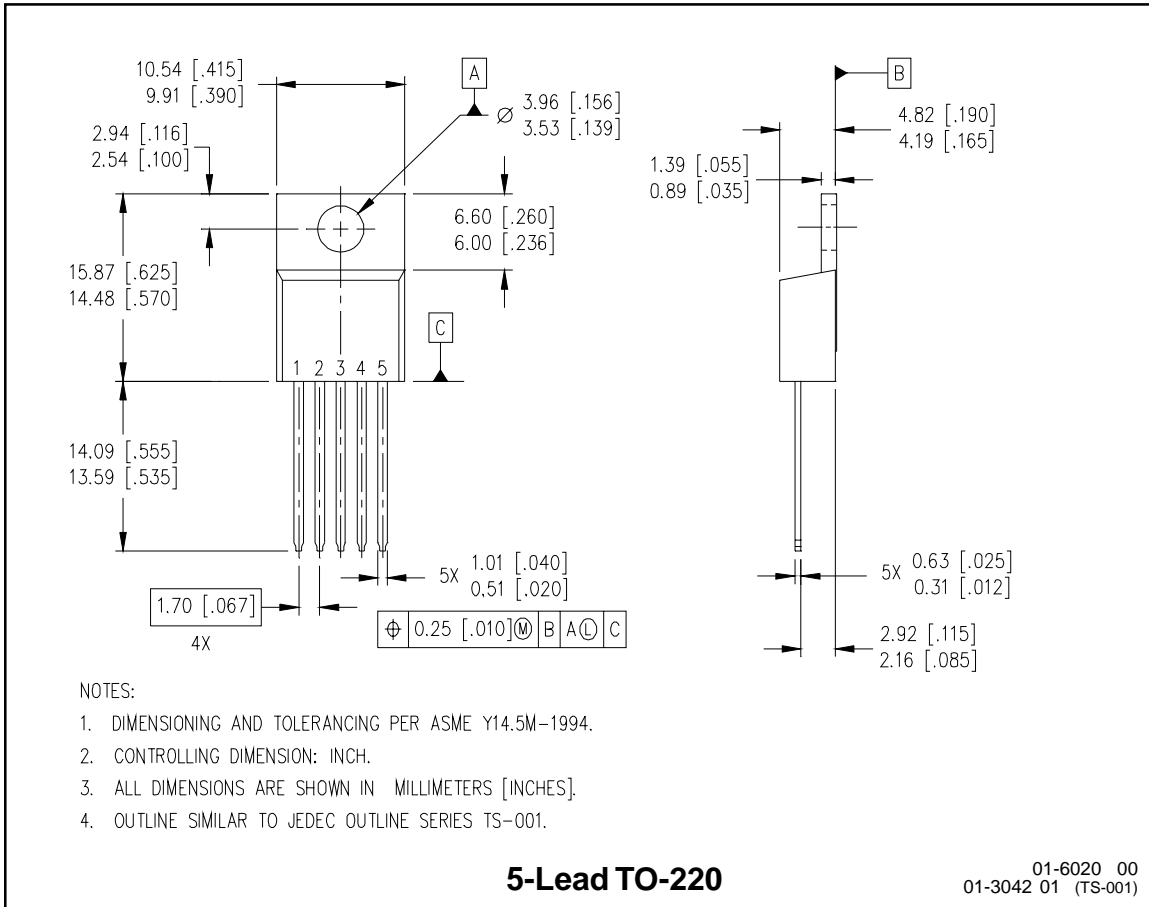
| Lead Assignments | Pin # | Symbol | Description |
|---|-------|--------|---|
|  | 1 | S | MOSFET Source terminal |
| | 2 | Ground | Ground terminal |
| | 3 | D | MOSFET Drain terminal |
| | 4 | Vcc | Control circuit supply voltage |
| | 5 | OCP/FB | Overcurrent detection, and Voltage mode control feedback signal |

Other Functions

O.V.P. – Overvoltage Protection Circuit

T.S.D. – Thermal Shutdown Circuit

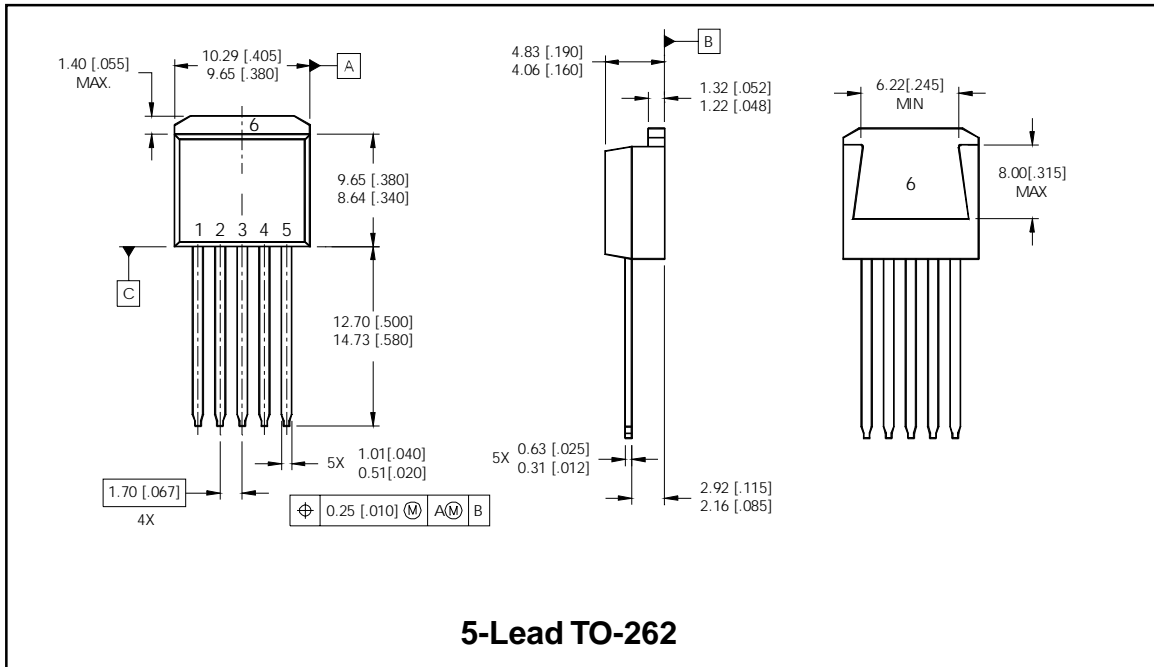
Case outline



IRIS4013(K)

International
IR Rectifier

Case outline



International
IR Rectifier
IR WORLD HEADQUARTERS: 233 Kansas Street, El Segundo, California 90245 Tel: (310) 252-7105
Data and specifications subject to change without notice. 10/16/2001