
SDRAM MODULE

128 MByte (16M x 64 / 72) SDRAM Low Profile
Unbuffered 168 Pin DIMM

General Description:

This memory module is a high performance 128 Megabyte Unbuffered synchronous dynamic RAM module organized as 16M x 64 in a 168 pin Dual In-Line Memory Module (DIMM) package in two Banks. The module utilizes sixteen (16) 2Mx4X8 SDRAM (64ms Refresh) devices in a TSOP II 400 mil package. Also available with ECC option as 16M X 72 in a DIMM package that utilizes eighteen (18) 4Mx4X8 SDRAM devices. A 256 Byte Serial EEPROM contains the module configuration information. The EEPROM can be configured to a customer's specifications.

These modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high rate with automatic column-address generation, interleave between internal banks in order to hide precharge time, and the capability to randomly change column address on each clock cycle during burst.

Features:

- ◆ High density: 128 MB (16M x 64)
 128 MB (16M x 72)
- ◆ Cycle time: 10ns (100 MHz)
- ◆ JEDEC Standard 168 Pin Unbuffered SDRAM DIMM
- ◆ PC-100 Compliant
- ◆ Single power supply of 3.3V ± 10%
- ◆ Serial Presence Detect
- ◆ LVTTL Compatible I/O and Clock
- ◆ Unbuffered Control & Address Lines
- ◆ Auto Precharge and Auto Refresh Modes handled by SDRAM Devices
- ◆ Programmable Burst Type, Burst Length and CAS Latency of SDRAM devices
- ◆ Internal Pipeline Operation
- ◆ Fully Synchronous – all signals registered on positive edge of system clock
- ◆ Package Height: 1.20 inches

Absolute Maximum Ratings*:

Item	Symbol	Rating	Unit
Supply voltage (V_{CC} Relative to V_{SS})	V_{CC}	-1.0 to +4.6	V
Input/Output Voltage	$V_{I/O}$	-1.0 to +4.6	V
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C
Short circuit output current	I_{out}	±50	mA

* Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions:

(Voltage referenced to V_{CC} . $T_A = 0$ to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input high voltage	V_{IH}	2.0	-	$V_{CC}+0.3$	V
Input low voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_A	0	+25	+70	°C

Capacitance:

($T_A=25^\circ\text{C}$, $V_{cc}=3.3\text{V}\pm 0.3\text{V}$, $f = 1 \text{ Mhz}$)

Parameter ¹	Symbol	Min.	Max.	Unit
Input capacitance (Address, WE, RAS, CAS)	C_{IN}	45	68.5	pF
Input capacitance (DQMB0~DQMB7)	C_{IN}	5	15.2	pF
Input capacitance (CK0, CK1, CK2, CK3)	C_{CLK}	10	21	pF
Input capacitance (CS0~CS3)	C_{IN}	10	19	pF
Input capacitance (CKE0, CKE1)	C_{IN}	22.5	34.2	pF
Input/Output capacitance (DQ0~DQ63, CB0~CB7)	$C_{I/O}$	8	13	pF

Pin Names:

CK0-CK3	Clock Inputs	DQ0-DQ63	Data Inputs/Outputs
CKE0	Clock Enables	CB0-CB7	ECC Data Input/Output
/RAS	Row Address Strobe	DQMB0-DQMB7	Data Mask Enables
/CAS	Column Address Strobe	V_{CC}	Power supply
/WE	Write Enable	V_{SS}	Ground
/CS0-/CS3	Chip Select	SCL	Serial Clock
A0-A11	Address Inputs	SDA	Serial Data Input/Output
BA0, BA1	SDRAM Bank Select	SA0-SA2	Decode Input
REGE/NC	Register Enable	WP	Write Protect for SPD
NC or DU	No Connect		

SDRAM DIMM Pinout:

¹ Based on 64Mbit PC100 NEC SDRAM. Manufacturer dependant value.

No.	Designation	No.	Designation	No.	Designation	No.	Designation
1	V _{SS}	43	V _{SS}	85	V _{SS}	127	V _{SS}
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	CS2	87	DQ33	129	CS3*
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V _{CC}	48	DU	90	V _{CC}	132	A13
7	DQ4	49	V _{CC}	91	DQ36	133	V _{CC}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	V _{SS}	54	V _{SS}	96	V _{SS}	138	V _{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V _{CC}	101	DQ45	143	V _{CC}
18	V _{CC}	60	DQ20	102	V _{CC}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	CKE1	105	CB4	147	REG
22	CB1	64	V _{SS}	106	CB5	148	V _{SS}
23	V _{SS}	65	DQ21	107	V _{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V _{CC}	68	V _{SS}	110	V _{CC}	152	V _{SS}
27	WE*	69	DQ24	111	CAS*	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0*	72	DQ27	114	CS1*	156	DQ59
31	DU	73	V _{CC}	115	RAS*	157	V _{CC}
32	V _{SS}	74	DQ28	116	V _{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V _{SS}	120	A7	162	V _{SS}
37	A8	79	CK2	121	A9	163	CK3
38	A10/AP	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	V _{CC}	82	SDA	124	V _{CC}	166	SA1
41	V _{CC}	83	SCL	125	CK1	167	SA2
42	CK0	84	V _{CC}	126	A12	168	V _{CC}

DC Characteristics:
 $(V_{CC} = 3.3V \pm 0.3V, V_{SS} = 0V, T_A = 0 \text{ to } +70^\circ\text{C})$

Parameter ²	Symbol	100MHz Max.	Unit
Operating current (No Burst, $T_{CK} = \text{min.}$, $T_{RC} = \text{min.}$)	I_{CC1}	500	mA
Precharge Standby Current ($CKE = V_{IL}$, $T_{CK} = \text{min.}$ Bank idle) ($CKE = V_{IH}$, $T_{CK} = \text{min.}$ Bank idle)	I_{CC2}	18 450	mA
Active Standby Current ($CKE = V_{IL}$, $T_{CK} = \text{min.}$) ($CKE = V_{IH}$, $T_{CK} = \text{min.}$)	I_{CC3}	60 550	mA
Burst Mode Current ($t_{CK} = \text{min.}$)	I_{CC4}	900	mA
Refresh Current (per Bank) ($t_{CK} = \text{min.}$, $t_{RC} = \text{min.}$, $t_{RRD} = \text{min.}$, Auto Refresh)	I_{CC5}	1000	mA
Self Refresh Current ($CKE = V_{IL}$)	I_{CC6}	18	mA

AC Electrical Characteristics:
 $(T_A = 0^\circ\text{C to } +70^\circ\text{C}, V_{CC} = 3.3V \pm 0.3V, V_{SS} = 0V)$

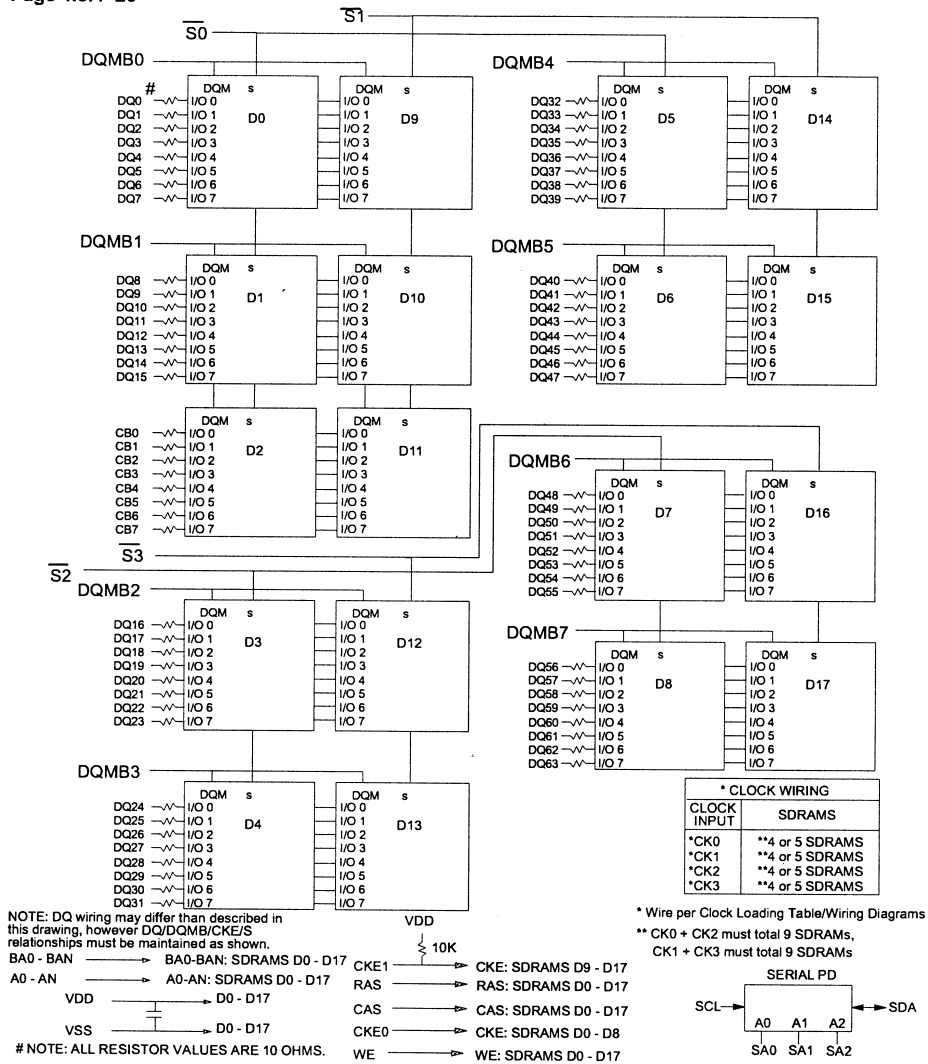
Parameter	Symbol	100MHz Min.	100MHz Max.	Unit
Row to row active delay	t_{RRD}	20		ns
RAS to CAS delay	t_{RCD}	20		ns
Row precharge time	t_{RP}	20		ns
Row active time	t_{RAS}	50	120K	ns
Row cycle time	t_{RC}	70		ns
Last data in to row precharge	t_{RDL}	10		ns
Last data in to new Col. Address delay	t_{CDL}	1		clk
Last data in to burst stop	t_{BDL}	1		clk
Column address to column address delay	t_{CCD}	1		clk
Number of valid output data (CL=3) (CL=2)			2 1	Ea
Clock Cycle Time (CL=3) (CL=2)	t_{CC}	10 10^3		ns
Clock to Valid Output Delay (CL=3) (CL=2)	t_{AC}		6 6	ns
Output Data Hold Time (CL=3) (CL=2)	t_{OH}	3 3		ns
Clock High Pulse Width	t_{CH}	3		ns
Clock Low Pulse Width	t_{CL}	3		ns
Input Setup Time	t_{SI}	2		ns
Input Hold Time	t_{SH}	1		ns
Clock to Output in Low-Z	T_{SLZ}	1		ns
Clock to Output in High-Z	t_{SHZ}		6	ns

² Typical Actual values run lower than Max Spec'ed Values.

³ Available for select SDRAM devices/part numbers.

Functional Block Diagram:

JEDEC Standard No. 21-C
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NOTE: All future designs using this configuration should use Version 2, which reduces the DQMB1 loading from 4 to 3 SDRAMs. See Fig. 4.5.4-AC on P. 4.5.4-30

Figure 4.5.4-S
X72 ECC SDRAM DIMM, 2 Banks with X8 SDRAMs

Release 7c8r9

Part Numbers:

Part number*	Configuration	Clock Speed
KT1672SSN0U-XXL	32M x 72	10ns (100 MHz)
KT1664SSN0U-XXL	32M x 64	10ns (100 MHz)

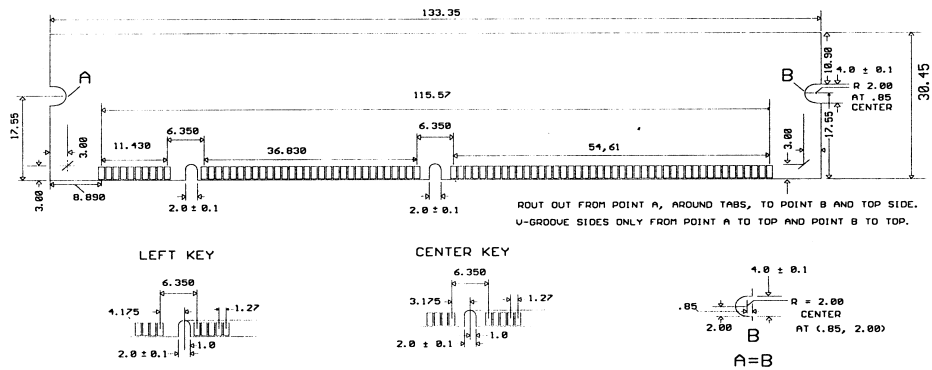
* The "XX" designation relates to the SDRAM manufacturer's device used in production. Please contact Kentron Technologies for more information.

Package Description:

Dimensions (in.):

Length: 5.250

Height: 1.200



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