

IRF7488

HEXFET® Power MOSFET

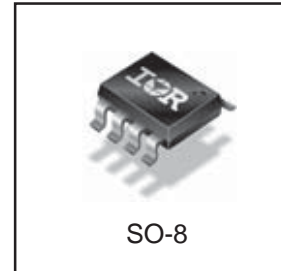
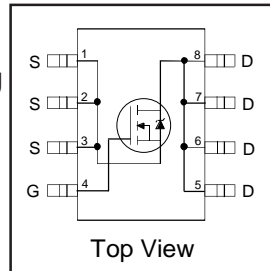
Applications

- High frequency DC-DC converters

V_{DSS}	R_{DS(on)} max	Q_g
80V	29mΩ@V_{GS}=10V	38nC

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{oss} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V _{DS}	Drain-Source Voltage	80	V
V _{GS}	Gate-to-Source Voltage	± 20	
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V	6.3	A
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ 10V	5.0	
I _{DM}	Pulsed Drain Current ^①	50	
P _D @ T _A = 25°C	Maximum Power Dissipation	2.5	W
P _D @ T _A = 70°C	Maximum Power Dissipation	1.6	
	Linear Derating Factor	20	mW/°C
T _J	Operating Junction and Storage Temperature Range	-55 to + 150	°C
T _{STG}	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJL}	Junction-to-Drain Lead	—	20	°C/W
R _{θJA}	Junction-to-Ambient ^④	—	50	

Notes ^① through ^④ are on page 9
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Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	80	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.089	—	V/°C	Reference to 25°C, I _D = 1mA ③
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	24	29	mΩ	V _{GS} = 10V, I _D = 3.8A ③
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 80V, V _{GS} = 0V
		—	—	250		V _{DS} = 64V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V _{GS} = -20V

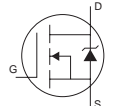
Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	9.3	—	—	S	V _{DS} = 15V, I _D = 3.8A
Q _g	Total Gate Charge	—	38	57	nC	I _D = 3.8A
Q _{gs}	Gate-to-Source Charge	—	9.1	—		V _{DS} = 40V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	12	—		V _{GS} = 10V,
t _{d(on)}	Turn-On Delay Time	—	13	—	ns	V _{DD} = 40V
t _r	Rise Time	—	12	—		I _D = 3.8A
t _{d(off)}	Turn-Off Delay Time	—	44	—		R _G = 9.1Ω
t _f	Fall Time	—	16	—		V _{GS} = 10V ③
C _{iss}	Input Capacitance	—	1680	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	270	—		V _{DS} = 25V
C _{riss}	Reverse Transfer Capacitance	—	32	—		f = 1.0MHz
C _{oss}	Output Capacitance	—	1760	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	170	—		V _{GS} = 0V, V _{DS} = 64V, f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance	—	340	—		V _{GS} = 0V, V _{DS} = 0V to 64V ⑤

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy②	—	96	mJ
I _{AR}	Avalanche Current①	—	3.8	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	2.3	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	50		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 3.8A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	—	65	98	ns	T _J = 25°C, I _F = 3.8A
Q _{rr}	Reverse Recovery Charge	—	190	290	nC	di/dt = 100A/μs ③

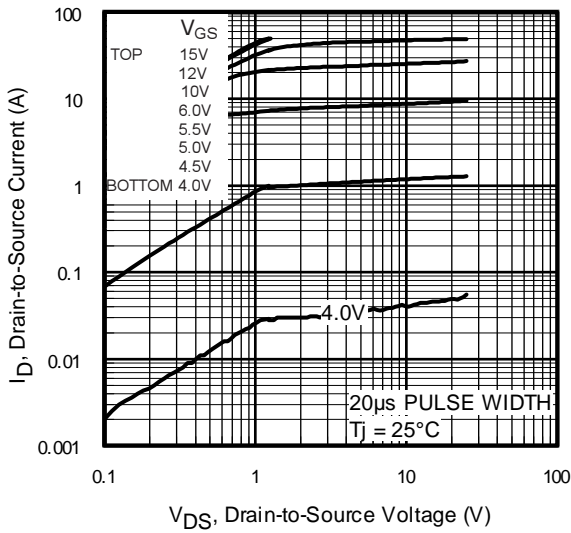


Fig 1. Typical Output Characteristics

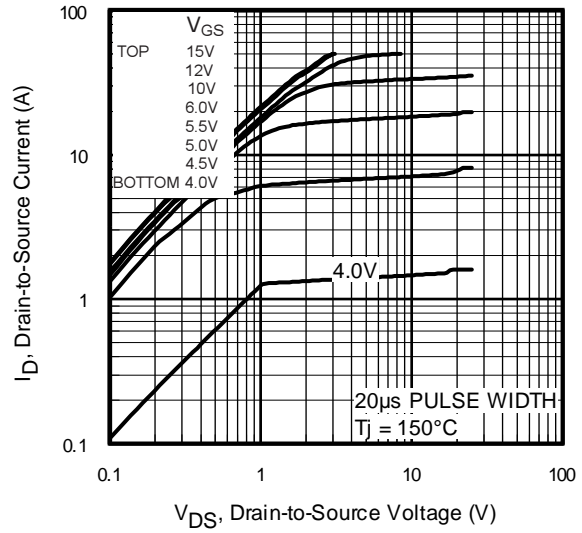


Fig 2. Typical Output Characteristics

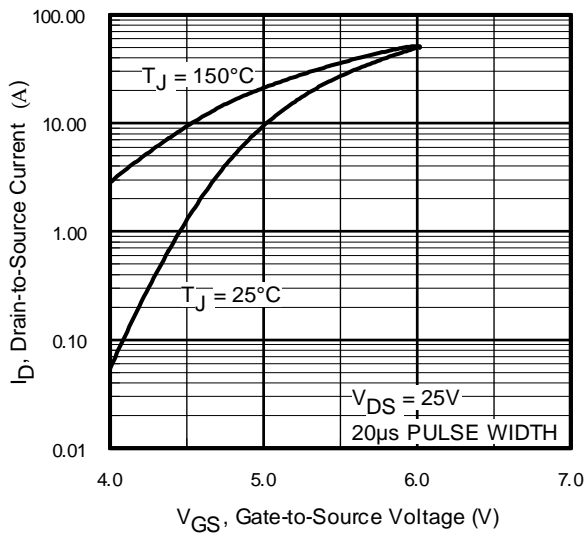


Fig 3. Typical Transfer Characteristics

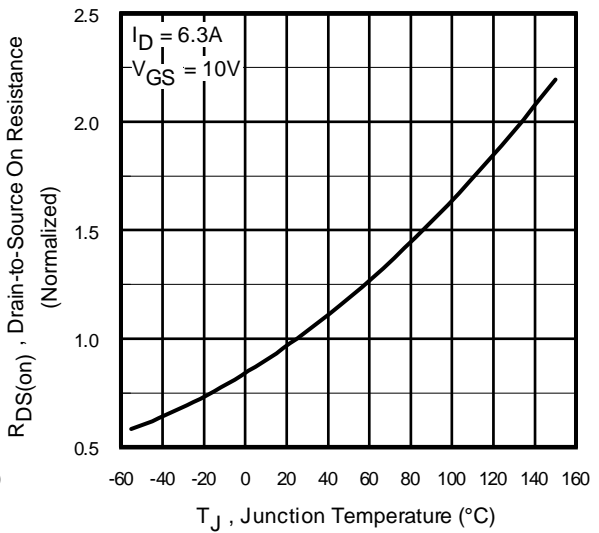


Fig 4. Normalized On-Resistance Vs. Temperature

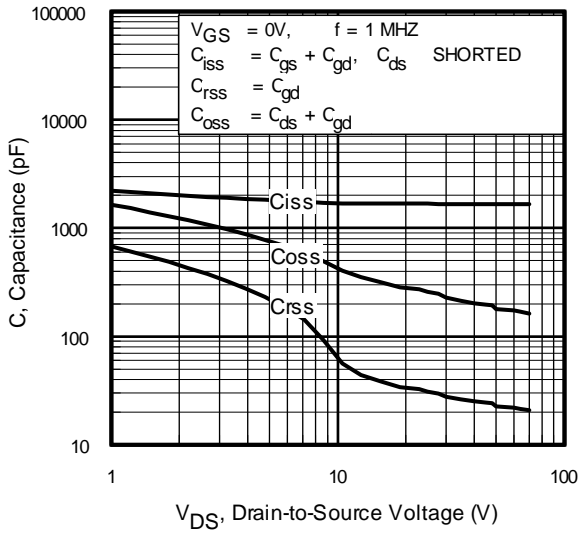


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

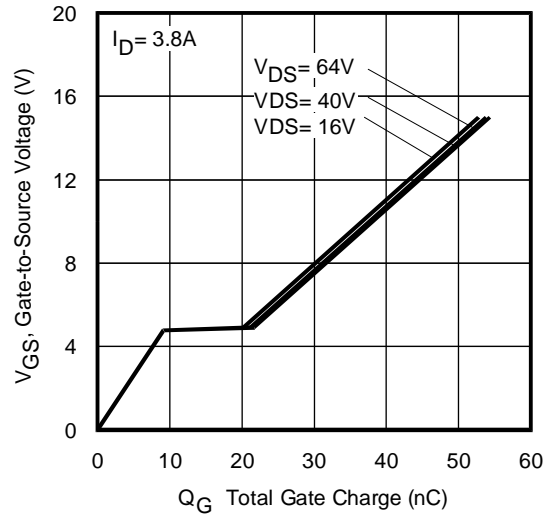


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

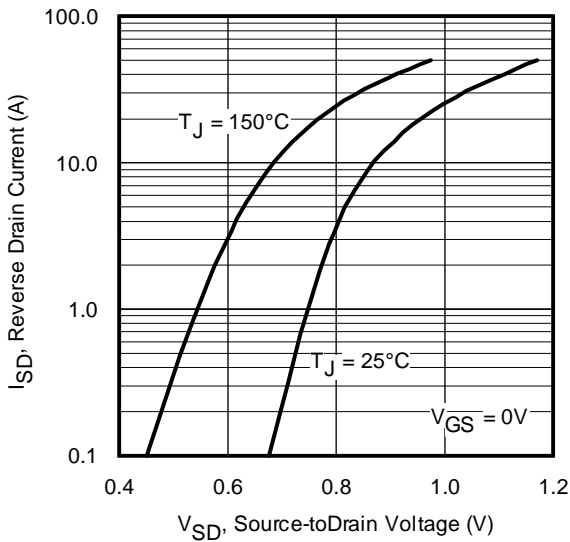


Fig 7. Typical Source-Drain Diode Forward Voltage

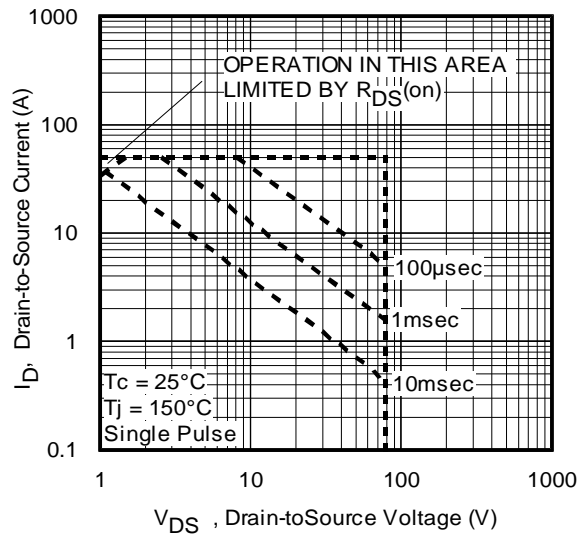


Fig 8. Maximum Safe Operating Area

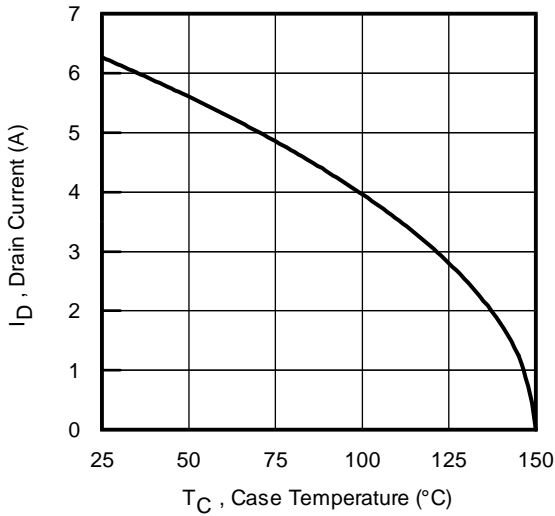


Fig 9. Maximum Drain Current Vs. Ambient Temperature

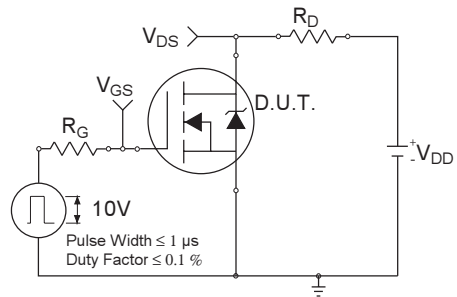


Fig 10a. Switching Time Test Circuit

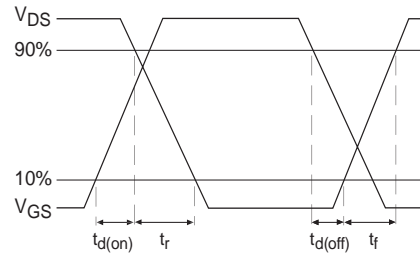


Fig 10b. Switching Time Waveforms

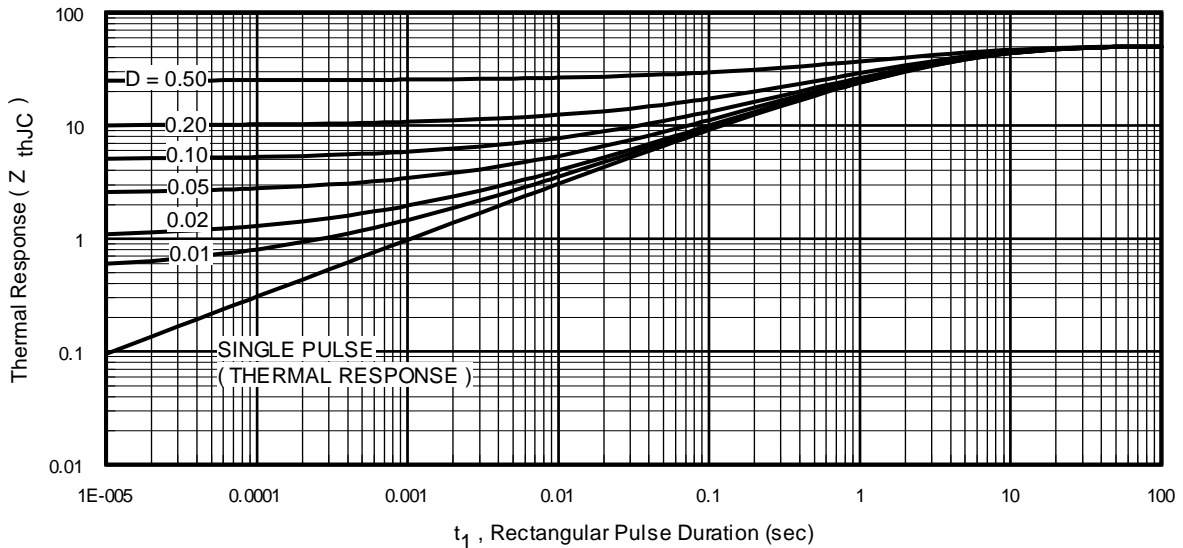


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

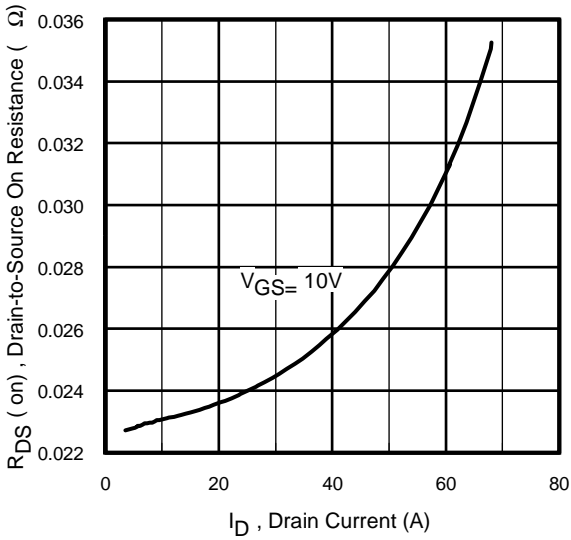


Fig 12. On-Resistance Vs. Drain Current

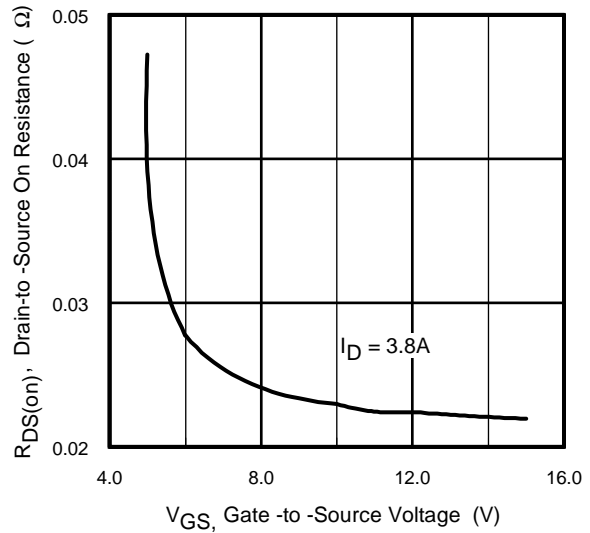


Fig 13. On-Resistance Vs. Gate Voltage

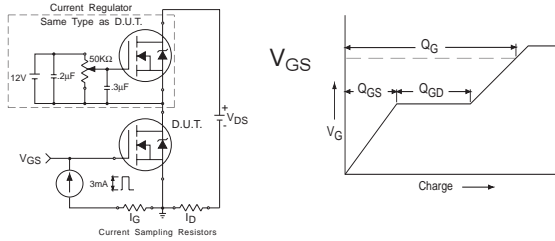


Fig 14a&b. Basic Gate Charge Test Circuit and Waveform

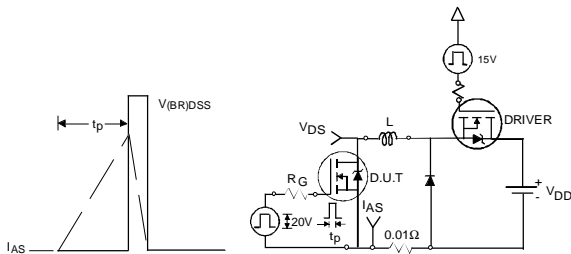


Fig 15a&b. Unclamped Inductive Test circuit and Waveforms

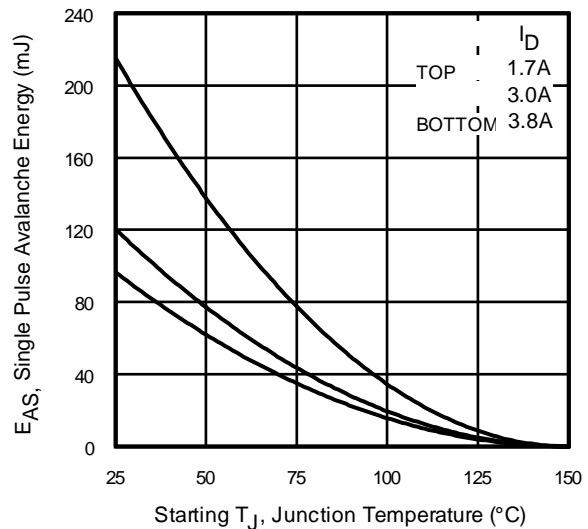


Fig 15c. Maximum Avalanche Energy Vs. Drain Current

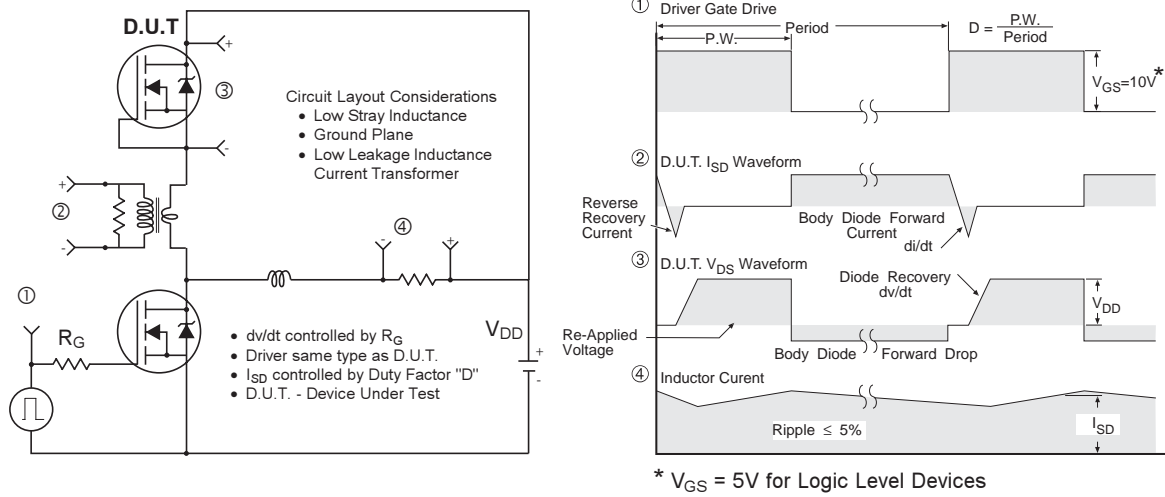


Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

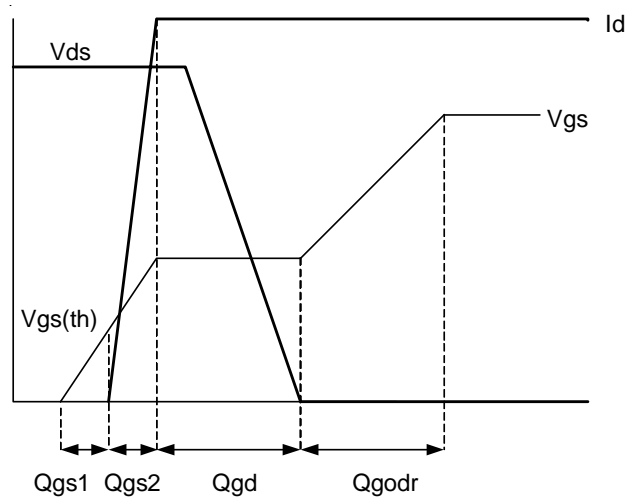
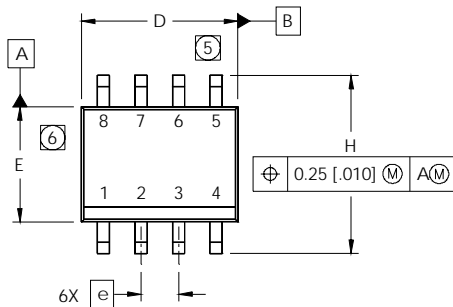
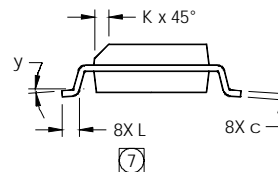
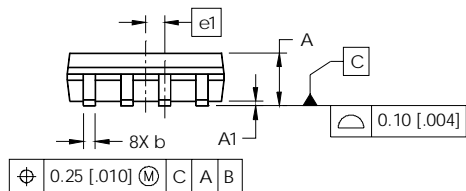


Fig 17. Gate Charge Waveform

SO-8 Package Details



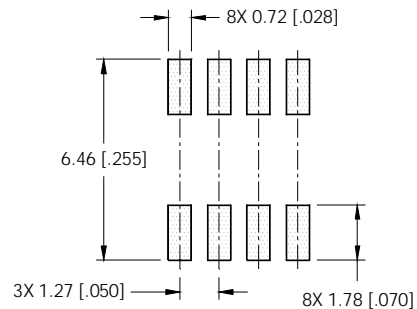
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



NOTES:

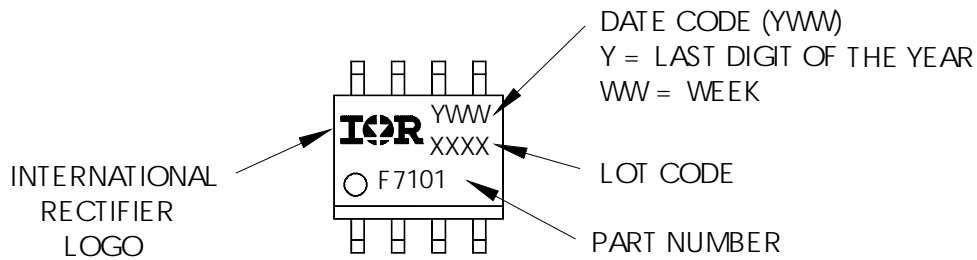
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA
- ⑤ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [0.006].
- ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [0.010].
- ⑦ DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT

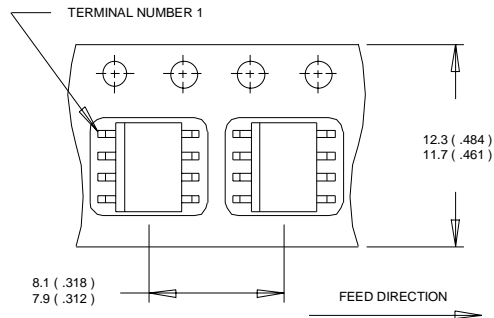


SO-8 Part Marking

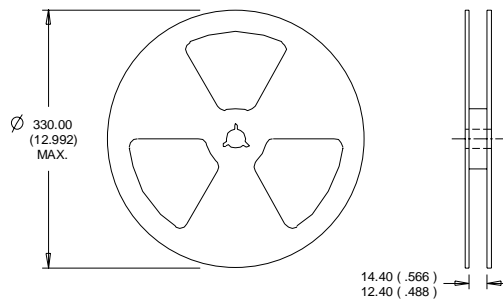
EXAMPLE: THIS IS AN IRF7101 (MOSFET)



SO-8 Tape and Reel



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 13\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 3.8\text{A}$.
- ③ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ When mounted on 1 inch square copper board
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Industrial market.
 Qualification Standards can be found on IR's Web site.