

MM74HCT273

Octal D-Type Flip-Flop with Clear

General Description

The MM74HCT273 utilizes advanced silicon-gate CMOS technology. It has an input threshold and output drive similar to LS-TTL with the low standby power of CMOS.

These positive edge-triggered flip-flops have a common clock and clear-independent Q outputs. Data on a D input, having the specified set-up and hold time, is transferred to the corresponding Q output on the positive-going transition of the clock pulse. The asynchronous clear forces all outputs LOW when it is LOW.

All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground.

MM74HCT devices are intended to interface TTL and NMOS components to CMOS components. These parts can be used as plug-in replacements to reduce system power consumption in existing designs.

Features

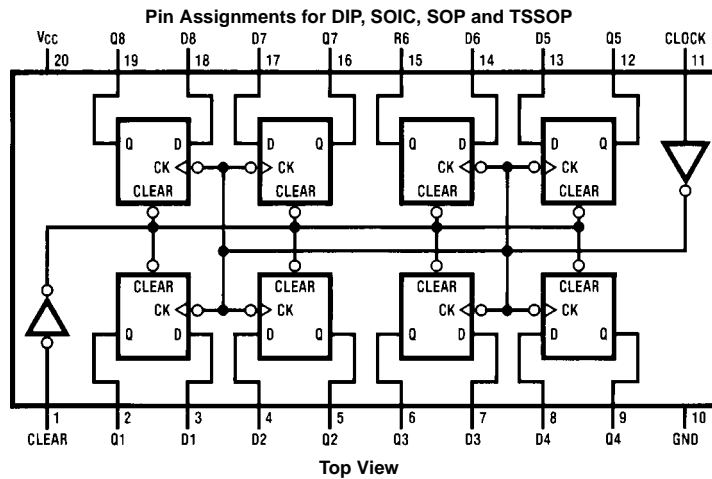
- Typical propagation delay: 20 ns
- Low quiescent current: 80 μ A maximum (74HCT series)
- Fanout of 10 LS-TTL loads

Ordering Code:

| Order Number | Package Number | Package Description |
|---------------|----------------|---|
| MM74HCT273WM | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| MM74HCT273SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| MM74HCT273MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| MM74HCT273N | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



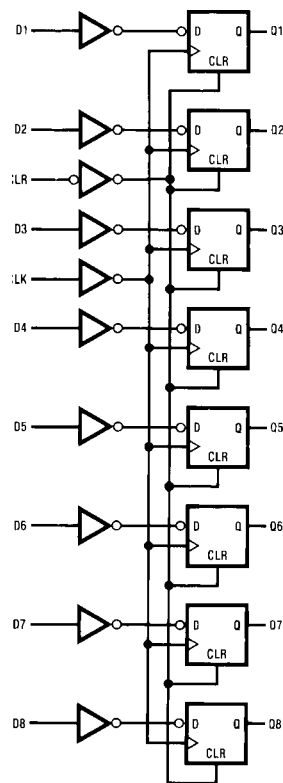
Truth Table

(Each Flip-Flop)

| Inputs | | | Outputs |
|--------|-------|---|---------|
| Clear | Clock | D | Q |
| L | X | X | L |
| H | ↑ | H | H |
| H | ↑ | L | L |
| H | L | X | Q0 |

H = HIGH Level (steady-state)
 L = LOW Level (steady-state)
 X = Don't Care
 ↑ = Transition from LOW-to-HIGH level
 Q0 = The level of Q before the indicated steady-state input conditions were established.

Logic Diagram



| Absolute Maximum Ratings ^(Note 1) | | Recommended Operating Conditions | | | |
|--|-------------------------------------|--|------------|------------|--------------|
| (Note 2) | | | Min | Max | Units |
| Supply Voltage (V_{CC}) | -0.5V to +7.0V | Supply Voltage (V_{CC}) | 4.5 | 5.5 | V |
| DC Input Voltage (V_{IN}) | -1.5V to $V_{CC} + 1.5V$ | DC Input or Output Voltage | | | |
| DC Output Voltage (V_{OUT}) | -0.5V to $V_{CC} + 0.5V$ | (V_{IN}, V_{OUT}) | 0 | V_{CC} | V |
| Clamp Diode Current (I_{IK}, I_{OK}) | ± 20 mA | Operating Temperature Range (T_A) | -40 | +85 | $^{\circ}C$ |
| DC Output Current, per Pin (I_{OUT}) | ± 25 mA | Input Rise or Fall Times | | | |
| DC V_{CC} or GND Current, per Pin (I_{CC}) | ± 50 mA | (t_r, t_f) | | 500 | ns |
| Storage Temperature Range (T_{STG}) | -65 $^{\circ}C$ to +150 $^{\circ}C$ | Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur. | | | |
| Power Dissipation (P_D) | | Note 2: Unless otherwise specified all voltages are referenced to ground. | | | |
| (Note 3) | 600 mW | Note 3: Power dissipation temperature derating—plastic "N" package: -12 mW/ $^{\circ}C$ from 65 $^{\circ}C$ to 85 $^{\circ}C$. | | | |
| S.O. Package only | 500 mW | | | | |
| Lead Temperature (T_L) | | | | | |
| (Soldering, 10 seconds) | 260 $^{\circ}C$ | | | | |

DC Electrical Characteristics

$V_{CC} = 5V \pm 10\%$ unless otherwise specified

| Symbol | Parameter | Conditions | $T_A = 25^{\circ}C$ | | $T_A = -40^{\circ}C$ to $85^{\circ}C$ | $T_A = -55^{\circ}C$ to $125^{\circ}C$ | Units |
|----------|-----------------------------------|--|---------------------|-------------------|---------------------------------------|--|---------|
| | | | Typ | Guaranteed Limits | | | |
| V_{IH} | Minimum HIGH Level Input Voltage | | | 2.0 | 2.0 | 2.0 | V |
| V_{IL} | Maximum LOW Level Input Voltage | | | 0.8 | 0.8 | 0.8 | V |
| V_{OH} | Minimum HIGH Level Output Voltage | $V_{IN} = V_{IH}$ or V_{IL} | V_{CC} | $V_{CC}-0.1$ | $V_{CC}-0.1$ | $V_{CC}-0.1$ | V |
| | | $ I_{OUT} = 20 \mu A$ | 4.2 | 3.98 | 3.84 | 3.7 | V |
| | | $ I_{OUT} = 4.0$ mA, $V_{CC} = 4.5V$ | 5.2 | 4.98 | 4.84 | 4.7 | V |
| V_{OL} | Minimum LOW Level Voltage | $V_{IN} = V_{IH}$ or V_{IL} | 0 | 0.1 | 0.1 | 0.1 | V |
| | | $ I_{OUT} = 20 \mu A$ | 0.2 | 0.26 | 0.33 | 0.4 | V |
| | | $ I_{OUT} = 4.0$ mA, $V_{CC} = 4.5V$ | 0.2 | 0.26 | 0.33 | 0.4 | V |
| I_{IN} | Maximum Input Current | $V_{IN} = V_{CC}$ or GND, V_{IH} or V_{IL} | | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| | | $V_{IN} = V_{CC}$ or GND | | 8 | 80 | 160 | μA |
| I_{CC} | Maximum Quiescent Supply Current | $I_{OUT} = 0 \mu A$ | | 0.6 | 0.8 | 0.9 | mA |
| | | $V_{IN} = 2.4V$ or $0.5V$ (Note 4) | | | | | |

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics $V_{CC} = 5V, T_A = 25^\circ C, C_L = 15 \text{ pF}, t_r = t_f = 6 \text{ ns}$

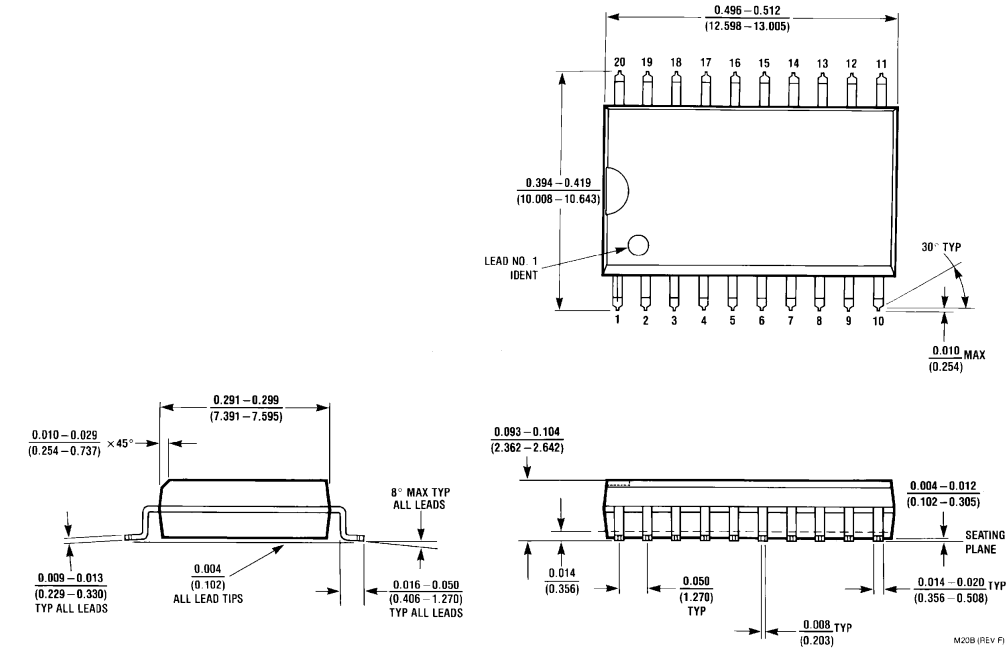
| Symbol | Parameter | Conditions | Typ | Guaranteed Limits | Units |
|--------------------|---|------------|-----|-------------------|-------|
| f_{MAX} | Maximum Operating Frequency | | 68 | 30 | MHz |
| t_{PHL}, t_{PLH} | Maximum Propagation Delay from Clock to Q | | 18 | 30 | ns |
| t_{PHL}, t_{PLH} | Maximum Propagation Delay from Clear to Q | | 21 | 30 | ns |
| t_{REM} | Minimum Removal Time, Clear to Clock | | -1 | 5 | ns |
| t_S | Minimum Set-Up Time D to Clock | | 6 | 20 | ns |
| t_H | Minimum Hold Time Clock to D | | -3 | 5 | ns |
| t_W | Minimum Pulse Width Clock or Clear | | 10 | 16 | ns |

AC Electrical Characteristics $V_{CC} = 5.0V \pm 10\%, C_L = 50 \text{ pF}, t_r = t_f = 6 \text{ ns}$ unless otherwise specified

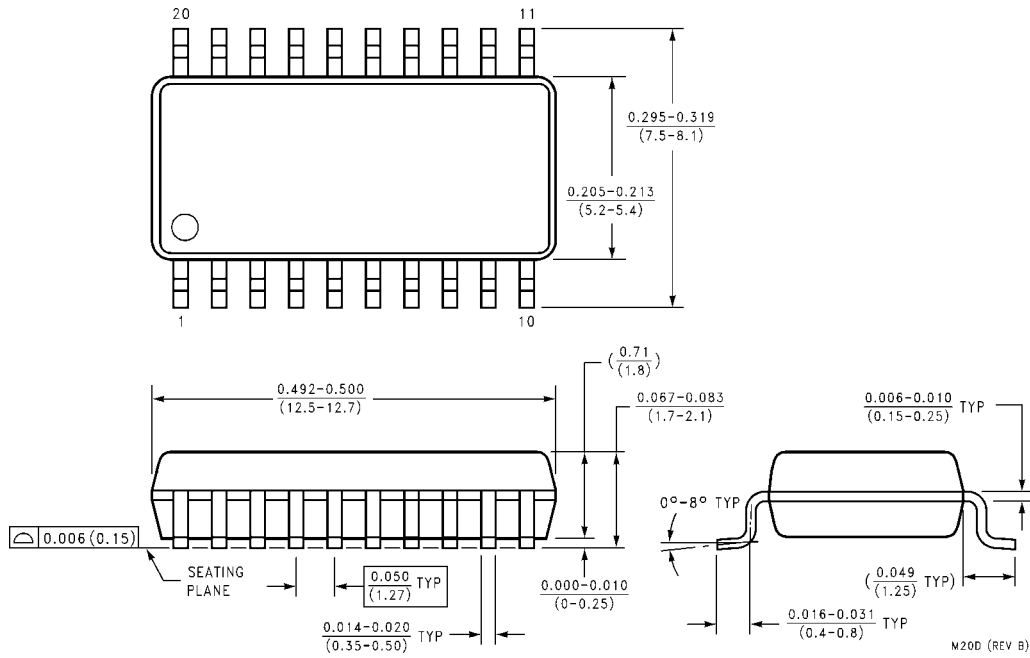
| Symbol | Parameter | Conditions | $T_A = 25^\circ C$ | | $T_A = -40^\circ C \text{ to } 85^\circ C$ | $T_A = -55^\circ C \text{ to } 125^\circ C$ | Units |
|--------------------|---|-----------------|--------------------|-------------------|--|---|-------|
| | | | Typ | Guaranteed Limits | | | |
| f_{MAX} | Maximum Operating Frequency | | 68 | 27 | 21 | 18 | MHz |
| t_{PHL}, t_{PLH} | Maximum Propagation Delay from Clock to Q | | 22 | 37 | 46 | 56 | ns |
| t_{PHL}, t_{PLH} | Maximum Propagation Delay from Clear to Q | | 25 | 35 | 44 | 52 | ns |
| t_{REM} | Minimum Removal Time Clear to Clock | | -1 | 5 | 6 | 7 | ns |
| t_S | Minimum Set-Up Time D to Clock | | 6 | 20 | 25 | 30 | ns |
| t_H | Minimum Hold Time Clock to D | | -3 | 5 | 5 | 5 | ns |
| t_W | Minimum Pulse Width Clock or Clear | | 10 | 16 | 25 | 30 | ns |
| t_r, t_f | Maximum Input Rise and Fall Time, Clock | | | 500 | 500 | 500 | ns |
| t_{THL}, t_{TLH} | Maximum Output Rise and Fall Time | | 11 | 15 | 19 | 22 | ns |
| C_{PD} | Power Dissipation Capacitance (Note 5) | (Per Flip-Flop) | 50 | | | | pF |
| C_{IN} | Maximum Input Capacitance | | 6 | 10 | 10 | 10 | pF |

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC}^2 f + I_{CC}$.

Physical Dimensions inches (millimeters) unless otherwise noted

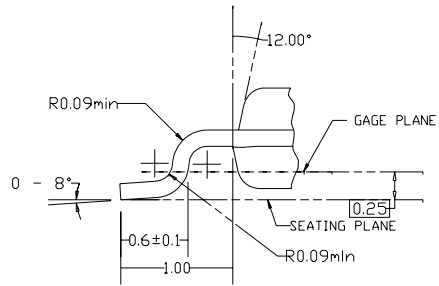
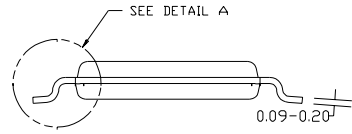
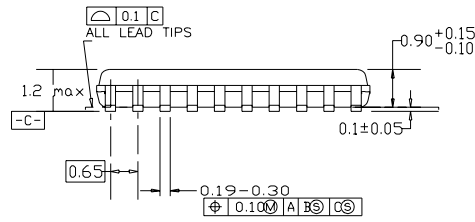
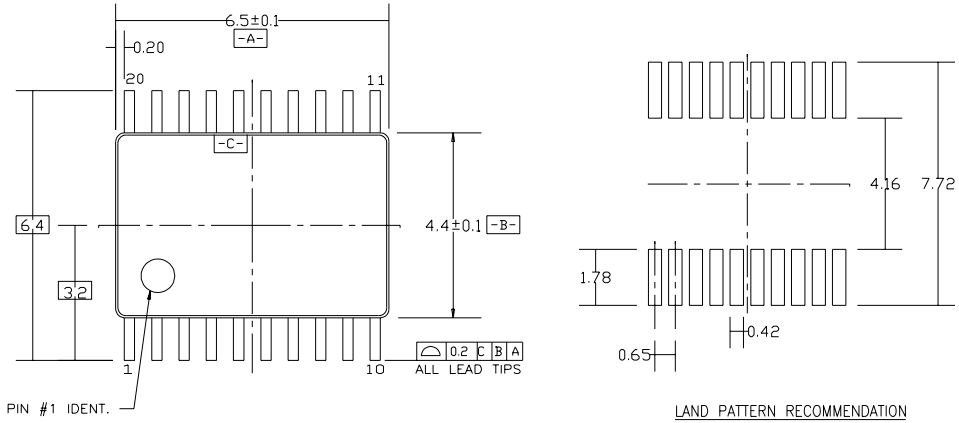


20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Package Number M20B



20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



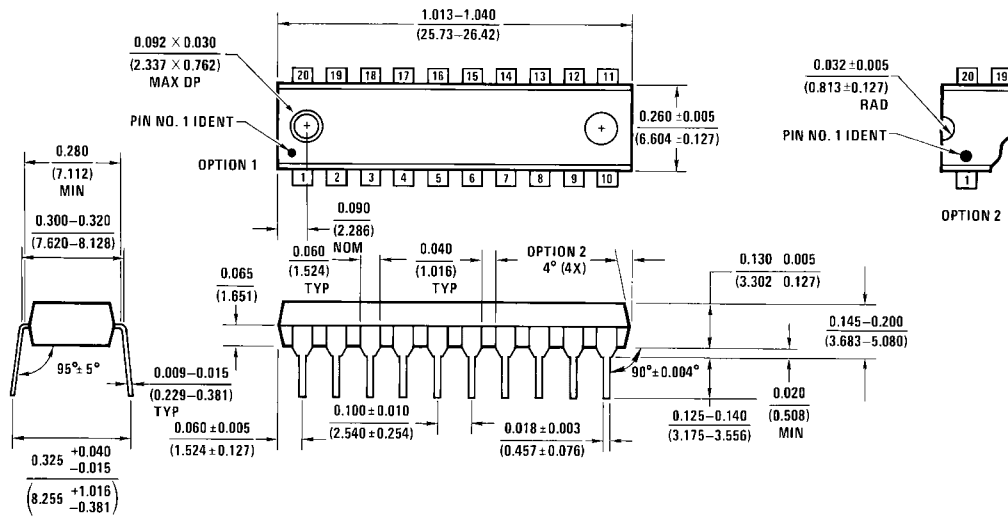
DETAIL A

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A**

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com