- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 20-μA Max I_{CC}**

- **Typical t_{pd} = 7 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**
- **Unbuffered Outputs**

SN54HCU04 . . . J OR W PACKAGE
SN74HCU04 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)

```
        ┌───∪───┐
 1A  [ 1      14 ] V_CC
 1Y  [ 2      13 ] 6A
 2A  [ 3      12 ] 6Y
 2Y  [ 4      11 ] 5A
 3A  [ 5      10 ] 5Y
 3Y  [ 6       9 ] 4A
 GND [ 7       8 ] 4Y
        └───────┘
```
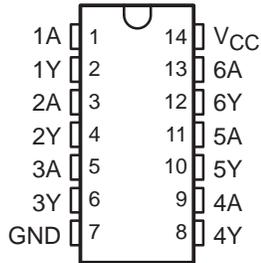
SN54HCU04 . . . FK PACKAGE
(TOP VIEW)

```
          1Y  1A  NC  V_CC 6A
           3   2   1  20  19
  2A  [ 4              18 ] 6Y
  NC  [ 5              17 ] NC
  2Y  [ 6              16 ] 5A
  NC  [ 7              15 ] NC
  3A  [ 8              14 ] 5Y
           9  10  11  12  13
          3Y  GND  NC  4Y  4A
```
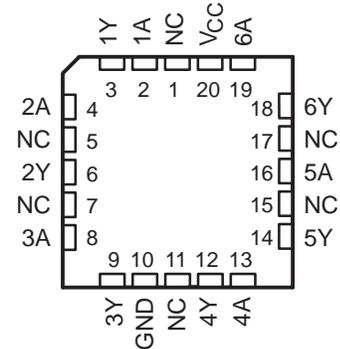
NC – No internal connection

description/ordering information

The 'HCU04 devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP – N	Tube of 25	SN74HCU04N	SN74HCU04N
	SOIC – D	Tube of 50	SN74HCU04D	HCU04
		Reel of 2500	SN74HCU04DR	
		Reel of 250	SN74HCU04DT	
	SOP – NS	Reel of 2000	SN74HCU04NSR	HCU04
	SSOP – DB	Reel of 2000	SN74HCU04DBR	HU04
	TSSOP – PW	Reel of 90	SN74HCU04PW	HCU04
		Reel of 2000	SN74HCU04PWR	
		Reel of 250	SN74HCU04PWT	
−55°C to 125°C	CDIP – J	Tube of 25	SNJ54HCU04J	SNJ54HCU04J
	CFP – W	Tube of 150	SNJ54HCU04W	SNJ54HCU04W
	LCCC – FK	Tube of 55	SNJ54HCU04FK	SNJ54HCU04FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram (positive logic)

A ———————▷○——— Y
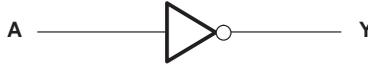
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) .... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) .... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±25 mA
Continuous current through V_{CC} or GND .... ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package .... 86°C/W
DB package .... 96°C/W
N package .... 80°C/W
NS package .... 76°C/W
PW package .... 113°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54HCU04			SN74HCU04			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.7			1.7			V
		$V_{CC} = 4.5$ V	3.6			3.6			
		$V_{CC} = 6$ V	4.8			4.8			
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V			0.5			0.5	V
		$V_{CC} = 4.5$ V			1.35			1.35	
		$V_{CC} = 6$ V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time	$V_{CC} = 2$ V			1000			1000	ns
		$V_{CC} = 4.5$ V			500			500	
		$V_{CC} = 6$ V			400			400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TEXAS INSTRUMENTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCU04		SN74HCU04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{CC} or GND	I_{OH} = −20 µA	2 V	1.8			1.8		1.8		V
			4.5 V	4			4		4		
			6 V	5.5			5.5		5.5		
		I_{OH} = −4 mA	4.5 V	3.98			3.7		3.84		
		I_{OH} = −5.2 mA	6 V	5.48			5.2		5.34		
V_{OL}	V_I = V_{CC} or GND	I_{OL} = 20 µA	2 V			0.2		0.2		0.2	V
			4.5 V			0.5		0.5		0.5	
			6 V			0.5		0.5		0.5	
		I_{OL} = 4 mA	4.5 V			0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V			0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V			±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			2		40		20	µA
C_i			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCU04		SN74HCU04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		40	80		120		100	ns
			4.5 V		8	16		24		20	
			6 V		7	14		20		17	
t_f		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per inverter	No load	20	pF

TEXAS
INSTRUMENTS

SN54HCU04, SN74HCU04
HEX INVERTERS

PARAMETER MEASUREMENT INFORMATION

From Output Under Test ● Test Point

C_L = 50 pF
(see Note A)

LOAD CIRCUIT

Input 50% 50% V_{CC} 0 V

t_{PLH} t_{PHL}

In-Phase Output 50% 10% 90% 90% 50% 10% V_{OH} V_{OL}

t_r† t_f

t_{PHL} t_{PLH}

Out-of-Phase Output 90% 50% 10% 50% 10% 90% V_{OH} V_{OL}

t_f t_r†

† t_r is not applicable to 'HCU devices.

Input 50% 10% 90% 90% 50% 10% V_{CC} 0 V

t_r t_f

**VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES**

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

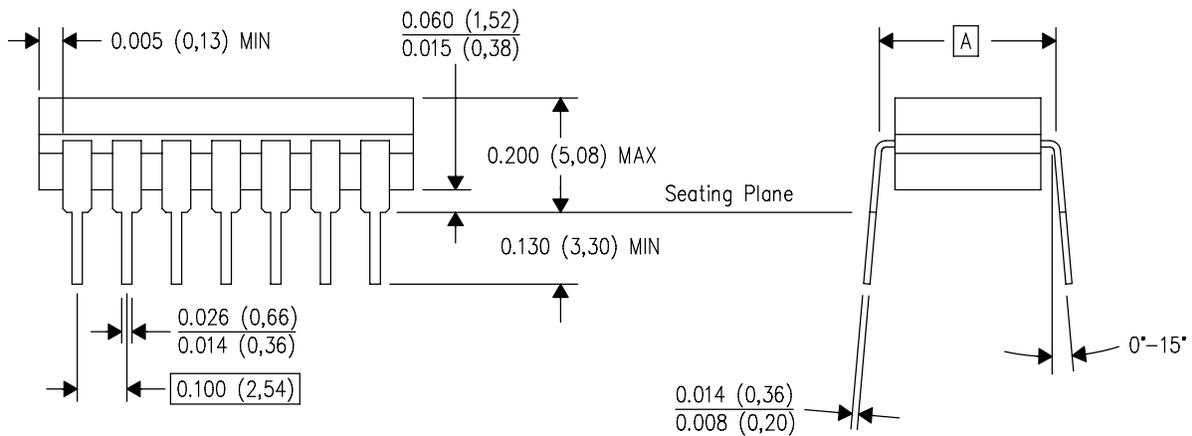**Figure 1. Load Circuit and Voltage Waveforms**
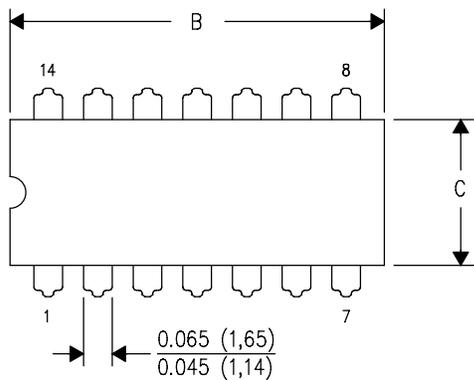
DIM ╲ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14　　　　　　　　8

C

1　　　　　　　7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

A

0°–15°

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

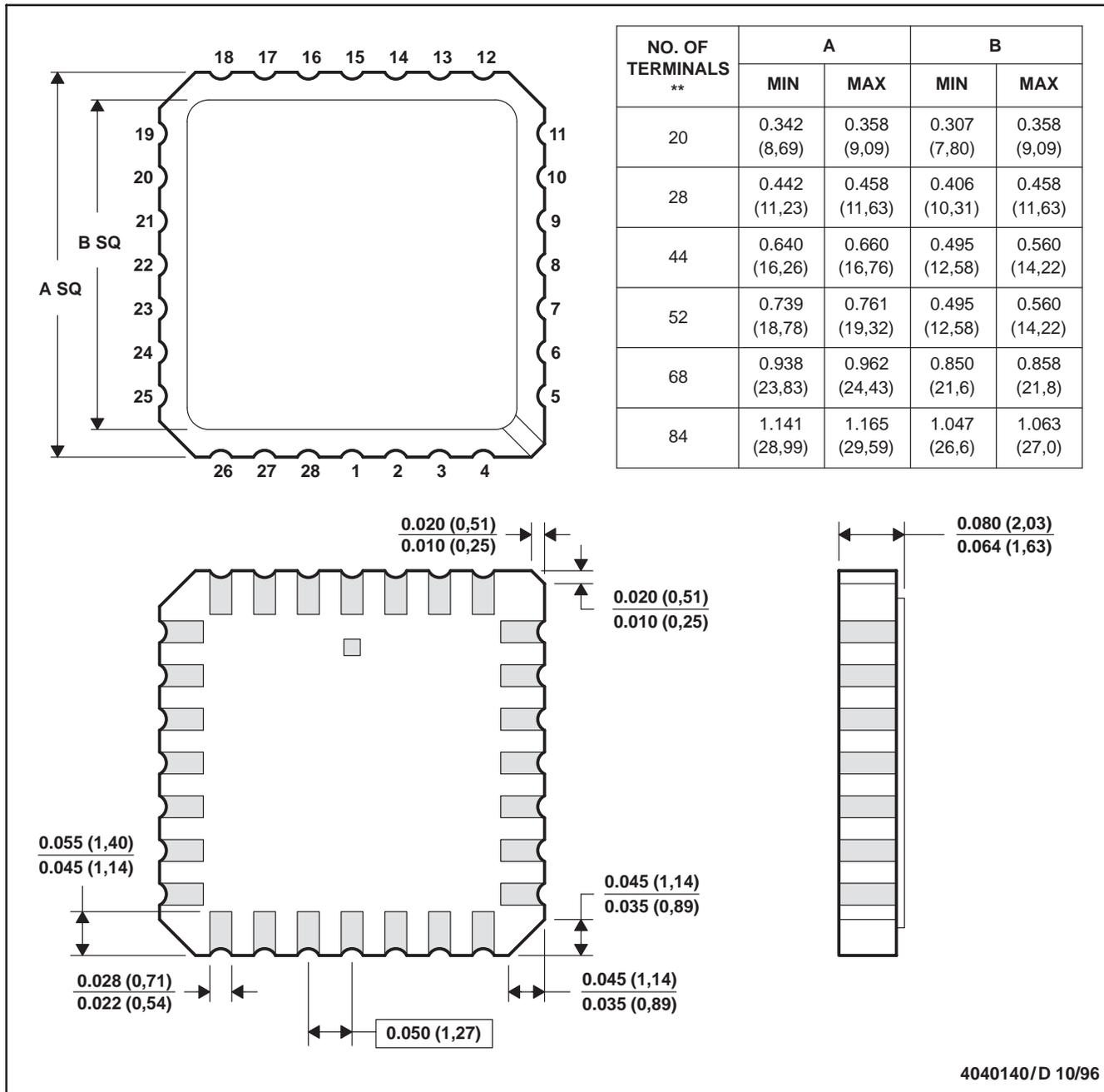0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES:　A.　All linear dimensions are in inches (millimeters).
　　　　　B.　This drawing is subject to change without notice.
　　　　　C.　This package is hermetically sealed with a ceramic lid using glass frit.
　　　　　D.　Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
　　　　　E.　Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)   **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

0.020 (0,51) / 0.010 (0,25)

0.020 (0,51) / 0.010 (0,25)

0.080 (2,03) / 0.064 (1,63)

0.055 (1,40) / 0.045 (1,14)

0.045 (1,14) / 0.035 (0,89)

0.028 (0,71) / 0.022 (0,54)

0.045 (1,14) / 0.035 (0,89)

0.050 (1,27)

4040140 / D 10/96
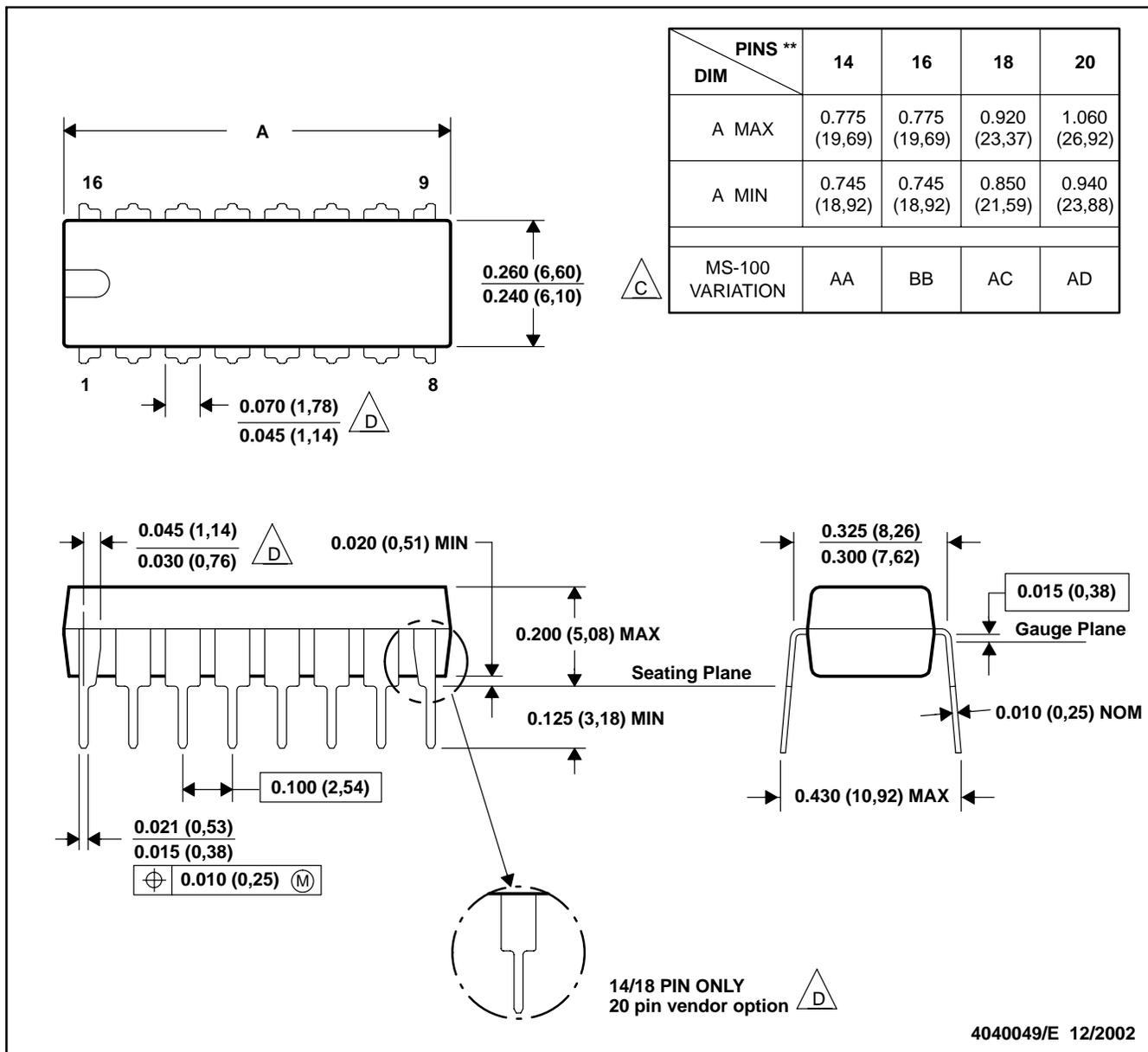
NOTES: A. All linear dimensions are in inches (millimeters).
     B. This drawing is subject to change without notice.
     C. This package can be hermetically sealed with a metal lid.
     D. The terminals are gold plated.
     E. Falls within JEDEC MS-004

TEXAS INSTRUMENTS

MECHANICAL

N (R-PDIP-T**)   **PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN

PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-100 VARIATION /C\	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) /D\

0.045 (1,14) / 0.030 (0,76) /D\

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 PIN ONLY 20 pin vendor option /D\
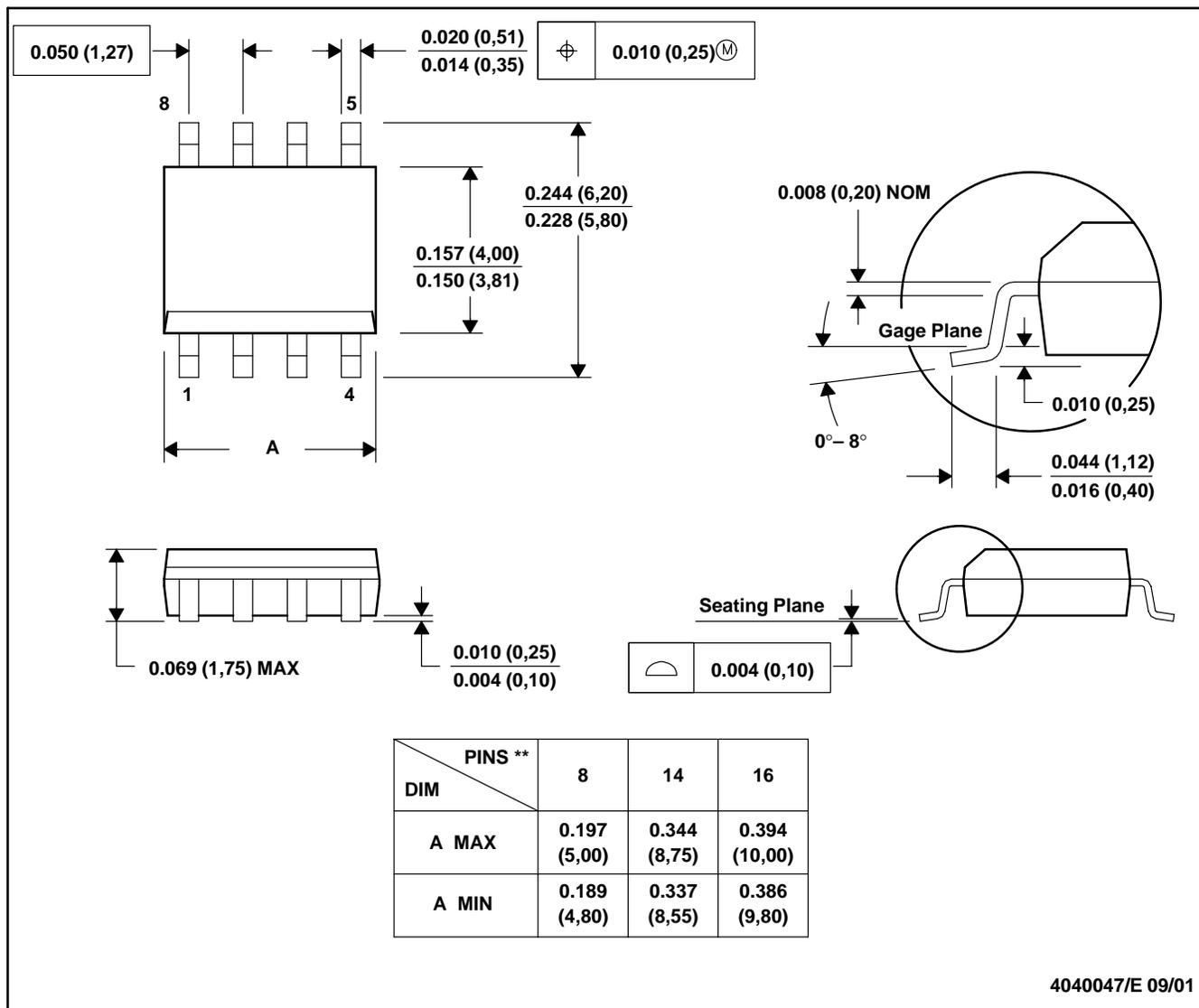
4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
/C\ Falls within JEDEC MS-001, except 18 and 20 pin minimum body lrngth (Dim A).
/D\ The 20 pin end lead shoulder width is a vendor option, either half or full width.

TEXAS
INSTRUMENTS

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D (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

8 PINS SHOWN

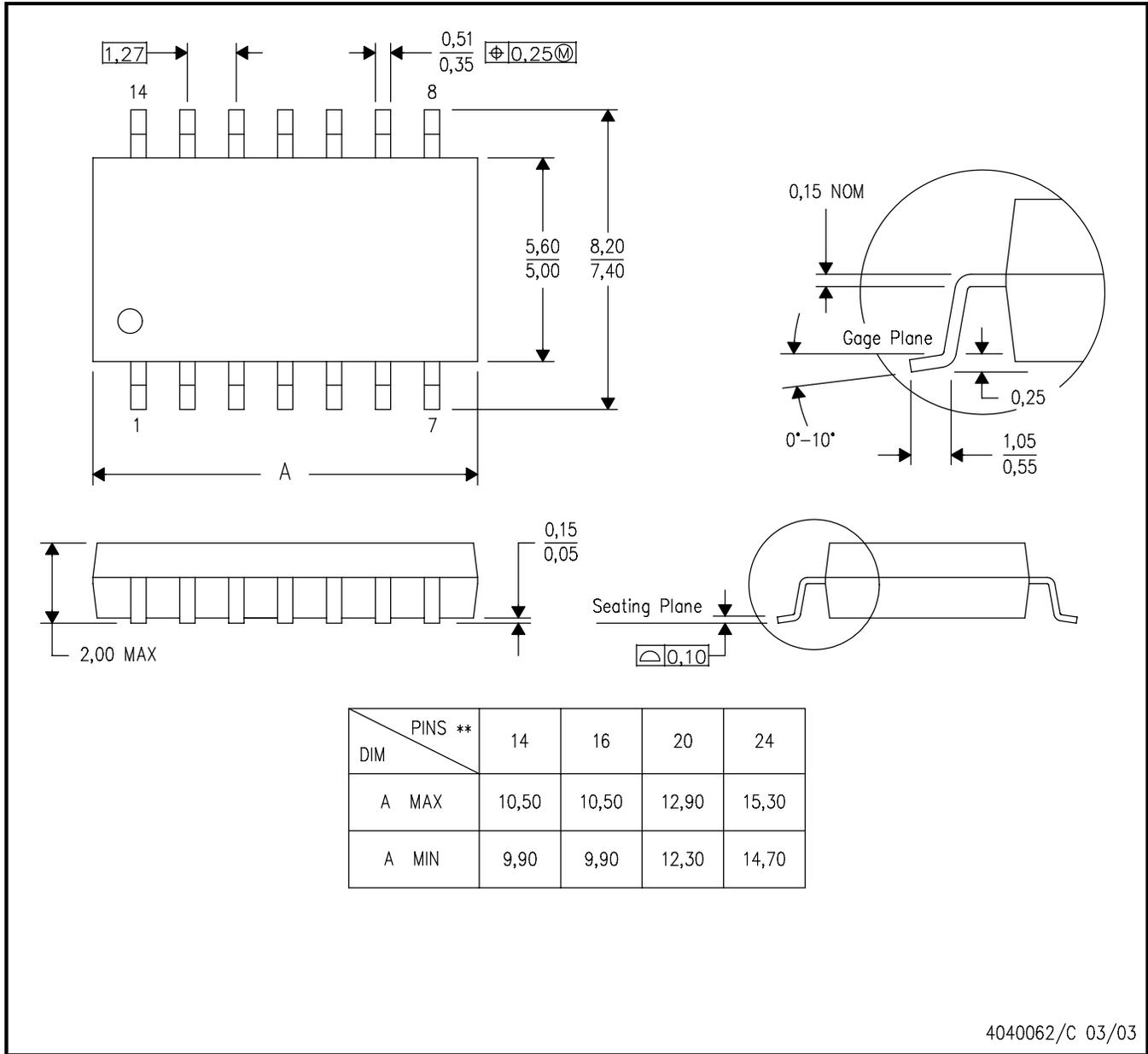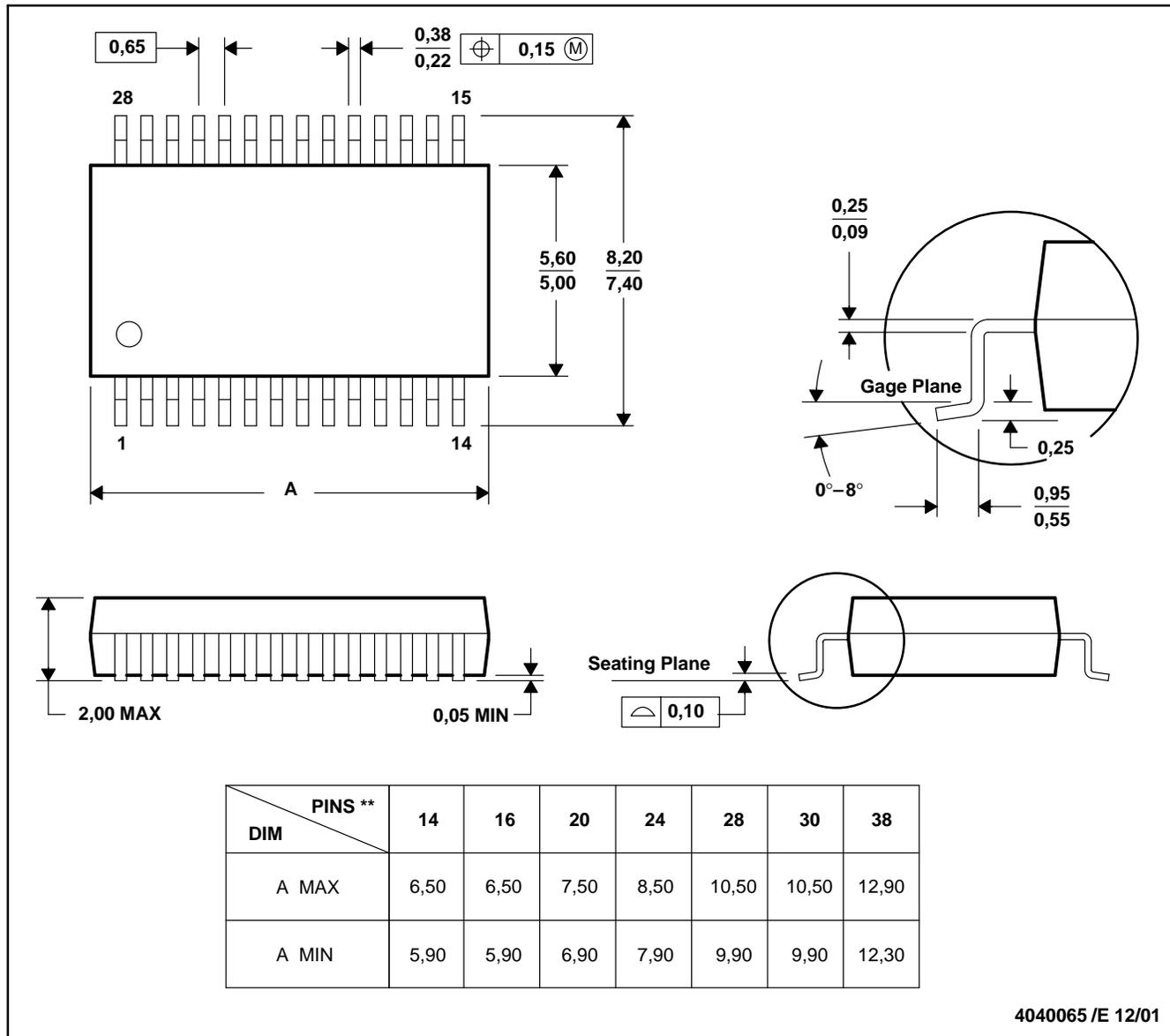| DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
        D. Falls within JEDEC MS-012

TEXAS INSTRUMENTS

MECHANICAL DATA

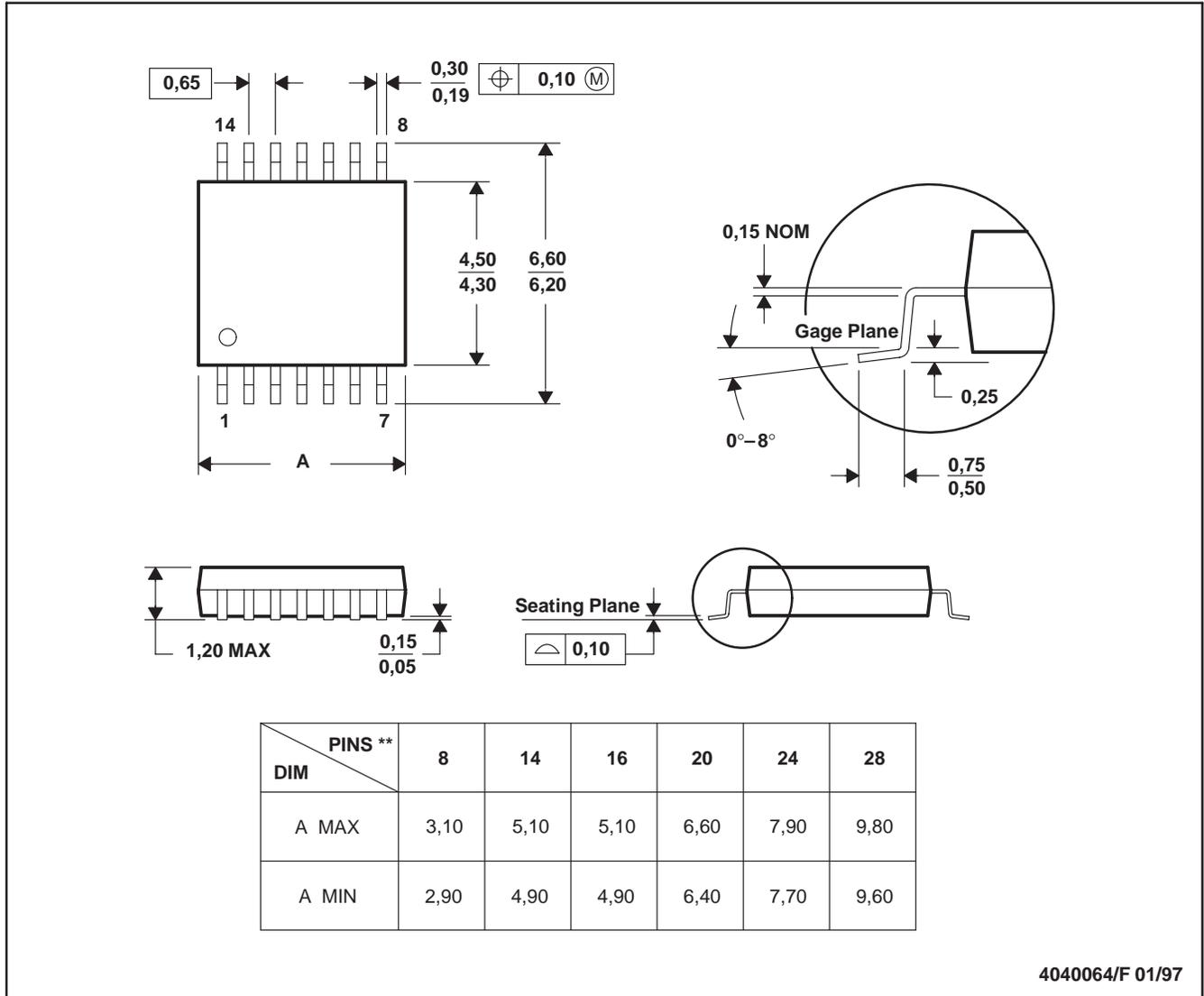| PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**) PLASTIC SMALL-OUTLINE

28 PINS SHOWN

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
    B. This drawing is subject to change without notice.
    C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
    D. Falls within JEDEC MO-153

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