DATA SHEET

74LVC1G80
Single D-type flip-flop; positive-edge trigger

Product specification
Supersedes data of 2004 Jun 29

2004 Sep 10

Philips
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Single D-type flip-flop; positive-edge trigger 74LVC1G80

FEATURES

- Wide supply voltage range from 1.65 V to 5.5 V
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V).
- ±24 mA output drive (V_{CC} = 3.0 V)
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

DESCRIPTION

The 74LVC1G80 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{off}. The I_{off} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC1G80 provides a single positive-edge triggered D-type flip-flop.

Information on the data input is transferred to the $\overline{Q}$ output pin on the LOW-to-HIGH transition of the clock pulse. The input pin D must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{Q}$	V_{CC} = 1.8 V; C_L = 30 pF; R_L = 1 kΩ	3.4	ns
		V_{CC} = 2.5 V; C_L = 30 pF; R_L = 500 Ω	2.3	ns
		V_{CC} = 2.7 V; C_L = 50 pF; R_L = 500 Ω	2.5	ns
		V_{CC} = 3.3 V; C_L = 50 pF; R_L = 500 Ω	2.4	ns
		V_{CC} = 5.0 V; C_L = 50 pF; R_L = 500 Ω	1.8	ns
f_{max}	maximum frequency	V_{CC} = 3.3 V; C_L = 50 pF; R_L = 500 Ω	350	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per buffer	V_{CC} = 3.3 V; notes 1 and 2	17	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUT		OUTPUT
CP	D	$\overline{Q}$
↑	L	H
↑	H	L
L	X	$\overline{q}$

Note

1. H = HIGH voltage level;
   L = LOW voltage level;
   ↑ = LOW-to-HIGH CP transition;
   X = don't care;
   $\overline{q}$ = lower case letter indicates the state of referenced input, one set-up time prior to the LOW-to-HIGH CP transition.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74LVC1G80GW	–40 °C to +125 °C	5	SC-88A	plastic	SOT353-1	VT
74LVC1G80GV	–40 °C to +125 °C	5	SC-74A	plastic	SOT753	V80
74LVC1G80GM	–40 °C to +125 °C	6	XSON6	plastic	SOT886	VT

PINNING

PIN TSSOP5; SC-74A	PIN XSON6	SYMBOL	DESCRIPTION
1	1	D	input D
2	2	CP	clock pulse input CP
3	3	GND	ground (0 V)
4	4	$\overline{Q}$	output $\overline{Q}$
-	5	n.c.	not connected
5	6	V_{CC}	supply voltage

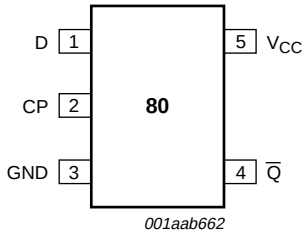
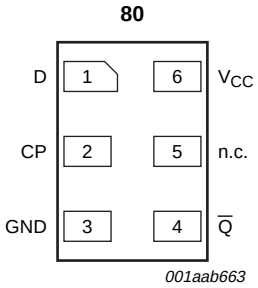


Fig.1 Pin configuration TSSOP5 and SC-74A.



Transparent top view

Fig.2 Pin configuration XSON6.

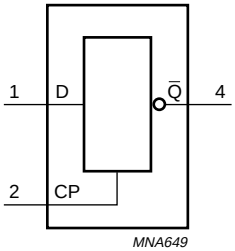


Fig.3 Logic symbol.

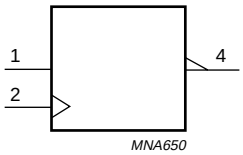


Fig.4 IEE/IEC logic symbol.

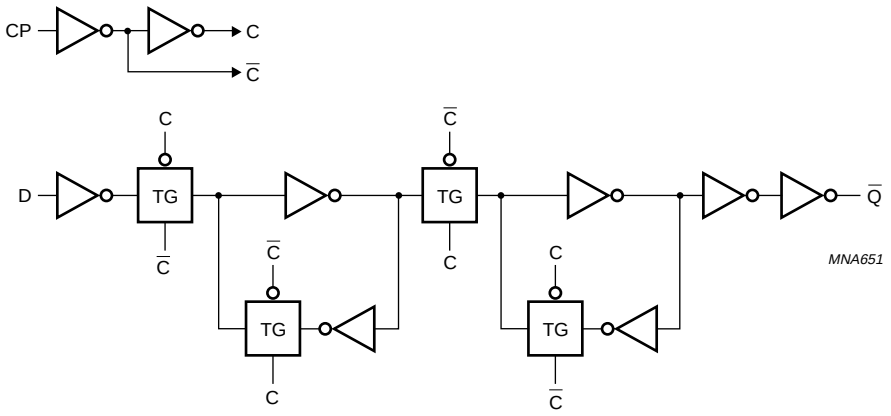


Fig.5 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	active mode	0	V_{CC}	V
		V_{CC} = 0 V; Power-down mode	0	5.5	V
T_{amb}	operating ambient temperature		–40	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.65 V to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input diode current	V_I < 0 V	–	–50	mA
V_I	input voltage	note 1	–0.5	+6.5	V
I_{OK}	output diode current	V_O > V_{CC} or V_O < 0 V	–	±50	mA
V_O	output voltage	active mode; note 1	–0.5	V_{CC} + 0.5	V
		Power-down mode; note 1	–0.5	+6.5	V
I_O	output source or sink current	V_O = 0 V to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C	–	250	mW

Note

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 °C to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		1.65 to 1.95	$0.65 \times V_{CC}$	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	$0.7 \times V_{CC}$	–	–	V
V_{IL}	LOW-level input voltage		1.65 to 1.95	–	–	$0.35 \times V_{CC}$	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	$0.3 \times V_{CC}$	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 100 μA	1.65 to 5.5	–	–	0.1	V
		I_O = 4 mA	1.65	–	–	0.45	V
		I_O = 8 mA	2.3	–	–	0.3	V
		I_O = 12 mA	2.7	–	–	0.4	V
		I_O = 24 mA	3.0	–	–	0.55	V
		I_O = 32 mA	4.5	–	–	0.55	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = −100 μA	1.65 to 5.5	V_{CC} − 0.1	–	–	V
		I_O = −4 mA	1.65	1.2	–	–	V
		I_O = −8 mA	2.3	1.9	–	–	V
		I_O = −12 mA	2.7	2.2	–	–	V
		I_O = −24 mA	3.0	2.3	–	–	V
		I_O = −32 mA	4.5	3.8	–	–	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	5.5	–	±0.1	±5	μA
I_{off}	power OFF leakage current	V_I or V_O = 5.5 V	0	–	±0.1	±10	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A	5.5	–	0.1	10	μA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC}$ − 0.6 V; I_O = 0 A	2.3 to 5.5	–	5	500	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 °C to +125 °C							
V_{IH}	HIGH-level input voltage		1.65 to 1.95	$0.65 \times V_{CC}$	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	$0.7 \times V_{CC}$	–	–	V
V_{IL}	LOW-level input voltage		1.65 to 1.95	–	–	$0.35 \times V_{CC}$	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	$0.3 \times V_{CC}$	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 100 μA	1.65 to 5.5	–	–	0.1	V
		I_O = 4 mA	1.65	–	–	0.7	V
		I_O = 8 mA	2.3	–	–	0.45	V
		I_O = 12 mA	2.7	–	–	0.60	V
		I_O = 24 mA	3.0	–	–	0.80	V
		I_O = 32 mA	4.5	–	–	0.80	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = −100 μA	1.65 to 5.5	$V_{CC} - 0.1$	–	–	V
		I_O = −4 mA	1.65	0.95	–	–	V
		I_O = −8 mA	2.3	1.7	–	–	V
		I_O = −12 mA	2.7	1.9	–	–	V
		I_O = −24 mA	3.0	2.0	–	–	V
		I_O = −32 mA	4.5	3.4	–	–	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	5.5	–	–	±100	μA
I_{off}	power OFF leakage current	V_I or V_O = 5.5 V	0	–	–	±200	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A	5.5	–	–	200	μA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC}$ − 0.6 V; I_O = 0 A	2.3 to 5.5	–	–	5000	μA

Note

1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

AC CHARACTERISTICS

GND = 0 V.

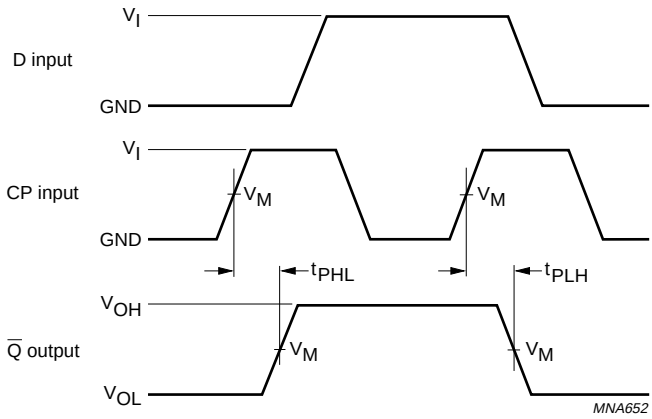
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 °C to +85 °C; note 1							
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{Q}$	see Figs 6 and 8	1.65 to 1.95	1.0	3.4	9.9	ns
			2.3 to 2.7	0.5	2.3	7.0	ns
			2.7	0.5	2.5	6.0	ns
			3.0 to 3.6	0.9	2.4	5.0	ns
			4.5 to 5.5	0.5	1.8	4.5	ns
t_{su}	set-up time D to CP	see Figs 7 and 8	1.65 to 1.95	2.3	0.8	–	ns
			2.3 to 2.7	1.5	0.6	–	ns
			2.7	1.5	0.5	–	ns
			3.0 to 3.6	1.3	0.4	–	ns
			4.5 to 5.5	1.1	0.5	–	ns
t_h	hold time D to CP	see Figs 7 and 8	1.65 to 1.95	0	−0.6	–	ns
			2.3 to 2.7	0	−0.4	–	ns
			2.7	+0.5	−0.2	–	ns
			3.0 to 3.6	0.9	0.2	–	ns
			4.5 to 5.5	+0.5	−0.1	–	ns
t_W	clock pulse with HIGH or LOW	see Figs 7 and 8	1.65 to 1.95	3.0	1.1	–	ns
			2.3 to 2.7	2.5	0.7	–	ns
			2.7	2.5	0.6	–	ns
			3.0 to 3.6	2.5	0.6	–	ns
			4.5 to 5.5	2.0	0.5	–	ns
f_{max}	maximum clock pulse frequency	see Figs 7 and 8	1.65 to 1.95	160	300	–	MHz
			2.3 to 2.7	160	350	–	MHz
			2.7	160	350	–	MHz
			3.0 to 3.6	160	350	–	MHz
			4.5 to 5.5	200	400	–	MHz

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 °C to +125 °C							
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{Q}$	see Figs 6 and 8	1.65 to 1.95	1.0	–	13.0	ns
			2.3 to 2.7	0.5	–	9.0	ns
			2.7	0.5	–	8.0	ns
			3.0 to 3.6	0.9	–	6.5	ns
			4.5 to 5.5	0.5	–	6.0	ns
t_{su}	set-up time D to CP	see Figs 7 and 8	1.65 to 1.95	2.3	–	–	ns
			2.3 to 2.7	1.5	–	–	ns
			2.7	1.5	–	–	ns
			3.0 to 3.6	1.3	–	–	ns
			4.5 to 5.5	1.1	–	–	ns
t_h	hold time D to CP	see Figs 7 and 8	1.65 to 1.95	0	–	–	ns
			2.3 to 2.7	0	–	–	ns
			2.7	0.5	–	–	ns
			3.0 to 3.6	0.9	–	–	ns
			4.5 to 5.5	0.5	–	–	ns
t_W	clock pulse with HIGH or LOW	see Figs 7 and 8	1.65 to 1.95	3.0	–	–	ns
			2.3 to 2.7	2.5	–	–	ns
			2.7	2.5	–	–	ns
			3.0 to 3.6	2.5	–	–	ns
			4.5 to 5.5	2.0	–	–	ns
f_{max}	maximum clock pulse frequency	see Figs 7 and 8	1.65 to 1.95	160	–	–	MHz
			2.3 to 2.7	160	–	–	MHz
			2.7	160	–	–	MHz
			3.0 to 3.6	160	–	–	MHz
			4.5 to 5.5	200	–	–	MHz

Note

1. All typical values are measured at T_{amb} = 25 °C.

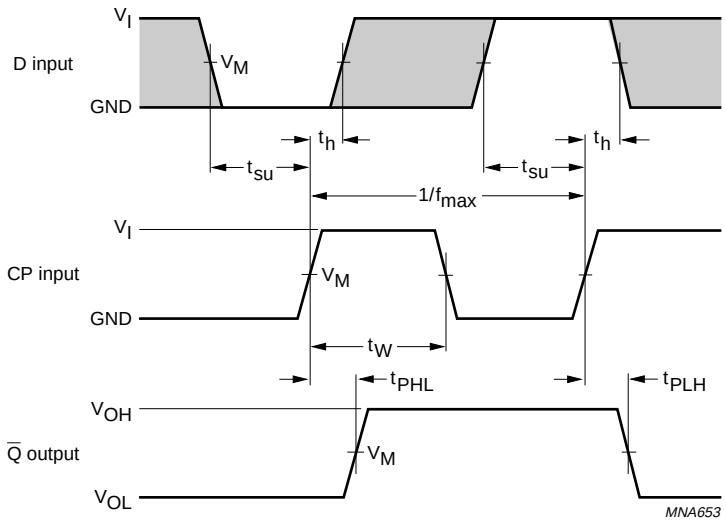
AC WAVEFORMS



V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 V to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 V to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 V to 5.5 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

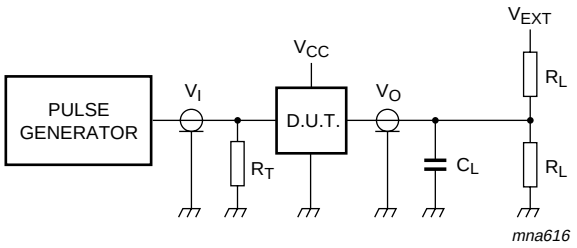
Fig.6 Clock (CP) to output ($\overline{Q}$) propagation delay times.



V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 V to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 V to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 V to 5.5 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns

The shaded areas indicate when the input is permitted to change for predictable output performance.
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.7 Clock (CP) to output ($\overline{Q}$) propagation delays, clock pulse width, D to CP set-up times, the D to CP hold times and maximum clock pulse frequency.



V_{CC}	V_I	C_L	R_L	V_{EXT}		
				t_{PLH}/t_{PHL}	t_{PZH}/t_{PHZ}	t_{PZL}/t_{PLZ}
1.65 V to 1.95 V	V_{CC}	30 pF	1 kΩ	open	GND	$2 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	30 pF	500 Ω	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

Definitions for test circuit:

R_L = Load resistor.

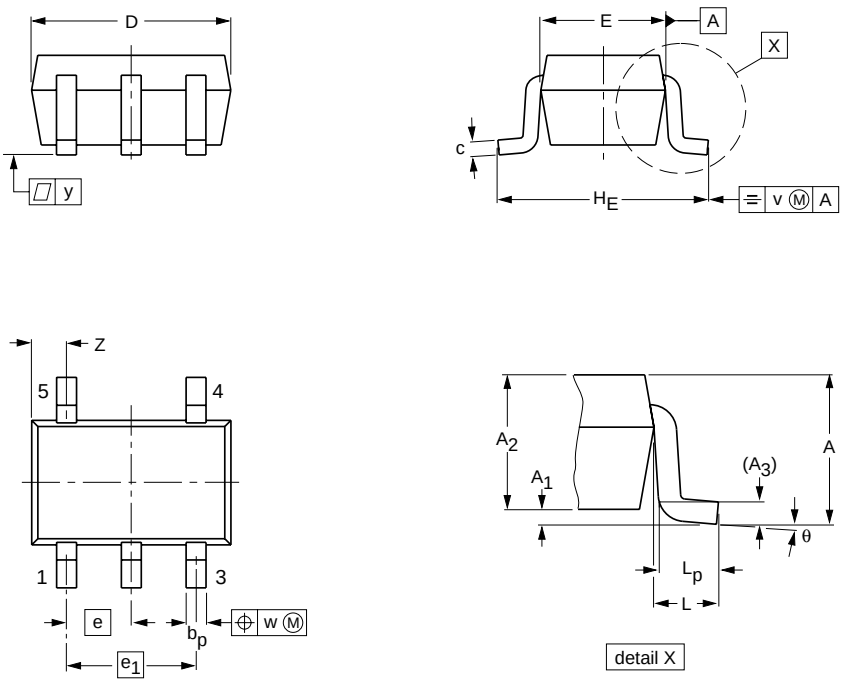
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.8 Load circuitry for switching times.

PACKAGE OUTLINES

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm **SOT353-1**



DIMENSIONS (mm are the original dimensions)

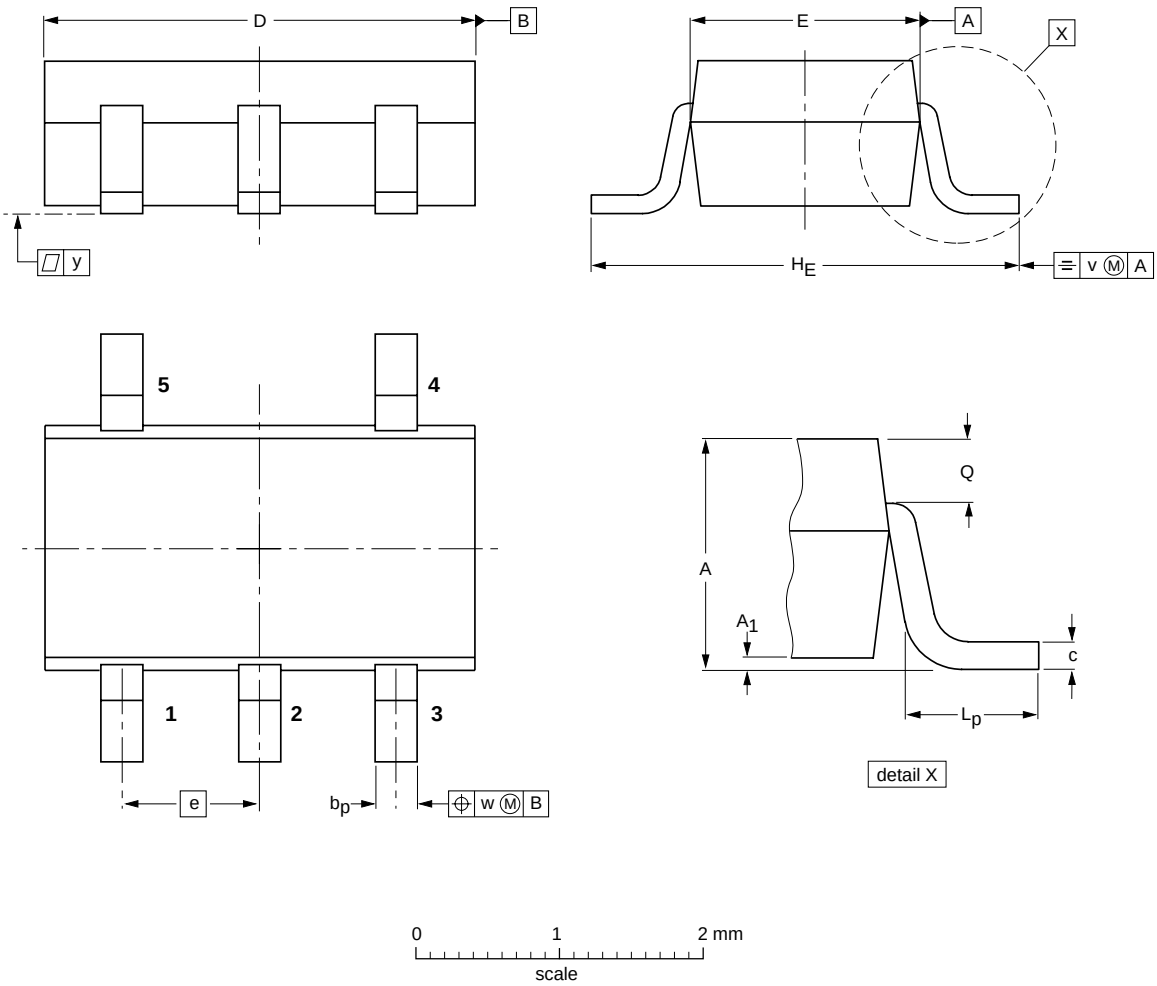
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	e_1	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.1 0	1.0 0.8	0.15	0.30 0.15	0.25 0.08	2.25 1.85	1.35 1.15	0.65	1.3	2.25 2.0	0.425	0.46 0.21	0.3	0.1	0.1	0.60 0.15	7° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT353-1		MO-203	SC-88A			~~00-09-01~~ 03-02-19

Plastic surface mounted package; 5 leads **SOT753**

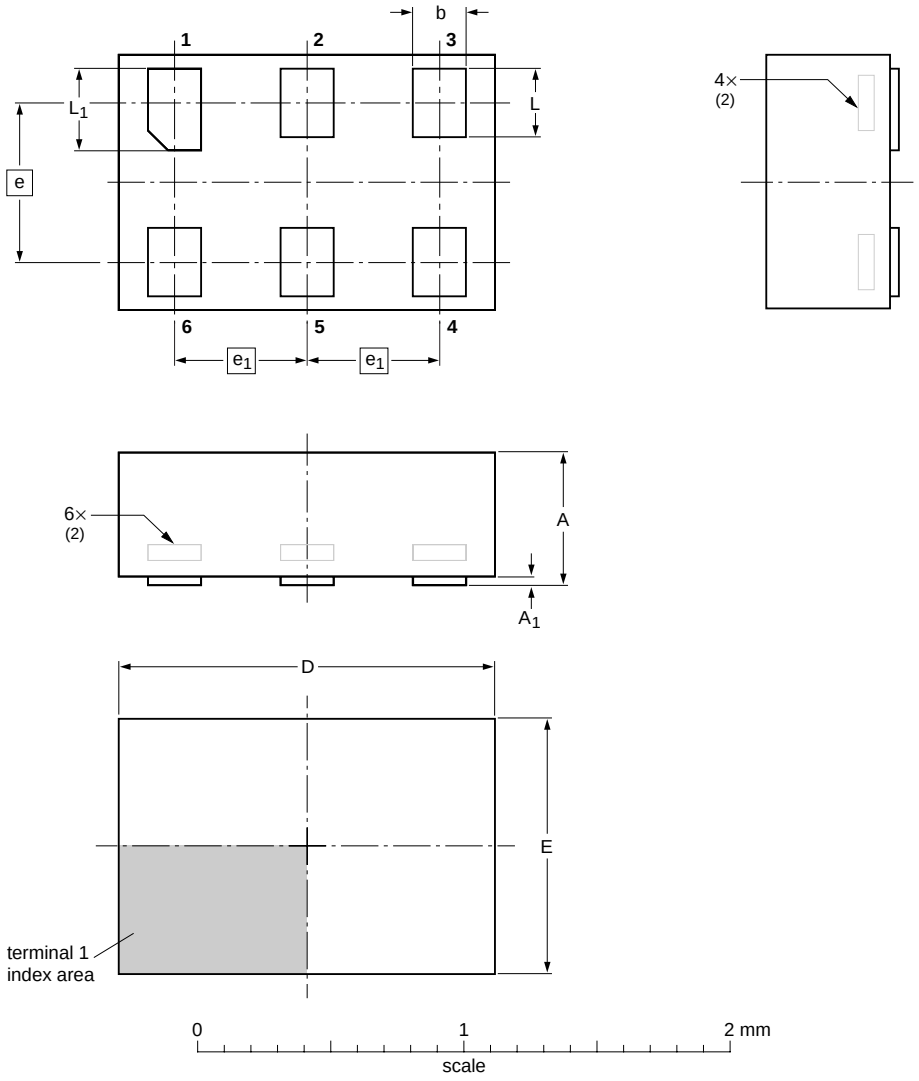


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			02-04-16

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm **SOT886**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A1 max	b	D	E	e	e1	L	L1
mm	0.5	0.04	0.25 0.17	1.5 1.4	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-15~~ 04-07-22

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

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