DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4894B
12-stage shift-and-store register LED driver

Product specification
File under Integrated Circuits, IC04

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Philips Semiconductors

PHILIPS

12-stage shift-and-store register LED driver HEF4894B

APPLICATIONS

- Automotive
- Industrial

GENERAL DESCRIPTION

The HEF4894B is a 12 stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel LED driver outputs O_0 to O_{11}. Data is shifted on positive-going clock transitions. The data in each shift register stage is transferred to the storage register when the strobe (STR) input is HIGH. Data in the storage register appears at the outputs whenever the output enable (EO) signal is HIGH.

Two serial outputs (O_S and O_S') are available for cascading a number of HEF4894B devices. Data is available at O_S on positive-going clock edges to allow high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information is available at O_S' on the next negative-going clock edge and provides cascading HEF4894B devices when the clock rise time is slow.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PIN POSITION	MATERIAL	CODE
HEF4894BT	20	SO	plastic	SO20/SOT163A
HEF4894BP	20	DIL	plastic	DIL20/SOT146

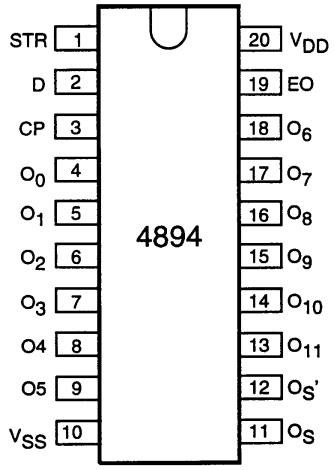
PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	STR	strobe input
2	D	data input
3	CP	clock input
4, 5, 6, 7, 8, 9, 18, 17, 16, 15, 14, 13	O_0 to O_{11}	parallel outputs (open drain)
10	V_{SS}	ground
11, 12	O_S, O_S'	serial outputs
19	EO	output enable input
20	V_{DD}	positive supply voltage

FAMILY DATA

See Family Specifications except for:
Rating for DC current into any open-drain output: 40 mA.

I_{DD} LIMITS category MSI: see Family Specifications.



Preliminary pin assignment.

Fig.1 Pinning diagram.

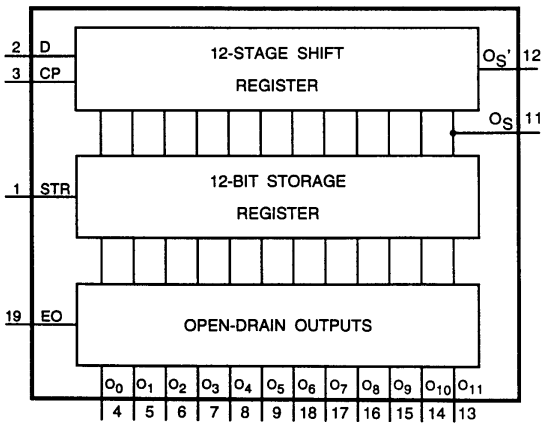


Fig.2 Functional diagram.

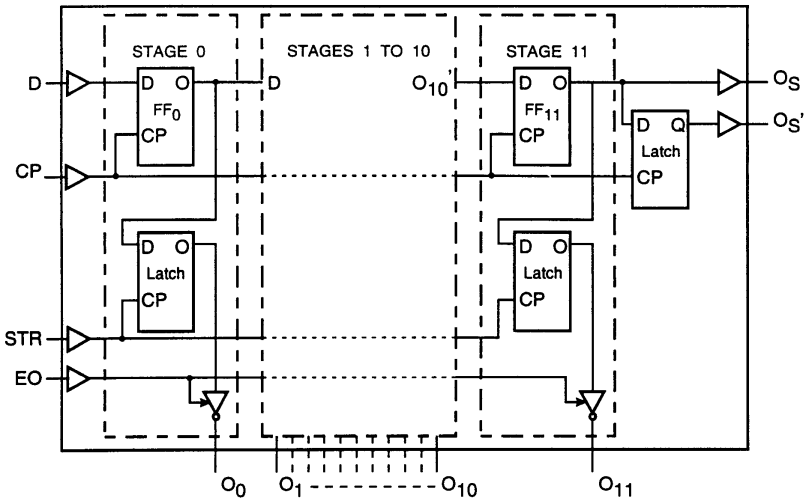


Fig.3 Logic diagram.

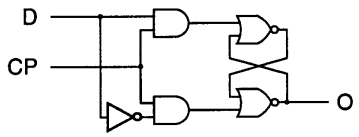


Fig.4 One D-latch.

FUNCTION TABLE

INPUTS				PARALLEL OUTPUTS		SERIAL OUTPUTS	
CP	**EO**	**STR**	**D**	O_0	O_n	O_S	O_S'
↑	L	X	X	Z	Z	O_{10}'	nc
↓	L	X	X	Z	Z	nc	O_{11}
↑	H	L	X	nc	nc	O_{10}'	nc
↑	H	H	L	Z	$O_n - 1$	O_{10}'	nc
↑	H	H	H	L	$O_n - 1$	O_{10}'	nc
↓	H	H	H	nc	nc	nc	O_{11}

Notes

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial
4. ↑ = positive-going transition
5. ↓ = negative-going transition
6. Z = high impedance OFF state
7. nc = no change
8. O_{11}' = the information in the twelfth shift register stage.

At the positive clock edge the information in the 10th register stage is transferred to the 11th register stage and the O_s output.

DC CHARACTERISTICS

V_{SS} = 0 V.

PARAMETER	V_{DD} (V)	SYMBOL	T_{amb} (°C)						UNIT	CONDITIONS
			−40		+ 25		+ 85			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
output voltage LOW; O_n	5	V_{OL}	–	0.75	–	0.75	–	1.5	V	$V_I = V_{SS}$ or V_{DD}; $\lvert I_o \rvert$ < 20 mA
	10		–	0.75	–	0.75	–	1.5		
	15		–	0.75	–	0.75	–	1.5		
output leakage current; HIGH; O_n	5	I_{OZH}	–	2	–	2	–	15	μA	V_o = 15 V
	10		–	2	–	2	–	15		
	15		–	2	–	2	–	15		

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns.

PARAMETER	V_{DD} (V)	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$1200\ f_i + \sum(f_o C_L) \times V_{DD}^2$	where:
	10	$5550\ f_i + \sum(f_o C_L) \times V_{DD}^2$	$R_{load} = \infty$
	15	$15000\ f_i + \sum(f_o C_L) \times V_{DD}^2$	f_i = input frequency (MHz),
			f_o = output frequency (MHz),
			C_L = load capacitance (pF),
			$\sum(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns.

PARAMETER	V_{DD} (V)	SYMBOL	TYP.	MAX.	UNIT	TYPICAL EXTRAPOLATION FORMULA
Propagation delay CP to O_s HIGH to LOW	5	t_{PHL}	160	320	ns	132 ns + (0.55 ns/pF) C_L
	10		65	130		53 ns + (0.23 ns/pF) C_L
	15		45	90		37 ns + (0.16 ns/pF) C_L
Propagation delay CP to O_s LOW to HIGH	5	t_{PLH}	130	260	ns	102 ns + (0.55 ns/pF) C_L
	10		55	110		44 ns + (0.23 ns/pF) C_L
	15		40	80		32 ns + (0.16 ns/pF) C_L
Propagation delay CP to O_s' HIGH to LOW	5	t_{PHL}	120	240	ns	92 ns + (0.55 ns/pF) C_L
	10		50	100		39 ns + (0.23 ns/pF) C_L
	15		40	80		32 ns + (0.16 ns/pF) C_L
Propagation delay CP to O_s' LOW to HIGH	5	t_{PLH}	130	260	ns	102 ns + (0.55 ns/pF) C_L
	10		60	120		49 ns + (0.23 ns/pF) C_L
	15		45	90		37 ns + (0.16 ns/pF) C_L

PARAMETER	V_{DD} (V)	SYMBOL	TYP.	MAX.	UNIT	TYPICAL EXTRAPOLATION FORMULA
Propagation delay	5		240	480		
CP to O_n	10	t_{PZL}	80	160	ns	see note 1
OFF to LOW	15		55	110		
Propagation delay	5		170	340		
CP to O_n	10	t_{PLZ}	75	150	ns	see note 1
LOW to OFF	15		60	120		
Propagation delay	5		140	280		
STR to O_n	10	t_{PZL}	70	140	ns	see note 1
OFF to LOW	15		55	110		
Propagation delay	5		100	200		
STR to O_n	10	t_{PLZ}	40	100	ns	see note 1
LOW to OFF	15		35	70		
Output transition	5		85	170		35 ns + (1.0 ns/pF) C_L
time; O_s, O_s'	10	t_{THL}	40	80	ns	19 ns + (0.42 ns/pF) C_L
HIGH to LOW	15		30	60		16 ns + (0.28 ns/pF) C_L
Output transition	5		85	170		35 ns + (1.0 ns/pF) C_L
time; O_s, O_s'	10	t_{TLH}	40	80	ns	19 ns + (0.42 ns/pF) C_L
LOW to HIGH	15		30	60		16 ns + (0.28 ns/pF) C_L

Note

1. Definition of symbol equivalent to 3-state outputs.

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns.

PARAMETER	V_{DD} (V)	SYMBOL	MIN.	TYP.	MAX.	UNIT
output enable time	5	t_{PZL}	–	100	200	ns
EO to O_n	10		–	55	110	
OFF to LOW	15		–	50	100	
output disable time	5	t_{PLZ}	–	80	160	ns
EO to O_n	10		–	40	80	
LOW to OFF	15		–	30	60	
minimum clock pulse width	5	t_{WCPL}	60	30	–	ns
LOW	10		30	15	–	
	15		24	12	–	
minimum strobe pulse width	5	t_{WSTRH}	80	40	–	ns
HIGH	10		60	30	–	
	15		24	12	–	

PARAMETER	V_{DD} (V)	SYMBOL	MIN.	TYP.	MAX.	UNIT
set-up time	5	t_{su}	60	30	–	ns
D to CP	10		20	10	–	
	15		15	5	–	
hold time	5	t_{hold}	5	–15	–	ns
D to CP	10		20	5	–	
	15		20	5	–	
Maximum clock pulse frequency	5	f_{max}	5	10	–	MHz
	10		11	22	–	
	15		14	28	–	

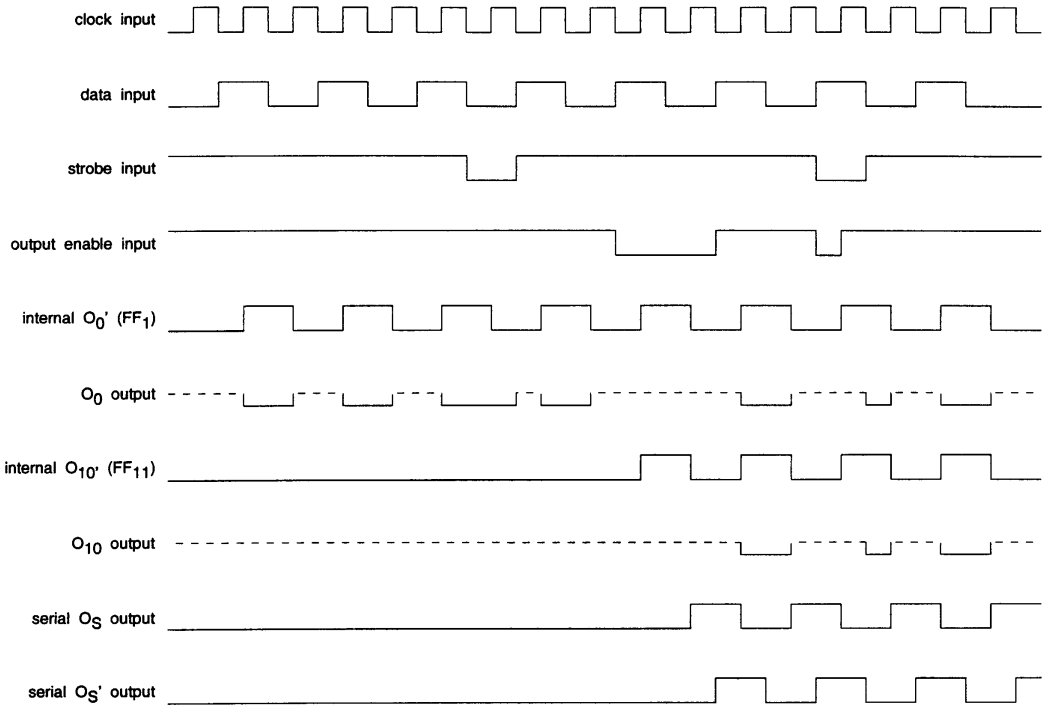


Fig.5 Timing diagram.

APPLICATION INFORMATION

An example of applications for the HEF4894B is:

- Serial-to-parallel converting LED driver

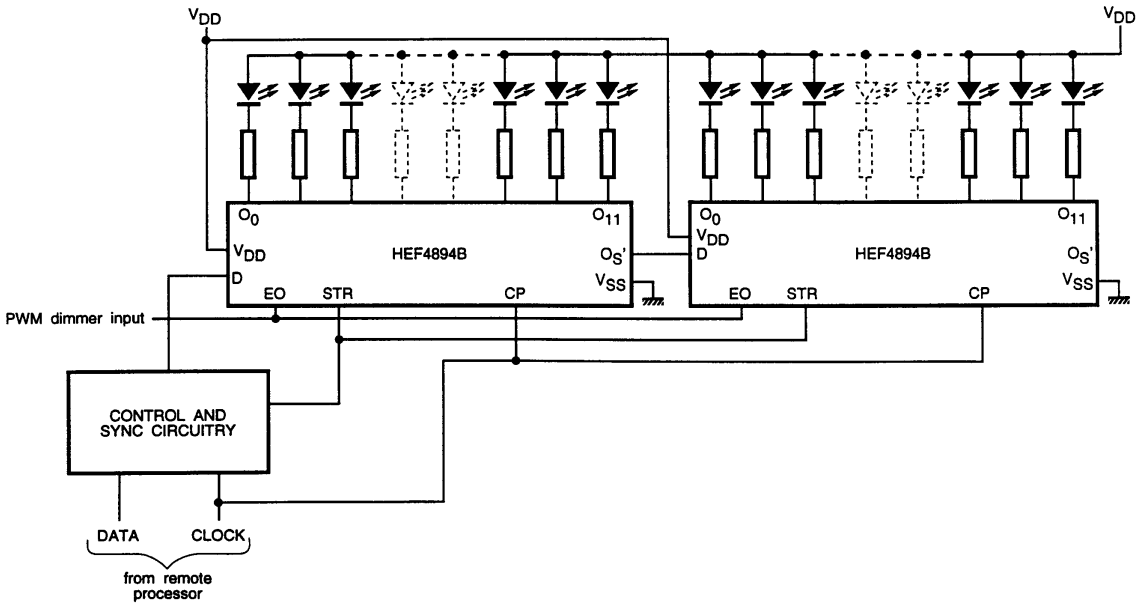


Fig.6 LED driver register.