EMIF10-LCD01F1

10 LINES EMI FILTER AND ESD PROTECTION

IPAD™

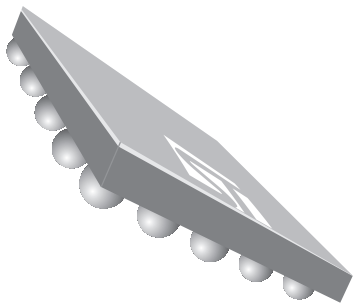
MAIN PRODUCT CHARACTERISTICS:

Where EMI filtering in ESD sensitive equipment is required :

- LCD for Mobile phones
- Computers and printers
- Communication systems
- MCU Boards

DESCRIPTION

The EMIF10-LCD01F1 is a 10 lines highly integrated devices designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF10 flip chip packaging means the package size is equal to the die size.
This filter includes an ESD protection circuitry, which prevents the device from destruction when subjected to ESD surges up 15kV.

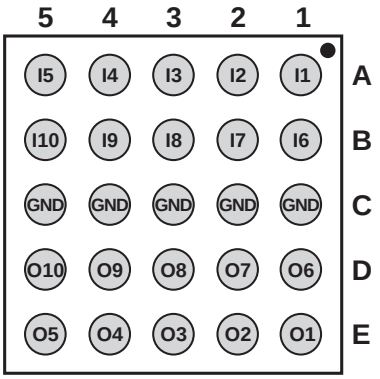


Flip Chip package

BENEFITS

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Very low PCB space consuming: 2.64mm x 2.64mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression on input pins (IEC6100-4-2 level 4)
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging.

PIN CONFIGURATION (ball side)



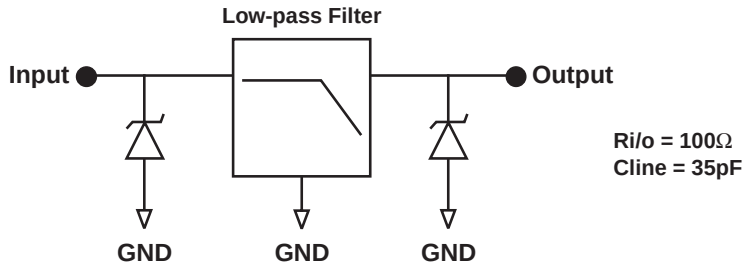
COMPLIES WITH THE FOLLOWING STANDARDS:

IEC61000-4-2

Level 4	input pins	15kV	(air discharge)
		8 kV	(contact discharge)
Level 1	output pins	2kV	(air discharge)
		2kV	(contact discharge)

MIL STD 883E - Method 3015-6 Class 3

BASIC CELL CONFIGURATION



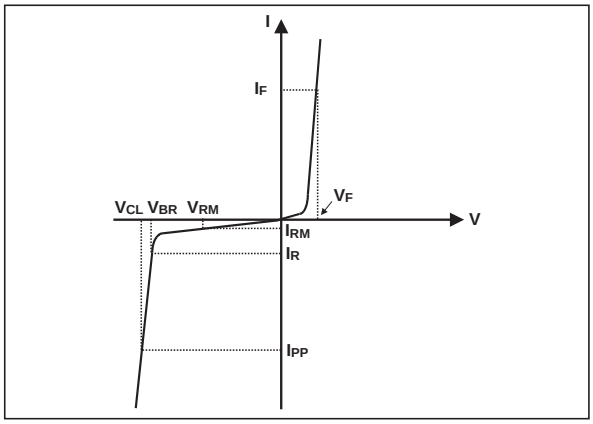
TM : IPAD is a trademark of STMicroelectronics.

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C)

Symbol	Parameter and test conditions	Value	Unit
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	-40 to + 85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameters
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min	Typ	Max	Unit
V_{BR}	I_R = 1mA	6	8	10	V
I_{RM}	V_{RM} = 3V			500	nA
$R_{I/O}$		90	100	110	Ω
C_{line}	At 0V bias			35	pF
Rt / Ft	Induced rise and fall time 10-90% at 26 MHz frequency signal V = 1.9 V (Rt / Ft input 1 ns, 50Ω impedance generator)		8 (1)		ns

(1) guaranteed by design

Fig. 1: S21(dB) all lines attenuation measurement and Aplac simulation.

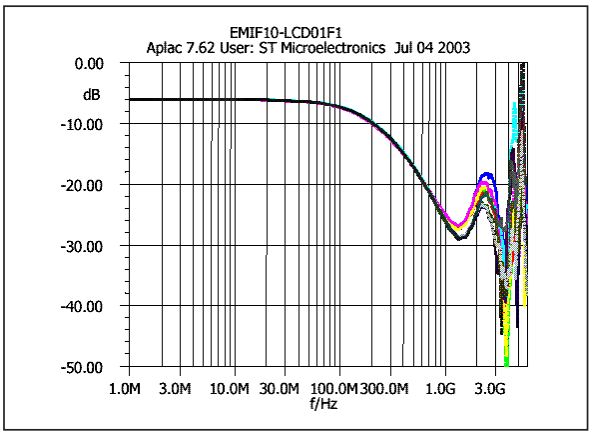


Fig. 2: Analog crosstalk measurements.

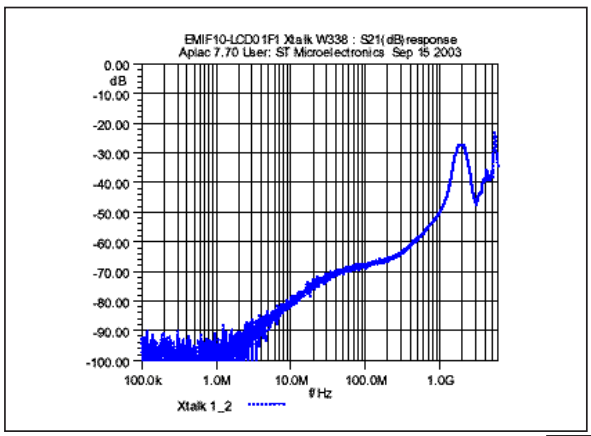


Fig. 3: ESD response to IEC61000-4-2 (+15kV air discharge) on one input and one output.

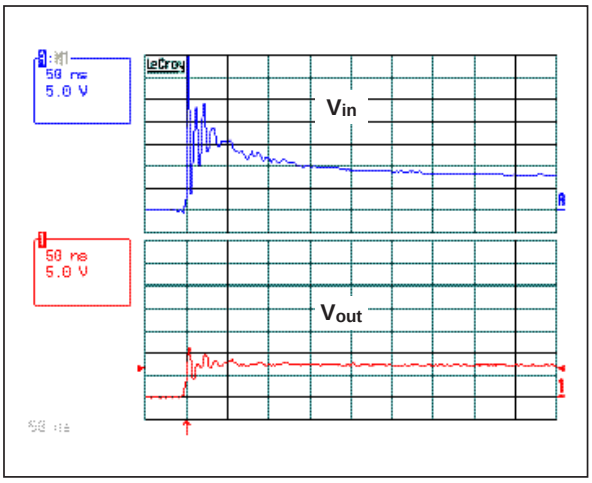


Fig. 4: ESD response to IEC61000-4-2 (-15kV air discharge) on one input and one output.

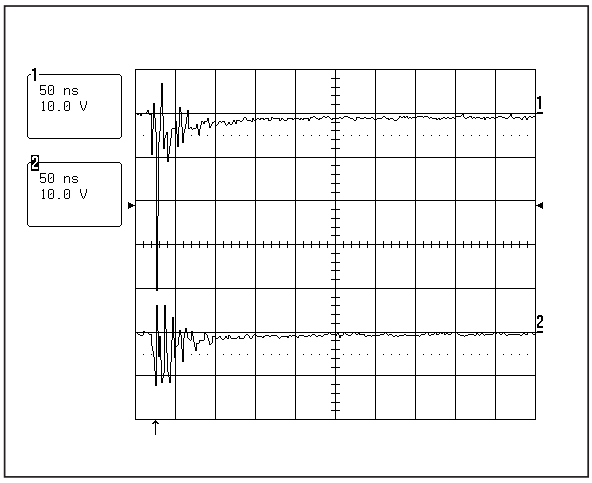


Fig. 5: Line capacitance versus applied voltage.

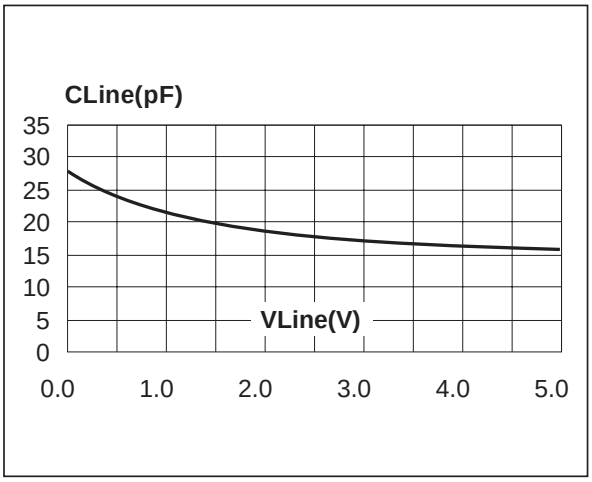


Fig. 6: Rise time 10-90% measurements with 1.9V signal at 26 MHz frequency (50Ω generator).

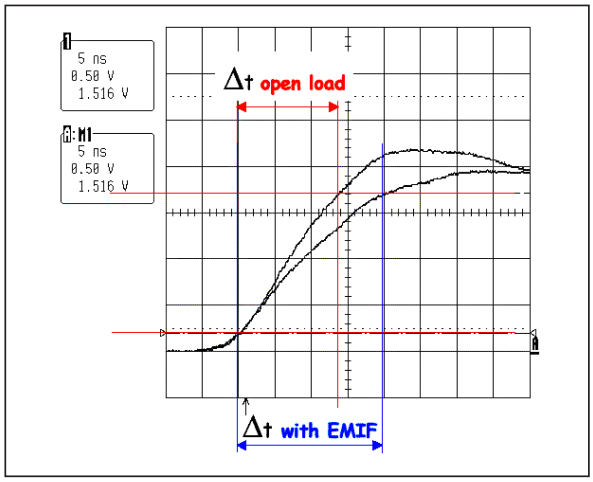
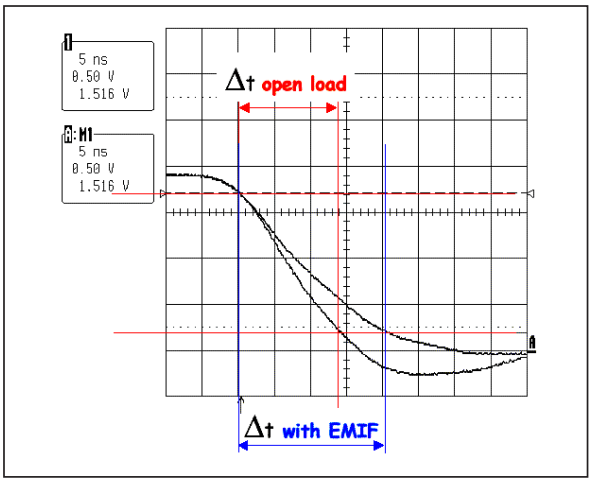
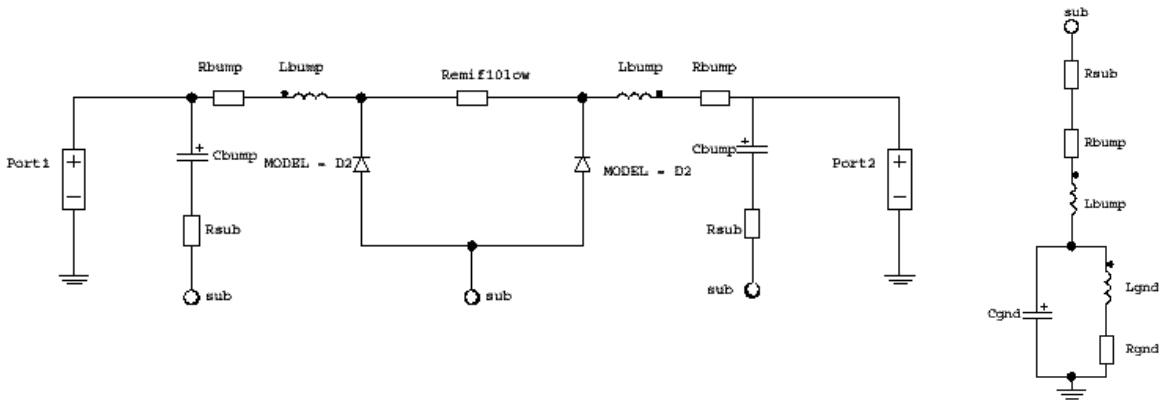


Fig. 7: Fall time 10-90% measurements with 1.9V signal at 26 MHz frequency (50Ω generator).



Aplac model.



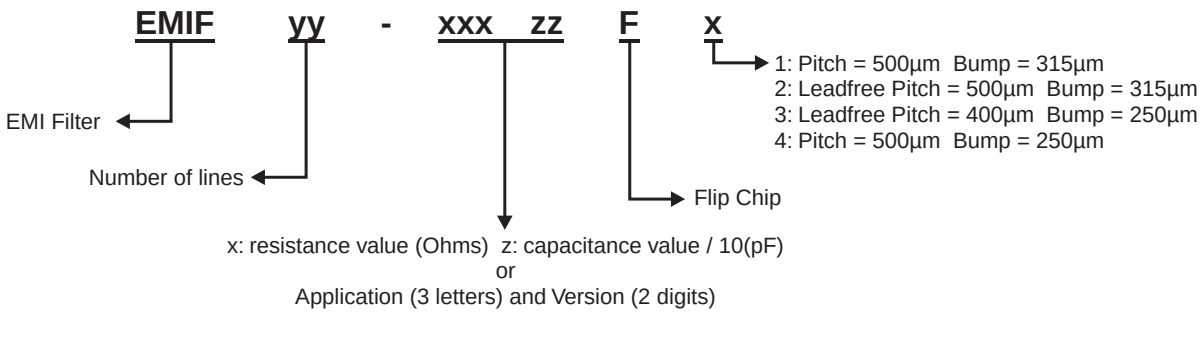
EMIF10-LCD01F1 model **Ground return**

Aplac parameters.

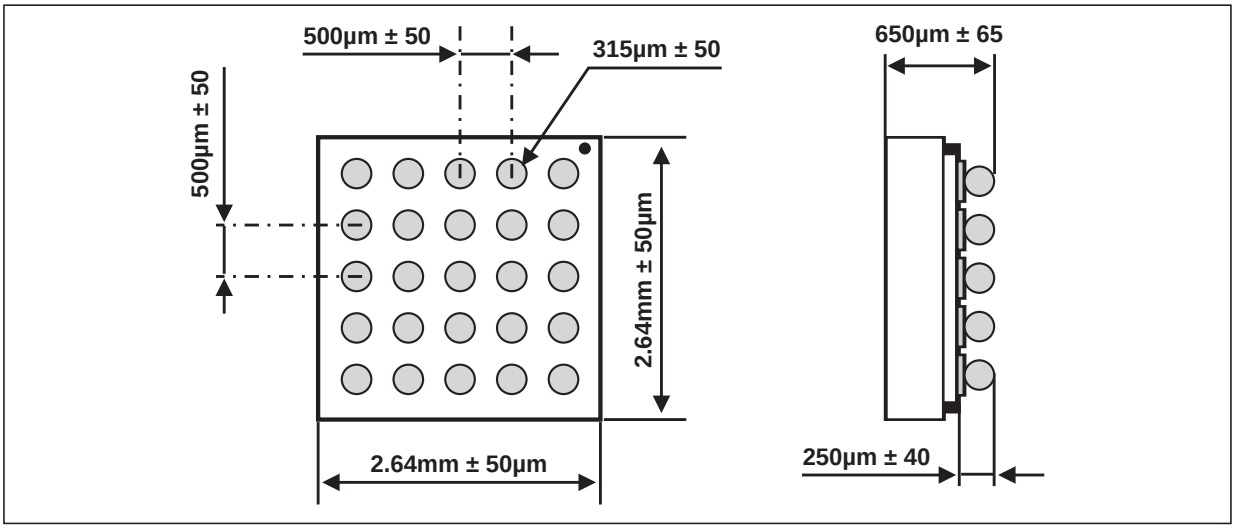
ZRZ structure
aplacvar Remif10low 100
aplacvar Cemif10flow 17.5pF
Bumps
aplacvar Lbump 50pH
aplacvar Rbump 20m
aplacvar Cbump 1.5pF
Bulk
aplacvar Rsub 100m
Gnd connections
aplacvar Rgnd 100m
aplacvar Lgnd 200pH
aplacvar Cgnd 0.15pF

BV = 7
CJO = Cemif10low
IBV = 1u
IKF = 1000
IS = 10f
ISR = 100p
N = 1
M = 0.3333
RS = 0.015
VJ = 0.6
TT = 50n

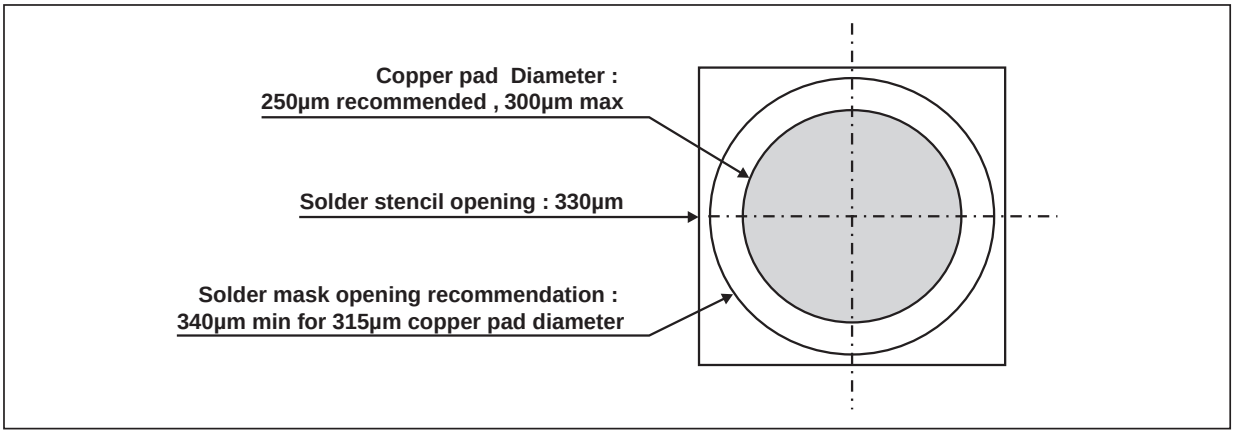
ORDER CODE



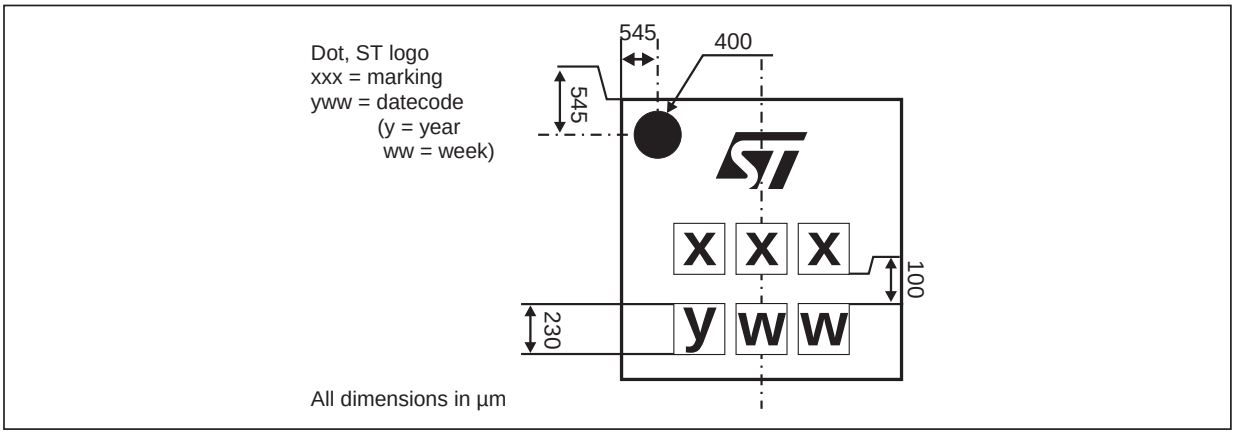
PACKAGE MECHANICAL DATA
FLIP CHIP



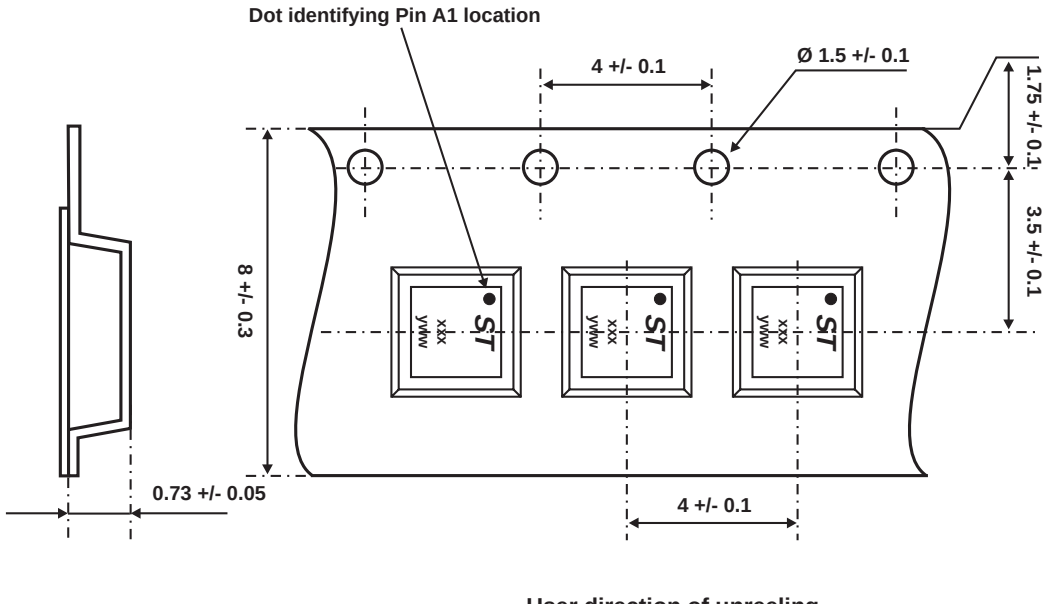
FOOT PRINT RECOMMENDATIONS



MARKING



PACKING



OTHER INFORMATION

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF10-LCD01F1	FLT	Flip Chip	9.3 mg	5000	Tape & reel (7”)

Note: More information are available in the application notes:
- AN1235: "Flip-Chip: Package description and recommandations for use"
- AN1751: "EMI Filters: Recommendations and measurements"