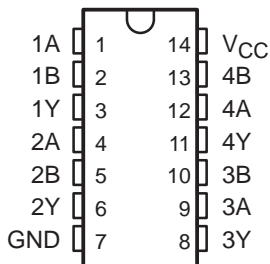


SN54AC08, SN74AC08 QUADRUPLE 2-INPUT POSITIVE-AND GATES

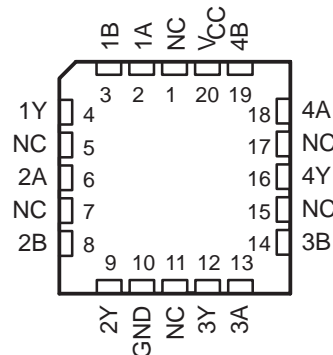
SCAS536D – SEPTEMBER 1995 – REVISED OCTOBER 2003

- 2-V to 6-V V_{CC} Operation
- Inputs Accept Voltages to 6 V
- Max t_{pd} of 7.5 ns at 5 V

SN54AC08 . . . J OR W PACKAGE
SN74AC08 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AC08 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'AC08 devices are quadruple 2-input positive-AND gates. These devices perform the Boolean function $Y = A \bullet B$ or $Y = \bar{A} + \bar{B}$ in positive logic.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|---------------|-----------------------|------------------|
| -40°C to 85°C | PDIP – N | Tube | SN74AC08N | SN74AC08N |
| | SOIC – D | Tube | SN74AC08D | AC08 |
| | | Tape and reel | SN74AC08DR | |
| | SOP – NS | Tape and reel | SN74AC08NSR | AC08 |
| | SSOP – DB | Tape and reel | SN74AC08DBR | AC08 |
| | TSSOP – PW | Tube | SN74AC08PW | AC08 |
| | | Tape and reel | SN74AC08PWR | |
| -55°C to 125°C | CDIP – J | Tube | SNJ54AC08J | SNJ54AC08J |
| | CFP – W | Tube | SNJ54AC08W | SNJ54AC08W |
| | LCCC – FK | Tube | SNJ54AC08FK | SNJ54AC08FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | H | H |
| L | X | L |
| X | L | L |



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54AC08, SN74AC08 QUADRUPLE 2-INPUT POSITIVE-AND GATES

SCAS536D – SEPTEMBER 1995 – REVISED OCTOBER 2003

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Output voltage range, V_O (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) | ±20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ±20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±50 mA |
| Continuous current through V_{CC} or GND | ±200 mA |
| Package thermal impedance, θ_{JA} (see Note 2): | |
| D package | 86°C/W |
| DB package | 96°C/W |
| N package | 80°C/W |
| NS package | 76°C/W |
| PW package | 113°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | | SN54AC08 | | SN74AC08 | | UNIT |
|---------------------|------------------------------------|------------------|----------|----------|----------|------|
| | | MIN | MAX | MIN | MAX | |
| V_{CC} | Supply voltage | 2 | 6 | 2 | 6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 3$ V | | 2.1 | | V |
| | | $V_{CC} = 4.5$ V | | 3.15 | | |
| | | $V_{CC} = 5.5$ V | | 3.85 | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 3$ V | | 0.9 | | V |
| | | $V_{CC} = 4.5$ V | | 1.35 | | |
| | | $V_{CC} = 5.5$ V | | 1.65 | | |
| V_I | Input voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| V_O | Output voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} | High-level output current | $V_{CC} = 3$ V | | –12 | | mA |
| | | $V_{CC} = 4.5$ V | | –24 | | |
| | | $V_{CC} = 5.5$ V | | –24 | | |
| I_{OL} | Low-level output current | $V_{CC} = 3$ V | | 12 | | mA |
| | | $V_{CC} = 4.5$ V | | 24 | | |
| | | $V_{CC} = 5.5$ V | | 24 | | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 8 | | 8 | | ns/V |
| T_A | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54AC08, SN74AC08 QUADRUPLE 2-INPUT POSITIVE-AND GATES

SCAS536D – SEPTEMBER 1995 – REVISED OCTOBER 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | SN54AC08 | | SN74AC08 | | UNIT |
|---------------------------------------|--------------------------|---|-----------------------|-------|------|----------|------|----------|------|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = -50 μA | 3 V | 2.9 | | | 2.9 | | 2.9 | V | |
| | | 4.5 V | 4.4 | | | 4.4 | | 4.4 | | |
| | | 5.5 V | 5.4 | | | 5.4 | | 5.4 | | |
| | I _{OH} = -12 mA | 3 V | 2.56 | | | 2.4 | | 2.46 | | |
| | | 4.5 V | 3.86 | | | 3.7 | | 3.76 | | |
| | I _{OH} = -24 mA | 4.5 V | 3.86 | | | 3.7 | | 3.76 | | |
| | | 5.5 V | 4.86 | | | 4.7 | | 4.76 | | |
| I _{OH} = -50 mA [†] | 5.5 V | | | | 3.85 | | | | | |
| I _{OH} = -75 mA [†] | 5.5 V | | | | | | 3.85 | | | |
| V _{OL} | I _{OL} = 50 μA | 3 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | 5.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | I _{OL} = 12 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | I _{OL} = 24 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | 5.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| I _{OL} = 50 mA [†] | 5.5 V | | | | | 1.65 | | | | |
| I _{OL} = 75 mA [†] | 5.5 V | | | | | | | 1.65 | | |
| I _I | A or B ports | V _I = V _{CC} or GND | 5.5 V | | | ±0.1 | | ±1 | ±1 | μA |
| I _{CC} | | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 2 | | 40 | 20 | μA |
| C _i | | V _I = V _{CC} or GND | 5 V | | 4.5 | | | | | pF |

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | T _A = 25°C | | | SN54AC08 | | SN74AC08 | | UNIT |
|------------------|--------------|-------------|-----------------------|-----|-----|----------|------|----------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | A or B | Y | 1.5 | 7.5 | 9.5 | 1 | 12.5 | 1 | 10 | ns |
| t _{PHL} | | | 1.5 | 7 | 8.5 | 1 | 11.5 | 1 | 9 | |

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | T _A = 25°C | | | SN54AC08 | | SN74AC08 | | UNIT |
|------------------|--------------|-------------|-----------------------|-----|-----|----------|-----|----------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | A or B | Y | 1.5 | 5.5 | 7.5 | 1 | 9 | 1 | 8.5 | ns |
| t _{PHL} | | | 1.5 | 5.5 | 7 | 1 | 8.5 | 1 | 7.5 | |

operating characteristics, V_{CC} = 5 V, T_A = 25°C

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|---|-----------------------------------|-----|------|
| C _{pd} Power dissipation capacitance | C _L = 50 pF, f = 1 MHz | 20 | pF |

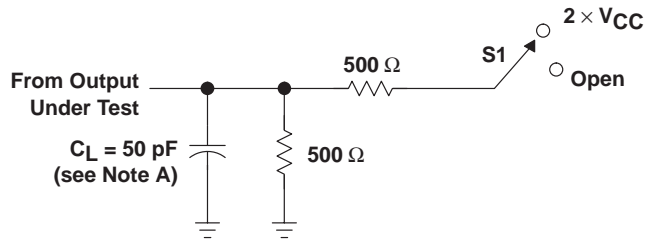


SN54AC08, SN74AC08 QUADRUPLE 2-INPUT POSITIVE-AND GATES

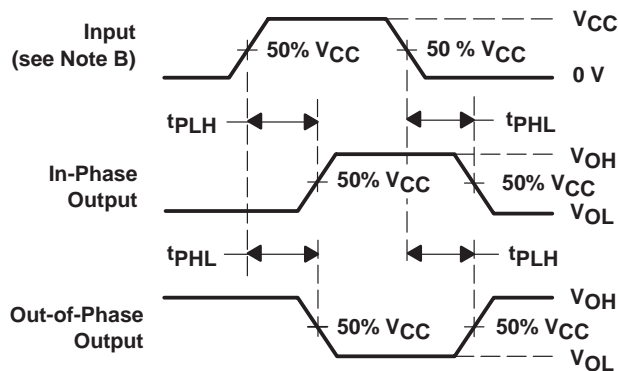
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PARAMETER MEASUREMENT INFORMATION

| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |



LOAD CIRCUIT



VOLTAGE WAVEFORMS

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

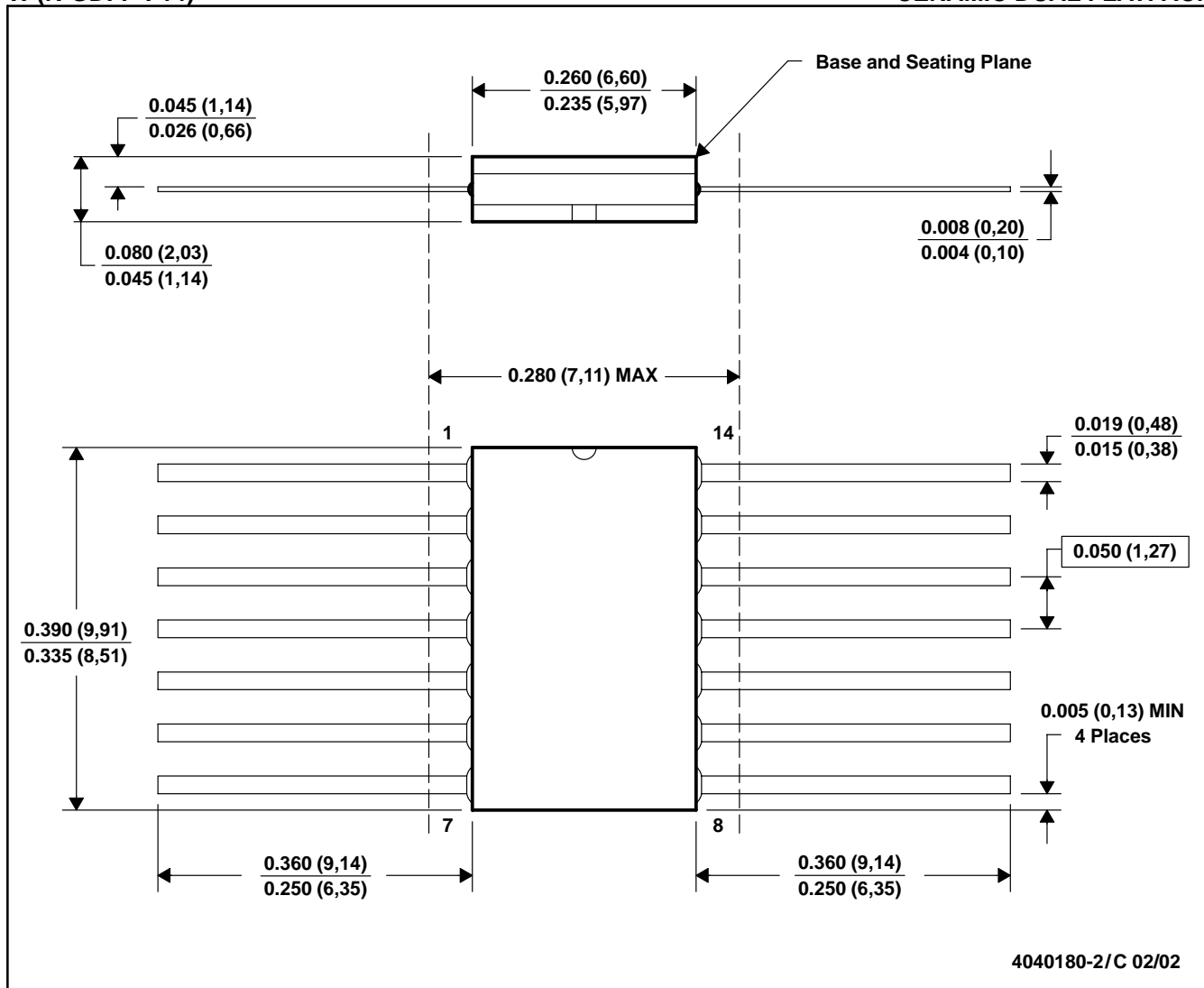


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.
 E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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