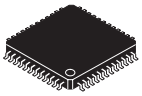
TEXAS INSTRUMENTS



SLUS513A − MAY 2003 − REVISED JULY 2004

DUAL-SLOT PCI HOT-PLUG POWER CONTROLLER WITH I²C INTERFACE

FEATURES

- **12-V, −12-V, 3.3-V, 5-V Main Power Switching and Auxiliary 3.3-V Power Switching**
- **12-V, −12-V And Auxiliary 3.3-V Power FETs**
- **Hot-Swap Protection and Control of All Supplies**
- **Overcurrent Protection for All Supplies**
- **Isolation of Any Load Fault in One Slot from Any Other Slot**
- **Undervoltage Monitoring for the Main 12-V, 3.3-V, 5-V and Auxiliary 3.3-V Supplies**
- **Power Fault Latching**
- **Overtemperature Shutdown**
- **I²C Interface for Power Control, Power Status, Slot Control And Slot Status**
- **Compliant To PCI And PCI-X Hot Plug Specifications**
- **One TPS2341 Supports Two Slots**

DESCRIPTION

The TPS2341 contains main supply power control, auxiliary supply power control, power FETs for 12-V, −12-V and auxiliary 3.3-V supplies, and a serial interface for communications with and control of slots. Each TPS2341 contains supply control and switching for two slots.

The main power control circuits start with all supplies off and hold all supplies off until power to the TPS2341 is valid on all positive supplies. When power is requested, the control circuit applies constant current to the gates of the power FETs, allowing each FET to ramp the load voltage linearly. Each main supply can be programmed for a desired ramp rate by selecting a gate capacitor for the power FET for that supply. The power control circuits also monitor load current and latch off that slot if the load current exceeds a programmed maximum value. In addition, once the 12-V, the 5-V, and the 3.3-V FET are fully enhanced, the load voltage is monitored. If the load voltage drops out of specification limit after these FETs are fully enhanced, the slot latches off. This feature provides another level of protection from load fault.

The auxiliary power control circuit provides power to the 3VAUXx pins through the 3.3-V main supply when it is above 3.0 V, and through the 3.3-V standby input supply when the 3.3-V main supply drops below 3.0 V.

The TPS2341 contains power FETs for 12 V at 500 mA, −12 V at 100 mA, and auxiliary 3.3 V at 375 mA for each slot. These power FETs are short-circuit protected, slew rate controlled, and over-temperature protected.

The serial interface communicates with a slot controller using the I²C serial protocol. The interface communicates with the slot, and mechanical switches with individual, dedicated lines. The interface operates from the 3.3-V auxiliary power, but inputs are 5-V tolerant. Mechanical switch inputs have internal pull-up and hysteresis. The serial interface controls slot power, and monitors board, power fault, and switch input status.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage range:	P12VIN	−0.5 V to 15 V
	M12VIN	−15.0 V to 0.5 V
	All others	−0.5 V to 6 V
Output voltage range:	P12VO, 5V3VG	−0.5 V to V_{P12VIN} +0.5 V
	P12VG	−0.5 V to 28 V
	M12VO, M12VG	V_{M12VIN}−0.5 V to 0.5 V
Output current pulse:	P12VO (DC internally limited)	4 A
	M12VO	0.8 A
Operating virtual temperature range, T_J		−40°C to 125°C
Storage temperature range, T_{stg}		−55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages are respect to DGND.

electrical characteristics over recommended operating temperature range, P12VINA = P12VINB = 12 V, V5IN = 5 V, V3IN = 3.3 V, DIGVCC = 3.3 V, M12VINA = M12VINB = −12 V, 3VSTBYIN = 3.3 V, all outputs unloaded, −40°C to 85°C, $T_A = T_J$ (unless otherwise noted)

5-V/3.3-V Supply

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$5V_{OC}$ input threshold voltage	R_{OCSET} = 6.04 kΩ,	$T_A = T_J$ = 25°C	35	42	49	mV
$5V_{OC}$ Input threshold voltage	R_{OCSET} = 6.04 kΩ		34	42	49	mV
$3V_{OC}$ Input threshold voltage	R_{OCSET} = 6.04 kΩ,	$T_A = T_J$ = 25°C	41	52	60	mV
$3V_{OC}$ input threshold voltage	R_{OCSET} = 6.04 kΩ		37	52	62	mV
5VISA, 5VISB voltage fault threshold	After P12VG and 5V3VG good		4.3	4.65	4.86	V
5VISA, 5VISB voltage fault minimum captured pulse				75	100	ns
5VSA, 5VSB input bias current	PWRENx = high		−100		100	µA
5VISA, 5VISB input bias current	PWRENx = high			250		
5VISA, 5VISB bleed current	PWRENx = low,	5VISx = 5 V	5	10	20	mA
3VISA, 3VISB voltage fault threshold	After P12VG and 5V3VG good		2.70	2.86	3.05	V
3VISA, 3VISB voltage fault minimum captured pulse time				75	100	ns
3VSA, 3VSB input bias current	PWRENx = high		−100		100	µA
3VISA, 3VISB input bias current	PWRENx = high			250		
3VISA, 3VISB bleed current	PWRENx = low,	3VISx = 3.3 V	5	10	20	mA
5V3VGA, 5V3VGB charge current			14	20	25	µA
5V3VGA, 5V3VGB discharge current				200		mA
5V3VGA, 5V3VGB good threshold	P12VIN = 12V		9.5	11	11.5	V
5V3VGA, 5V3VGB turn-off time	C_{5V3VG} = 0.022 µF, 5V3VG falling from 90% to 10%			1		µs

electrical characteristics over recommended operating temperature range, P12VINA = P12VINB = 12 V, V5IN = 5 V, V3IN = 3.3 V, DIGVCC = 3.3 V, M12VINA = M12VINB = −12 V, 3VSTBYIN = 3.3 V, all outputs unloaded, −40°C to 85°C, $T_A = T_J$ (unless otherwise noted) (continued)

+12-V Supply / −12-V Supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
+12-V Internal N-channel MOSFET on-resistance	PWREN = HIGH, I_D = 0.5 A, $T_A = T_J$ = 25°C		0.18	0.3	Ω
	PWREN = HIGH, I_D = 0.5 A			0.4	Ω
−12-V Internal N-channel MOSFET on-resistance	PWREN = HIGH, I_D = 0.1 A, $T_A = T_J$ = 25°C		0.5	0.75	Ω
	PWREN = HIGH, I_D = 0.1 A			0.9	
+12-V overcurrent threshold	R_{OCSET} = 6.04 kΩ, $T_A = T_J$ = 25°C	0.79	0.94	1.09	A
	R_{OCSET} = 6.04 kΩ	0.73	0.94	1.12	A
−12-V overcurrent threshold	R_{OCSET} = 6.04 kΩ, $T_A = T_J$ = 25°C	0.20	0.24	0.28	A
	R_{OCSET} = 6.04 kΩ	0.18	0.24	0.30	A
P12VOA, P12VOB fault threshold voltage	After P12VG and 5V3VG good	9.50	10.30	11.15	V
P12VOA, P12VOB voltage fault minimum captured pulse time			75	100	ns
M12VGA, M12VGB gate charge current		−23	−20	−13	µA
M12VGA, M12VGB gate discharge current			200		mA
P12VGA, P12VGB, charge current	Derived from charge pump	2	9	14	µA
P12VGA, P12VGB, discharge current			100		mA
P12VGA, P12VGB good threshold		17.5	19.0	20.5	V
Turn-on time	PWREN = HIGH to M12VO = −10.4 V, C_{M12VG} = 0.022 µF, R_L = 120 Ω, C_{M12VO} = 50 µF		15	20	ms
	PWREN = HIGH to P12VO = 11.4 V, C_{12PVG} = 0.022 µF, R_L = 24 Ω, C_{P12VO} = 200 µF		30	75	
Turn-off time	PWREN = LOW to P12VO = 0.6 V, CP12VG = 0.022 µF		1.5	3.5	µs
	PWREN = LOW to M12VO = −0.6 V, CM12VG = 0.022 µF		1.5	3.5	µs
M12VOA, M12VOB bleed current			−20		mA
P12VOA, P12VOB bleed current			10		

noise filter

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Ignored spike from overcurrent			250		ns
Latched spike from overcurrent			500		ns

electrical characteristics over recommended operating temperature range, P12VINA = P12VINB = 12 V, V5IN = 5 V, V3IN = 3.3 V, DIGVCC = 3.3 V, M12VINA = M12VINB = −12 V, 3VSTBYIN = 3.3 V, all outputs unloaded, −40°C to 85°C, $T_A = T_J$ (unless otherwise noted) (continued)

input/output control

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P12VINA, P12VINB supply current	PWRENx = LOW, P12VIN = 12 V		2		mA
V5IN supply current	V5IN = 5 V		1		
V3IN supply current	V3IN = 3.3 V		1000		μA
M12VINA, M12VINB supply current	PWRENx = LOW, M12VIN −12 V		250		
3VSTBYIN supply current	3VSTBYIN = 3.3 V		200		
DIGVCC supply current	DIGVCC = 3.3 V		200		
Overcurrent fault response time			500	960	ns
V3IN start-up threshold voltage		2.6	2.8	3.05	V
V3IN stop threshold voltage		2.35	2.55	2.80	
V5IN start-up threshold voltage		4.1	4.4	4.65	
V5IN stop threshold voltage		3.75	4.00	4.35	
P12VIN start-up threshold voltage		10.1	10.8	11.3	
P12VIN stop threshold voltage		9.5	10.0	11.0	

3.3 VAUX

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V3IN slow overcurrent shutdown	Load applied for > 1 ms, $T_A = T_J = 25°C$	0.7	1.0	1.3	A
	Load applied for > 1 ms	0.6	1.0	1.4	
V3IN slow overcurrent fault response time		0.3	1.0	2.0	ms
V3IN fast overcurrent shutdown	Load applied for < 100 μs, $T_A = T_J = 25°C$	1.15	1.5	1.85	A
	Load applied for < 100 μs	1.0	1.5	2.0	
V3IN fast overcurrent fault response time		5	10	35	μs
3VSTBYIN overcurrent shutdown		20	40	60	mA
3VSTBYIN overcurrent fault response time		10	25	50	μs
V3IN to 3VAUXA, 3VAUXB main switch on-resistance	I_{3VAUXx} = −500 mA		300	425	mΩ
3VSTBYIN to 3VAUXA, 3VAUXB standby switch on-resistance	I_{3VAUXx} = −10 mA		10	20	Ω
3VSTBYIN undervoltage lockout		2.0	2.5	2.9	V
V3IN to 3VAUXA, 3VAUXB turn-on slew rate			5		V/ms
3VSTBYIN to 3VAUXA, 3VAUXB turn-on slew rate			0.1		
3VAUXA, 3VAUXB turn-on time from SWA/SWB	from SWx < 0.8 V, C_{3VAUXx} = 150 μF		3		ms
3VAUXA, 3VAUXB turn-off time from SWA/SWB	from SWx > 2 V		2.5		
3VSTBYIN to V3IN crossover time			10		μs
V3IN to 3VSTBYIN crossover time			100		
3VSTBYIN to V3IN crossover threshold		2.8	2.9	3.0	V
3VSTBYIN to V3IN crossover hysteresis			50		mV
3VAUXA, 3VAUXB bleed current	3VAUXx = 3 V		150		μA

ac switching characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MAX} operating clock frequency	$0 \le T_A \le 70°C$	0	100	400	kHz
Recommended input rise and fall times	10% to 90% of DIGVCC	0.2		1	ns

electrical characteristics over recommended operating temperature range, P12VINA = P12VINB = 12 V, V5IN = 5 V, V3IN = 3.3 V, DIGVCC = 3.3 V, M12VINA = M12VINB = −12 V, 3VSTBYIN = 3.3 V, all outputs unloaded, −40°C to 85°C, $T_A = T_J$ (unless otherwise noted) (continued)

dc electrical characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input threshold voltage (SDA, SCL)		0.8	1.4	2.0	V
High-level input threshold voltage (SWA, SWB, PGOOD)		1.9	2.4	2.8	
Low-level input threshold voltage (SWA, SWB, PGOOD)		0.4	0.8	1.2	
Input hysteresis (SWA, SWB, PGOOD)		1.0	1.6	2.0	
Address and enable threshold voltage (ADDR1, ENA, ENB)		0.4	1.0	1.5	
Address and enable hysteresis voltage (ADDR1, ENA, ENB)			200		mV
Address and enable floating voltage when not externally driven (ADDR1, ENA, ENB)			1.65		V
Address and enable Thevenin equivalent impedance (ADDR1, ENA, ENB)			50		kΩ
Test mode threshold voltage (ADDR1)		1.75	2.50	2.80	V
Test mode hysteresis voltage (ADDR1)			200		mV
High-level output voltage (all digital outputs, except IRQ# and SDA)	I_L = −4 mA	DIGVCC − 0.4	DIGVCC − 0.2		V
Low-level output voltage (all digital outputs)	I_L = 4 mA		0.2	0.4	
3.3 V pull-up resistance (SWA, SWB, PGOOD)		30		200	kΩ

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, P12VINA, P12VINB	10.8	13.2	V
Input voltage, V5IN	4.75	5.25	
Input voltage, DIGVCC	3.1	3.5	
Input voltage, M12VINA, M12VINB	−13.2	−10.8	
Input voltage, 3VSTBYIN	3.1	3.5	
Load current, P12VOA, P12VOB	0	500	mA
Load current, M12VOA, M12VOB	0	100	
Load current, 3VAUXA, 3VAUXB	0	375	

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
3VAUXA	36	O	3.3Vaux voltage supply outputs. A 0.01-µF bypass capacitor to PWRGND2 is recommended.
3VAUXB	35	O	
3VISA	30	I	Connect to the load side of the sense resistor. See definition for 3VS. This pin has a switched FET to PWRGND to discharge any output load capacitance when the output is turned off. A 0.01-µF bypass capacitor to AGND is recommended.
3VISB	7	I	
3VSA	31	I	Connect to the source side of the 3.3-V FET switch. This pin in conjunction with the 3VIS pin senses the current to the 3.3-V load by sensing the voltage drop across a sense resistor. A 0.01-µF bypass capacitor to AGND is recommended.
3VSB	6	I	
3VSTBYIN	37	P	3.3Vaux standby voltage supply input. A 0.1-µF bypass capacitor to PWRGND2 is recommended.
5V3VGA	33	O	Gate drive for the 5-V and 3.3-V FET switches. Ramp rate is programmed by external capacitance connected to this pin. The capacitor is charged with a 20-µA current source and discharged with a switch to PWRGND. The output UV circuitry is disabled until the voltage on this pin is greater than 11 V and the voltage on P12VGx is greater than 20 V.
5V3VGB	5	O	
5VISA	29	I	Connect to the load side of the sense resistor. See definition for 5VS. 5VIS is also used to sense the output voltage for the 5-V UV circuit. This pin has a switched FET to PWRGND to discharge any output load capacitance when the output is turned off. A 0.01-µF bypass capacitor to AGND is recommended.
5VISB	8	I	
5VSA	28	I	Connect to the source of the 5-V FET switch. This pin in conjunction with the 5VIS pin senses the current to the 5-V load by sensing the voltage drop across the sense resistor. A 0.01-µF bypass capacitor to AGND is recommended.
5VSB	9	I	
ADDR1	17	I	Hard-wired I^2C address pin. This pin represents the least significant bit (LSB) of a device's I^2C address. Tie to DGND for a logic 0 or allow to float for a logic 1. Tie ADDR1 to DIGVCC for test mode fault mask.
AGND	11	G	Ground pin for the internal analog section.
AUX_GOODA	27	O	Output power good indicator for the 3.3-VAUXx ouptut. This pin is driven to DIGVCC when the internal N-channel MOSFET connected between V3IN and 3VAUXA (or 3VAUXB for slot B) is fully enhanced.
AUX_GOODB	19	O	
DIGVCC	24	P	Power pin for the digital section, connect to 3VSTBYIN. A 0.1-µF bypass capacitor from DIGVCC to DIGGND is recommended.
DGND	23	G	Ground pin for the internal digital section.
ENA	15	I	Hardware enable pins. Use these pins to enable the device without I^2C communication. Pull ENA high to enable slot A. Pull ENB high to enable slot B. Pull ENA low to disable slot A hardware control and revert to I^2C control. Transitioning ENA from high to low also clears the slot A main fault latch. Pull ENB low to disable slot B hardware control and revert to I^2C control. Transitioning ENB from high to low also clears the slot B main fault latch.
ENB	16	I	
IRQ#	18	O	Interrupt output. Open drain pulls low upon any fault detection or if SWA or SWB changes state.
M12VGA	41	O	A capacitor connected from this pin to M12VOA programs the ramp rate of the −12-V switched output. The capacitor is charged with a 20-µA current source and discharged with a switch to PWRGND.
M12VGB	48	O	A capacitor connected from this pin to M12VOB programs the ramp rate of the −12-V switched output. The capacitor is charged with a 20-µA current source and discharged with a switch to PWRGND.
M12VIN	2	P	−12-V input voltage to the device. M12VIN, M12VINA and M12VINB must be tied together and are internally connected by a high-resistance path. The heat conduction pad on the back of the package is also connected to M12VIN. A 0.1-µF bypass capacitor from M12VIN to PWRGND is recommended.
M12VIN	39	P	
M12VINA	40	P	−12-V input voltage to the device and the −12-V power FET. M12VINA, and M12VINB and M12VIN must be tied together and are internally connected by a high-resistance path. The heat conducting pad on the back of the package is also connected to M12VIN. A 0.1-µF bypass capacitor from M12VIN to PWRGND is recommended.
M12VINB	1	P	
M12VOA	38	O	−12-V Switched output. This pin has a switched FET to PWRGND to discharge any output load capacitance when the output is turned off. A 0.01-µF bypass capacitor to PWRGND is recommended.
M12VOB	3	O	
OCSET	10	I	A resistor connected between this pin and AGND sets the overcurrent threshold of the internal switches. The +12-V and −12-V switches are set for the maximum permissible currents per the PCI specification when a 1%, 6.04-kΩ resistor is used. A 0.1-µF bypass capacitor from OCSET to ANAGND is recommended.

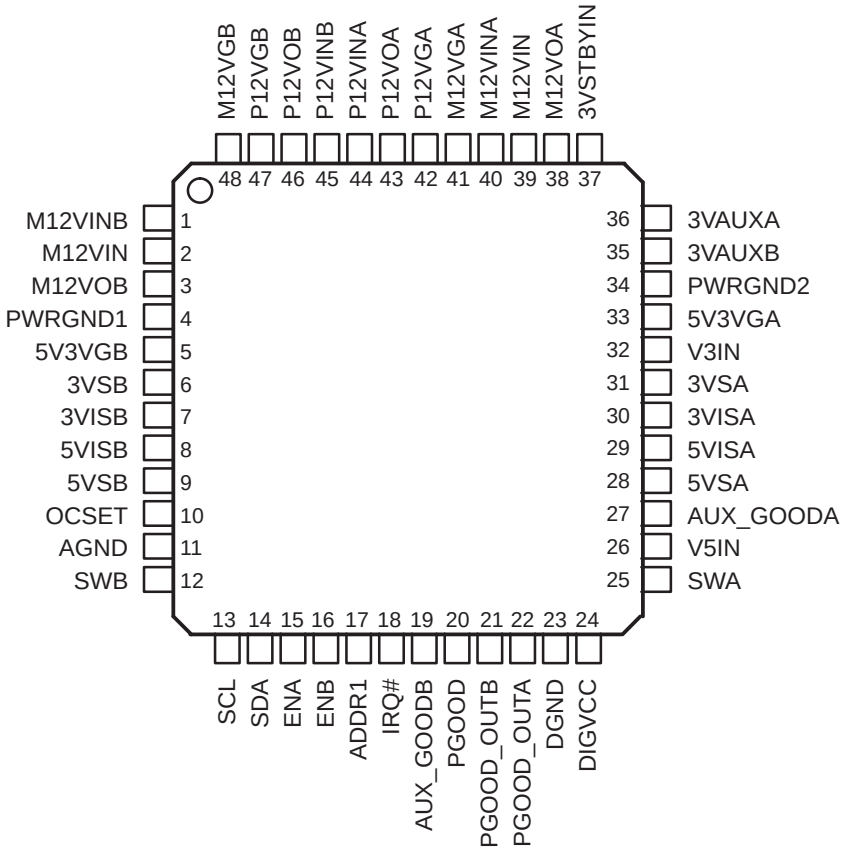
Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
P12VGA	42	O	Gate drive for the 12-V internal N-channel MOSFET for slot A. Connect a capacitor from this pin to PWRGND1 to program the ramp rate. The capacitor is charged with a 5−μA current source and discharged with a switch. The output undervoltage circuitry is disabled until the voltage on this pin is greater than 20 V and the voltage on 5V3VGA is greater than 11 V.
P12VGB	47	O	Gate drive for the 12-V internal N-channel MOSFET for slot B. Connect a capacitor from this pin to PWRGND2 to program the ramp rate. The capacitor is charged with a 5-μA current source and discharged with a switch. The output undervoltage circuitry is disabled until the voltage on this pin is greater than 20 V and the voltage on 5V3VGB is greater than 11 V.
P12VINA	44	P	12-V input to the device and the 12-V power FET for slot A. A 0.1-μF bypass capacitor from P12VINA to PWRGND1 is recommended.
P12VINB	45	P	12-V input to the device and the 12-V power FET for slot B. A 0.1-μF bypass capacitor from P12VINB to PWRGND2 is recommended.
P12VOA	43	O	12-V switched output for slot A. This pin has a switched FET to ground to discharge any output load capacitance when the output is turned off. A 0.01-μF bypass capacitor to PWRGND1 is recommended.
P12VOB	46	O	12-V switched output for slot B. This pin has a switched FET to ground to discharge any output load capacitance when the output is turned off. A 0.01-μF bypass capacitor to PWRGND2 is recommended.
PGOOD	20	I	Power good input. PGOOD has hysteresis so that it can be used as a power-on reset, driven from a slow-rising RC. PGOOD also has a 100-kΩ pull-up to DIGVCC.
PGOOD_OUTA	22	O	Output power good indicator for the main slot outputs. This pin is driven to DIGVCC when the voltage on P12VGA (or P12VGB for slot B) is greater than 20 V and the voltage on 5V3VGA (or 5V3VGB for slot B) is greater than 11 V.
PGOOD_OUTB	21	O	
PWRGND1	4	G	Ground pin for the power analog section.
PWRGND2	34	G	
SCL	13	I	Serial clock line for the I^2C bus.
SDA	14	I/O	Serial data line for the I^2C bus.
SWA	25	I	Slot A switch input. Low indicates the slot is populated. This input has hysteresis and a 100-kΩ pull-up to DIGVCC, requiring only a capacitor to ground for debouncing mechanical noise.
SWB	12	I	Slot B switch input. Low indicates the slot is populated. This input has hysteresis and a 100-kΩ pull-up to DIGVCC, requiring only a capacitor to ground for debouncing mechanical noise.
V3IN	32	P	3.3-V input to the device. A 0.1-μF bypass capacitor from V3IN to PWRGND is recommended.
V5IN	26	P	5-V input to the device. A 0.1-μF bypass capacitor from V5IN to PWRGND is recommended.

AVAILABLE OPTIONS

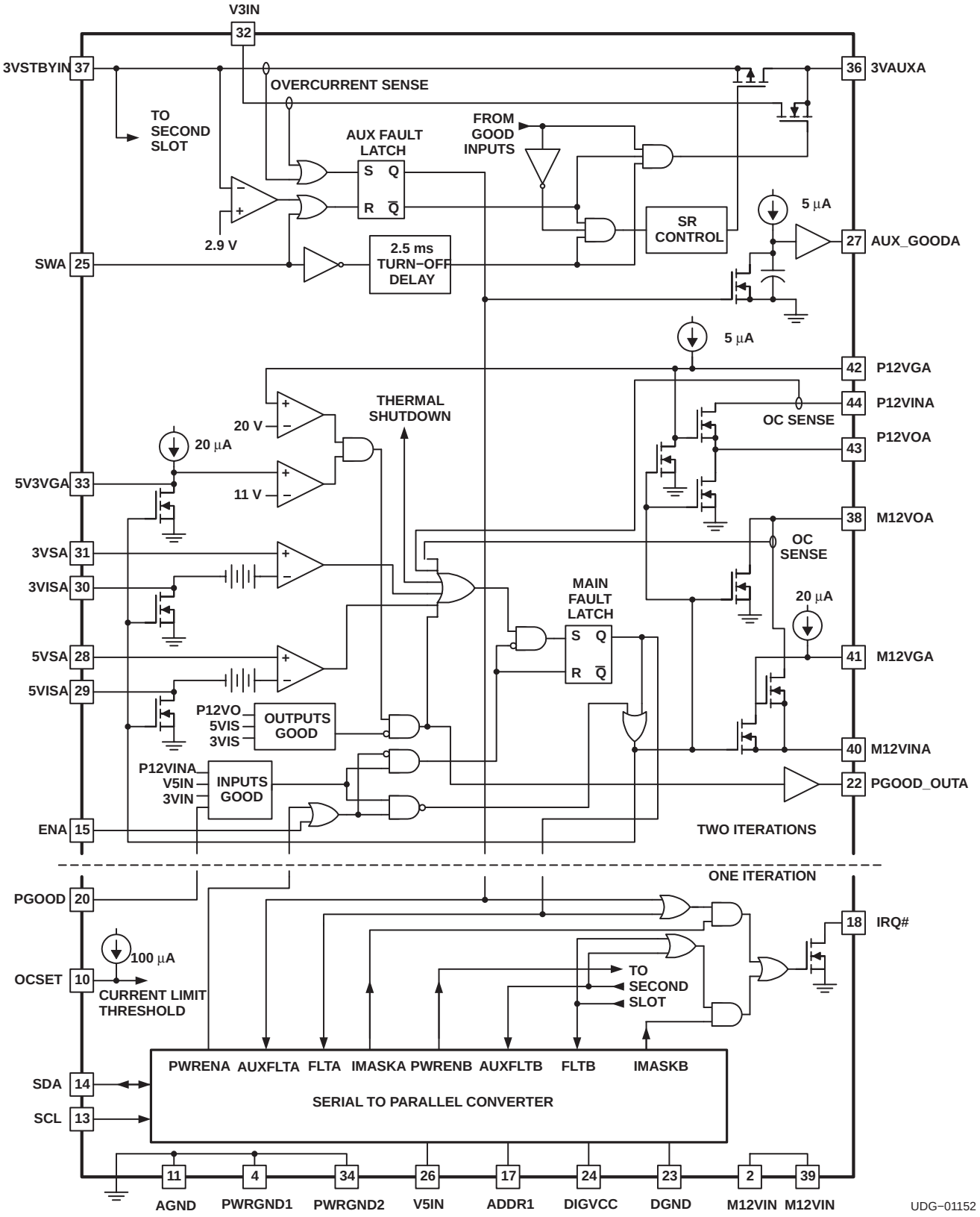
T_A	PACKAGE
	HTQFP (PHP)
−40°C to 85°C	TPS2341PHP

PHP PACKAGE
(TOP VIEW)



The heat-conduction pad on the underside of the package is electrically connected to M12VINA. Either connect the heat-conducting pad to −12 VIN or leave unconnected. Do not connect the heat-conducting pad to any other power plane or to a ground.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Refer to the typical application diagram (Figure 13) for circuit component values for Figures 1 through 9.

MAIN SWITCH RAMPUP VOLTAGE vs TIME

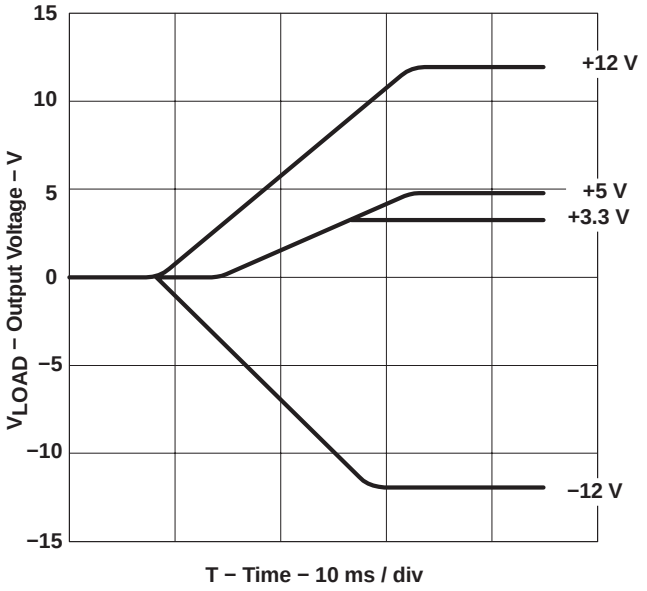


Figure 1.

3.3-V MAIN SWITCH UNDERVOLTAGE FAULT RESPONSE vs TIME

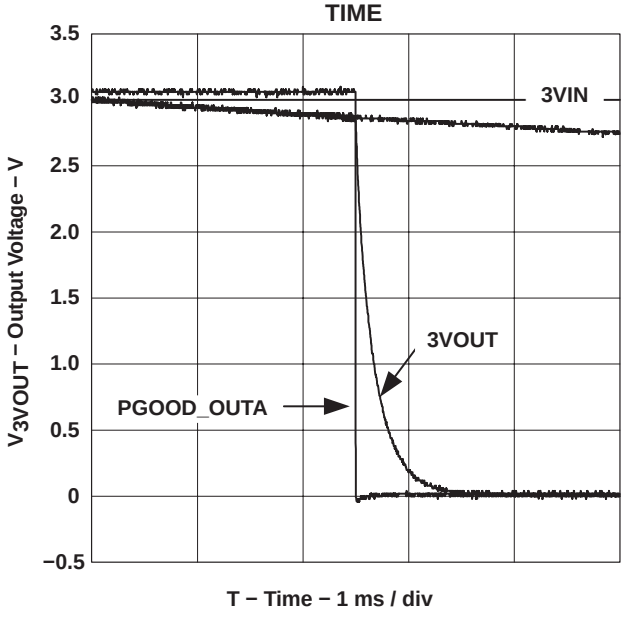


Figure 2.

12-V OUTPUT AND INRUSH CURRENT vs TIME

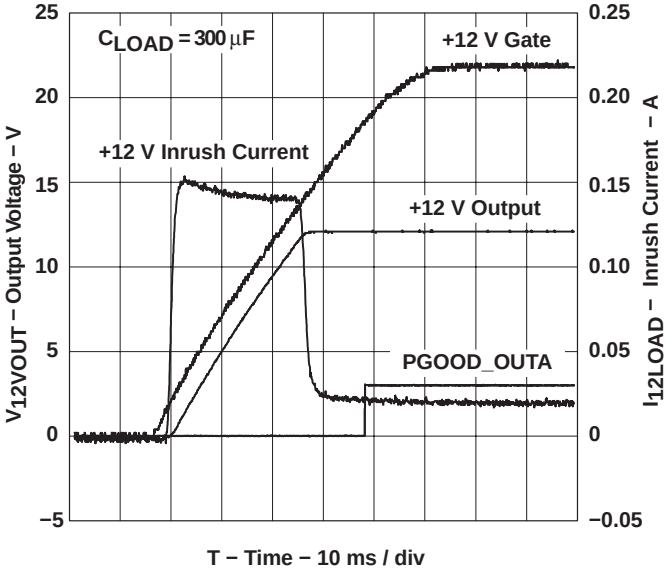


Figure 3.

5-V OUTPUT OVERLOAD RESPONSE vs TIME

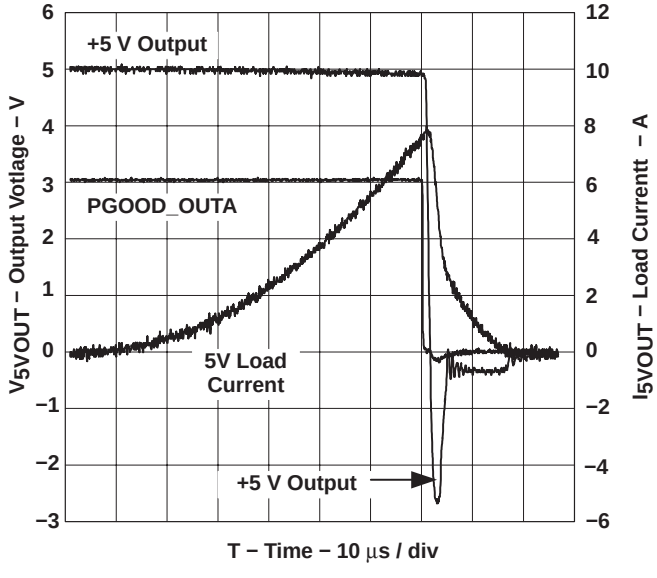


Figure 4.

TYPICAL CHARACTERISTICS

Refer to the typical application diagram (Figure 13) for circuit component values for Figures 1 through 9.

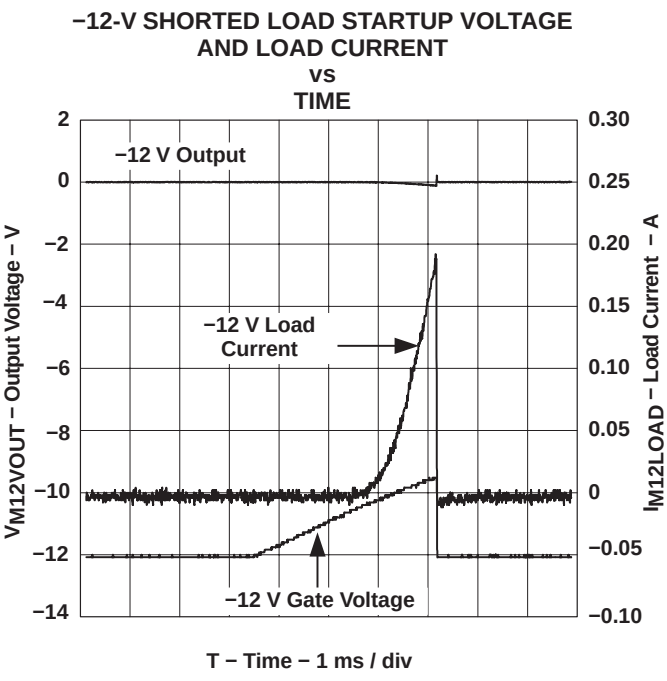


Figure 5.

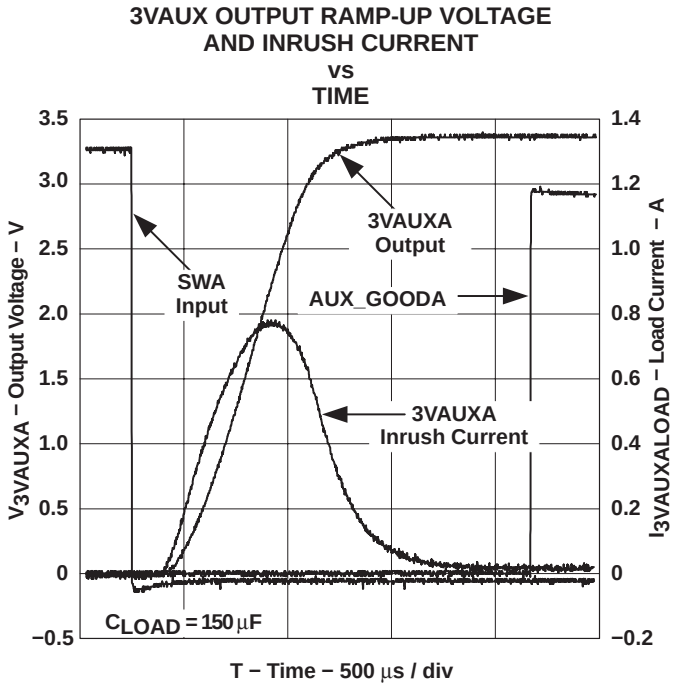


Figure 6.

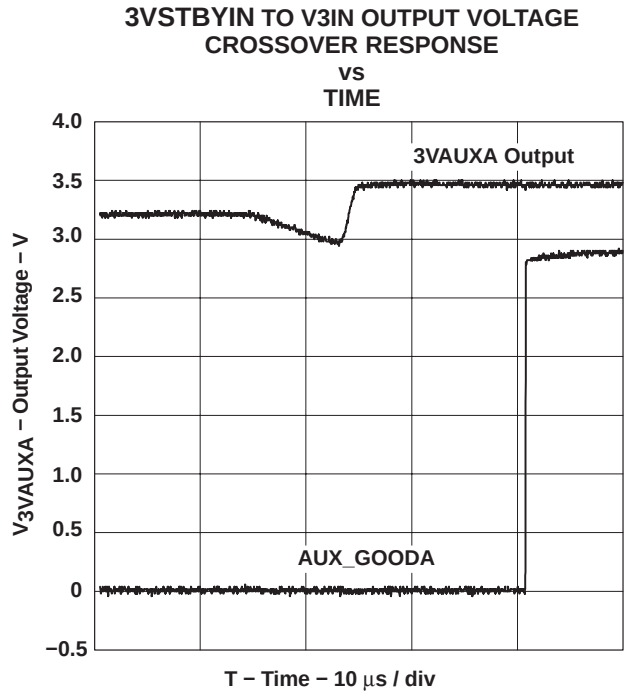


Figure 7.

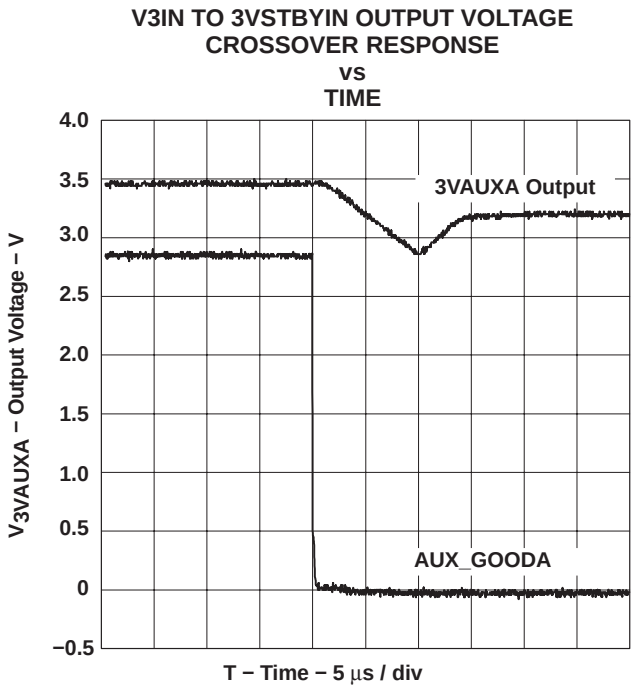


Figure 8.

TYPICAL CHARACTERISTICS

Refer to the typical application diagram (Figure 13) for circuit component values for Figures 1 through 9.

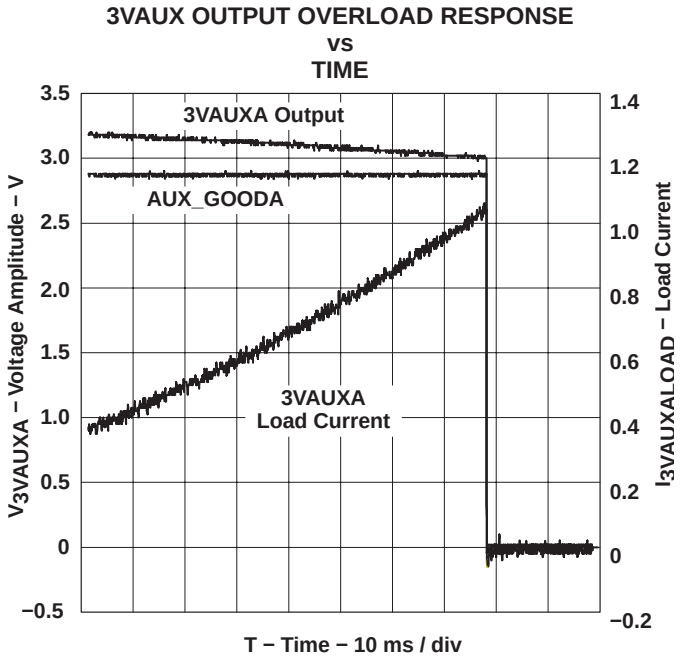


Figure 9.

APPLICATION INFORMATION

The functional block diagram shows the TPS2341 with detailed information on the analog functions. For clarity, the analog circuits for only one slot are shown in detail.

+12-V Supply Control

The TPS2341 integrates an N-channel power MOSFET for the +12-V supply between pins P12VINA and P12VOA. The switch has a nominal on resistance of 180 mΩ and shuts down the slot upon detecting an overcurrent condition. The in-rush current of the supply is controlled in an open-loop fashion by charging an external capacitor tied directly to the internal N-channel MOSFET gate with a constant current source. This results in a linear voltage ramp on the gate and also on the P12VOA output due to the source follower connection of the switch.

The switch turns on when the logic declares the input supplies are valid, slot is healthy and the enable from the I^2C serial interface is active. The P12VOA output voltage is monitored for an undervoltage fault once the +12-V, +5-V and +3.3-V switches are fully enhanced. The switch shuts off upon a disable command from the I^2C serial interface or a fault on the slot. An internal resistor connects between the P12VOA and PWRGND1 upon disable and bleeds off any residual charge on the output.

Slot B functions independently and in the same manner as slot A with the input supply connected to P12VINB and the load connected to P12VOB.

−12-V Supply Control

The TPS2341 integrates an N-channel power MOSFET for the −12-V supply between pins M12VINA and M12VOA. The switch has a nominal on resistance of 500 mΩ and shuts down the slot upon detecting an overcurrent condition. The in-rush current of the supply is controlled in a closed-loop fashion by charging an external Miller capacitor tied between the N-channel MOSFET gate and drain with a constant current source. This results in a linear voltage ramp on the drain (M12VOA) pin.

The switch turns on when the logic declares the input supplies are valid, slot is healthy and the enable from the I^2C serial interface is active. The M12VOA output voltage is not monitored for an undervoltage fault. The switch shuts off upon a disable command from the I^2C serial interface or a fault on the slot. An internal resistor connects between the M12VOA and PWRGND1 upon disable and bleeds off any residual charge on the output.

Slot B functions independently and in the same manner as slot A with the input supply connected to M12VINB and the load connected to M12VOB.

APPLICATION INFORMATION

+5-V and +3.3-V Supply Controls

The TPS2341 provides the control circuitry for external N-channel power MOSFETs on the +5-V and +3.3-V supplies. The switches share a common gate capacitor for slew rate control and have independent overcurrent detection circuitry. A source side sense resistor provides a differential sense voltage to pins 5VSA and 5VISA that is compared to a threshold voltage for the +5-V supply overcurrent fault. The +3.3-V supply operates similarly and a fault on either supply shuts down the slot. The in-rush current of the supply is controlled in a open-loop fashion by charging an external capacitor tied directly to the N-channel MOSFET gate with a constant current source. This results in a linear voltage ramp on the gate and also on the load due to the source follower connection of the switch.

The switch turns on when the logic declares the input supplies are valid, slot is healthy and the enable from the I^2C serial interface is active. The 3VISA and 5VISA pins are monitored for an undervoltage fault once the +12-V, +5-V and +3.3-V switches are fully enhanced. The switch shuts off upon a disable command from the I^2C serial interface or a fault on the slot. An internal resistor connects between 3VISA and PWRGND1 and also between 5VISA and PWRGND1 upon disable and bleeds off any residual charge on the output.

Slot B functions independently and in the same manner as slot A.

3VAUX Supply Control

The TPS2341 integrates the power FETs for the 3.3 V auxiliary outputs providing power from V3IN when the main supply is above 3 V and from the 3VSTBYIN supply when V3IN is below 3 V.

The 3VAUX circuit differs from the main circuits in regard to slew rate control. The main circuits slew rate is programmable by an external capacitor while the 3VAUX slew rate is fixed. The 3VAUX outputs turn on and slew up upon the application of 3VSTBYIN and SW. The slew rate is slow enough to allow charging a large bulk capacitor (up to 150 μF) without tripping the overload comparator. After the main supply inputs are active, the 3VAUX switch connected to 3VSTBYIN shuts off and the switch connected to V3IN turns on in a rapid break-before-make fashion.

Upon the undervoltage failure of the V3IN or one of the positive main supplies, the V3IN switch shuts off and the 3VSTBYIN switch turns on in a rapid break-before-make fashion. A high on the SW input shuts off the active switch.

The V3IN switch has slew rate control slow enough to allow charging the bulk capacitance in the event that 3VSTBYIN and the main supplies become active together.

The V3IN switches have two overcurrent thresholds. The slow overcurrent threshold trips when the load current exceeds 1 A for longer than 1 ms. The 3VAUX outputs can accomodate a transient current due to a load device enable or charge up to 150 μF of bulk capacitance without tripping a nuisance fault. The fast overcurrent threshold trips when the load current exceeds 1.5 A for longer than 10 μs. This threshold captures a direct short on the 3VAUX output.

The 3VSTBYIN switches detect an overcurrent condition when the load current exceeds 40 mA for 25 μs.

The main and standby faults are cleared by disabling the 3VAUX slot with the SW input or by removing the input supply voltage.

APPLICATION INFORMATION

Fault Logic

The main supply switches require the inputs to be healthy before turning on. The slot is shut down upon an overload condition or output undervoltage condition and all switches shut off upon a device overtemperature condition. The switch starts to turn on when the P12VINA, V5IN and V3IN supply inputs are above the undervoltage thresholds, the PGOOD input is active and the PWRENA (or PWRENB for slot B) control output from the I^2C serial interface is active.

The P12VOA, P5VISA and P3VISA pins monitor the load for an undervoltage fault once the +12-V, +5-V and +3.3-V switches are fully enhanced. The +12-V, +5-V, +3.3-V and −12-V load currents are monitored for an overload condition continuously upon slot enable. The device overtemperature sensor is always active, cannot be masked with the test mode fault mask, and shuts down all switches upon sensing excessive internal die temperature.

The main load faults are latched and can be cleared by cycling the slot enable with the I^2C serial interface (if operating in serial mode), by transitioning slot enable from high to low (if operating in hardware enable mode), or by dropping and then raising power to the TPS2341.

The 3.3VAux standby switch requires only the 3VSTBYIN supply to be healthy before turning on. An overload condition shuts down the slot standby switch. The latched fault can be cleared by toggling the SWA (or SWB for slot B) input or by cycling the standby supply voltage.

The 3.3VAux main switch requires the main supply voltages to be within specifications before turning on. The slot 3.3VAux main switch shuts off upon an overload condition and all switches shut off upon the device over temperature condition. The latched fault can be cleared by cycling the SWA (or SWB for slot B) 3.3VAux disable pin or removal and assertion of input supply voltage.

The I^2C serial interface can be used to determine the offending fault. Polling the STATUS READ register determines which slot caused the fault and differentiates between the main supply switches or the 3.3VAux switches. The slot STATUS register indicates an undervoltage fault, thermal shutdown, overload fault or commanded disable occurred. The OVERLOAD register isolates an overload condition to the individual supply switch.

Operation Without I^2C

The TPS2341 can be used in a system without I^2C, although some of the diagnostic capabilities of the TPS2341 are lost. Slot main power is applied by applying a rising edge to the PGOOD input and then applying a rising edge to the appropriate slot enable input ENx. Slot main power status is observed at the PGOOD_OUTx output.

In the event of a loss of power on any main input, the TPS2341 resets to all slots off. Main slot power restarts on the next rising edge of ENx after power is recovered.

In a system without I^2C, the interrupt output IRQ# is not meaningful and should not be connected. SDA should be pulled up to 3.3 V. SCL and ADDR1 should be grounded.

APPLICATION INFORMATION

Interrupt Service Request

The TPS2341 generates an interrupt by asserting the IRQ# output. Any of the following conditions causes an interrupt:

- The SWx input changes state.
- An auxiliary or main output over-current fault occurs.
- A main input/output under-voltage condition occurs.
- Thermal shutdown of the TPS2341 occurs.

The status registers (see Table 1) can be read to determine the cause of the interrupt and to identify the slot causing the interrupt.

Slot level control of an interrupt is possible through the interrupt mask in register 00h. For example, setting mask bits zero and two to logic 1 and logic 0, respectively, enables a slot A interrupt but disables a slot B interrupt. These mask bits only affect the IRQ# output pin, the internal IRQ bits in register 10h still acknowledge the fault.

Resetting the Interrupt

A SWx input state change causes an interrupt that is cleared by setting bit 4 (SW interrupt reset) of register 00h to logic 1. This bit must then be set to logic 0 to rearm the interrupt.

An interrupt that is caused by an overload on the auxiliary channel will be cleared along with the fault when the SWx input pin is brought high (disable) or the PGOOD input pin is brought low.

An interrupt that is caused by an overload on the main channel or a main input/output undervoltage condition will be cleared along with the fault when the ENx input pin is brought low and the ENx bit in register 00h is brought low. This interrupt is also cleared when the PGOOD input is brought low.

I^2C Operation

The TPS2341 communicates with the master controller using the I^2C serial protocol. The SCL pin, which is the clock, and the SDA pin, which is the bi-directional data, are used for transferring data to and from the device. The TPS2341 implements a 7-bit addressing scheme with the upper six bits internally defined 010000 and the least significant bit user programmable with the ADDR1 pin.

The data protocol recognizes a START pulse as a high-to-low transition on the SDA pin when the SCL pin is high. The rising edge of the SCL pin clocks a logic-high into (or out of) the device when SDA is high and a logic-low when the SDA pin is low. An ACKNOWLEDGE handshake occurs as the device receiving the 8-bit word pulls the SDA pin low when the SCL pin is clocked the ninth time. Another 8-bit word followed by an ACKNOWLEDGE bit can immediately begin depending upon the read or write cycle protocol.

The write cycle protocol begins with a START bit, contains three 8-bit words, each followed by an ACKNOWLEDGE bit and ends with a STOP bit. The first 8-bit word is the device address which must match the internally defined upper 6 bits and externally defined least significant bit with a low LSB (A0) to indicate a write cycle. Following a good device address word, the second 8-bit word selects the internal register that the control device would like to place data into. The third 8-bit word is the actual data to be placed into the selected registers.

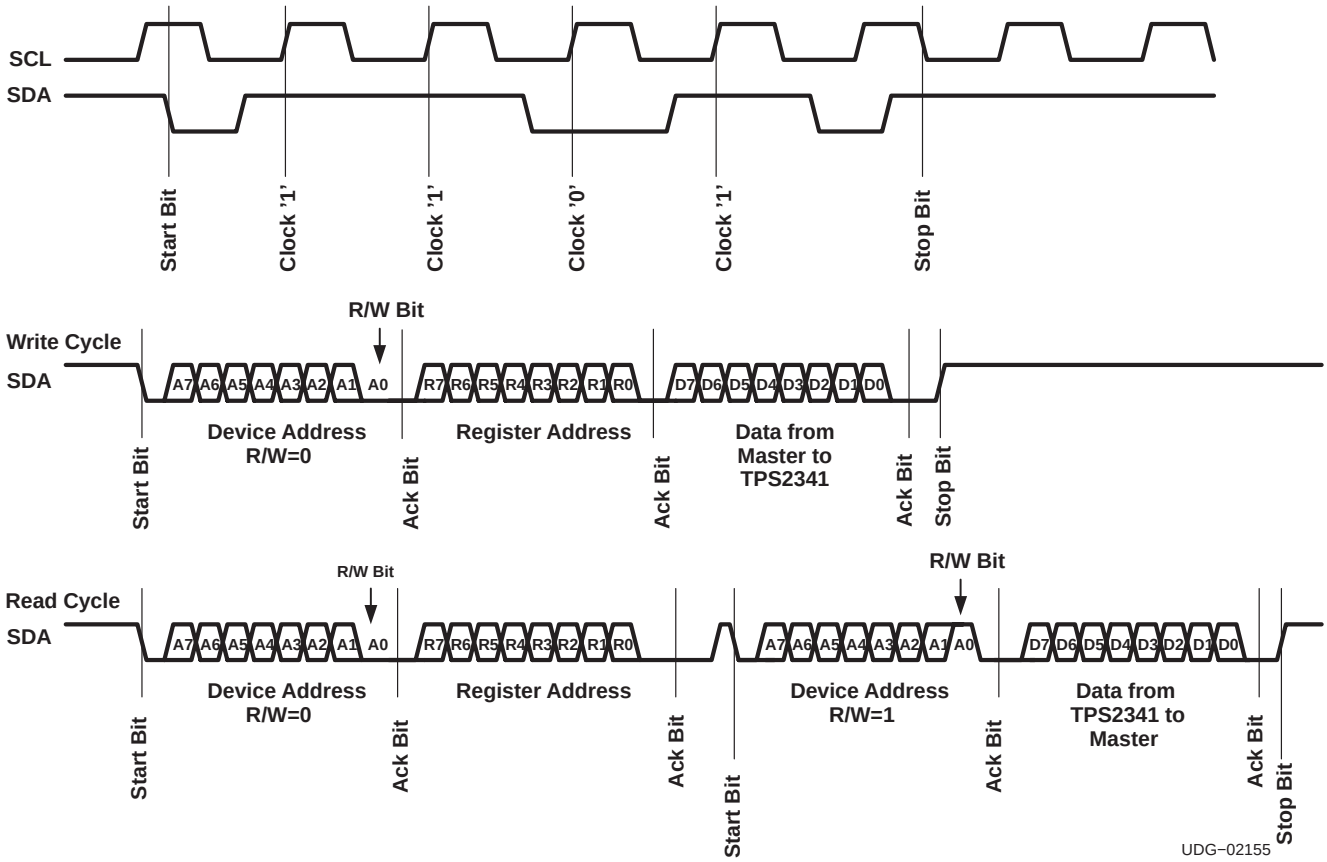


Figure 10. I²C Signal Timing

APPLICATION INFORMATION

I²C Operation (continued)

The read cycle protocol begins with a START bit, followed by two 8-bit words, another START bit, another two 8-bit words and ends with a STOP bit. The first two 8-bit words are similar to the write cycle, with a low LSB for the device address, and instruct the device which internal register will be polled. A START bit after the second word interrupts the write cycle after the internal register is defined. The next 8-bit word following the second START bit is once again the device address, however, the LSB (A0) is now high indicating the device is expected to return the data from the selected internal register. After the ACKNOWLEDGE bit, the TPS2341 drives the SDA line and return the 8-bits of data from the internal register.

Table 1. Register DefinitionS

REGISTER	ASSIGNMENT	BIT	READ/ WRITE	DEFINITION
00h	Control Write	0	W	Slot A Int_Mask 1: Allow Slot A interrupts to set IRQ# active 0: Mask Slot A interrupts on IRQ#
		1		Slot A Enable 1: Enable Slot A main switches 0: Disable Slot A main switches
		2		Slot B Int_Mask 1: Allow Slot B interrupts to set IRQ# active 0: Mask Slot B interrupts on IRQ#
		3		Slot B Enable 1: Enable Slot B main switches 0: Disable Slot B main switches
		4		SW Interrupt Reset 1: Reset interrupt request from SWA or SWB edge transition 0: Clear reset
		5		Spare a; data stored here is visible on read 11h, bit 5
		6		Spare b; data stored here is visible on read 11h, bit 6
		7		Spare c; data stored here is visible on read 11h, bit 7
10h	Status Read	0	R	Slot A PGood 1: Slot A main switches active and healthy 0: Slot A main switches not healthy
		1		Slot A Aux_Good 1: Slot A 3.3-V Aux main active and healthy 0: Slot A 3.3-V Aux not healthy
		2		Slot A IRQ 1: Slot A interrupt request active 0: Slot A interrupt request inactive
		3		Slot B PGood 1: Slot B main switches active and healthy 0: Slot B main switches not healthy
		4		Slot B Aux_Good 1: Slot B 3.3-V Aux main active and healthy 0: Slot B 3.3-V Aux not healthy
		5		Slot B IRQ 1: Slot B interrupt request active 0: Slot B interrupt request inactive
		6		PGOOD_INPUT 1: PGOOD input pin is high 0: PGOOD input pin is low
		7		0

APPLICATION INFORMATION

Table 1. Register Definitions (continued)

11h	Control Read	0	R	Slot A Int_Mask 1: Slot A allows interrupts to set IRQ# active 0: Slot A masks interrupts on IRQ#
		1		Slot A Enable 1: Slot A main switches enable active 0: Slot A main switches enable inactive
		2		Slot B Int_Mask 1: Slot B allows interrupts to set IRQ# active 0: Slot B masks interrupts on IRQ#
		3		Slot B Enable 1: Slot B main switches enable active 0: Slot B main switches enable inactive
		4		SW Interrupt Reset 1: Reset Interrupt request from SWA or SWB edge transition 0: Clear reset
		5		Spare a; Data stored from write 00h, bit 5
		6		Spare b; Data stored from write 00h, bit 6
		7		Spare c; Data stored from write 00h, bit 7
12h	Slot A Status	0	R	Slot A enable 1: Slot A main switches enable active 0: Slot A main switches enable inactive
		1		Input undervoltage fault 1: Input undervoltage fault active 0: Input undervoltage fault inactive
		2		Slot A output undervoltage fault 1: Slot A output undervoltage fault active 0: Slot A output undervoltage fault inactive
		3		Slot A overload fault 1: Slot A overload fault active 0: Slot A overload fault inactive
		4		Thermal shutdown fault 1: Thermal shutdown fault active 0: Thermal shutdown fault inactive
		5		SWA input 1: SWA input active; after rising edge delay 0: SWA input inactive; no falling edge delay
		6		Slot A PGOOD 1: Slot A main switches active and healthy 0: Slot A main switches not healthy
		7		Slot A Main Fault 1: Slot A main fault active 0: Slot A main fault inactive

APPLICATION INFORMATION

Table 1. Register Definitions (continued)

REGISTER	ASSIGNMENT	BIT	READ/ WRITE	DEFINITION
13h	Slot A Overload	0	R	Slot A +3V Overload 1: Slot A +3.3-V overload active 0: Slot A +3.3-V overload inactive
		1		Slot A +5V Overload 1: Slot A +5-V overload active 0: Slot A +5-V overload inactive
		2		Slot A +12-V Overload 1: Slot A +12-V overload active 0: Slot A +12-V overload inactive
		3		Slot A −12-V Overload 1: Slot A −12-V overload active 0: Slot A −12-V overload inactive
		4		Slot A 3VSTBYIN Overload 1: Slot A 3.3-VAux standby overload active 0: Slot A 3.3-VAux standby overload inactive
		5		Slot A 3VMAIN overload 1: Slot A 3.3-VAux main overload active 0: Slot A 3.3-VAux main overload inactive
		6		Slot A 3VAUX standby switch on 1: Slot A 3.3-VAux standby switch active 0: Slot A 3.3-Vaux standby switch inactive
		7		Slot A 3VAUX main switch on 1: Slot A 3.3VAux main switch active 0: Slot A 3.3VAux main switch inactive
14h	Slot B Status	0	R	Slot B enable 1: Slot B main switches enable active 0: Slot B main switches enable inactive
		1		Input undervoltage fault 1: Input undervoltage fault active 0: Input undervoltage fault inactive
		2		Slot B output undervoltage fault 1: Slot B output undervoltage fault active 0: Slot B output undervoltage fault inactive
		3		Slot B overload fault 1: Slot B overload fault active 0: Slot B overload fault inactive
		4		Thermal shutdown fault 1: Thermal shutdown fault active 0: Thermal shutdown fault inactive
		5		SWA input 1: SWA input active; after rising edge delay 0: SWA input inactive; no falling edge delay
		6		Slot B PGOOD 1: Slot B main switches active and healthy 0: Slot B main switches not healthy
		7		Slot B Main Fault 1: Slot B main fault active 0: Slot B main fault inactive

APPLICATION INFORMATION

Table 1. Register Definitions (continued)

15h	Slot B Overload	0	R	Slot B +3V Overload 1: Slot B +3.3-V overload active 0: Slot B +3.3-V overload inactive
		1		Slot B +5V Overload 1: Slot B +5-V overload active 0: Slot B +5-V overload inactive
		2		Slot B +12-V Overload 1: Slot B +12-V overload active 0: Slot B +12-V overload inactive
		3		Slot B −12-V Overload 1: Slot B −12-V overload active 0: Slot B −12-V overload inactive
		4		Slot B 3VSTBYIN Overload 1: Slot B 3.3-VAux standby overload active 0: Slot B 3.3-VAux standby overload inactive
		5		Slot B 3VMAIN overload 1: Slot B 3.3-VAux main overload active 0: Slot B 3.3-VAux main overload inactive
		6		Slot B 3VAUX standby switch on 1: Slot B 3.3-VAux standby switch active 0: Slot B 3.3-Vaux standby switch inactive
		7		Slot B 3VAUX main switch on 1: Slot B 3.3VAux main switch active 0: Slot B 3.3VAux main switch inactive

APPLICATION INFORMATION

Test Mode Functions for Address Bit

The TPS2341 address pin (ADDR1) provides two functions. The input provides the I2C serial interface with a unique address when two TPS2341 devices share the same address bank and also provides a means of disabling faults. Three different voltage levels are used to define the status of the input signal. Upon pulling the address pin low, the serial interface address bit is set low. The serial interface address bit is set high if the address pin is allowed to float or is driven to one-half the voltage at DIGVCC. Upon pulling ADDR1 to DIGVCC the internal test mode is invoked which masks the overload and undervoltage faults and does not shut down the slots when the thresholds are exceeded. This is intended to be used for board development only to avoid nuisance faults from improperly sized bulk capacitance or excessive switching loads. Caution must be taken to never exceed the maximum dissipation or absolute maximum conditions of the device while the device self-protection is disabled.

Table 2. I2C Device Address Decode

BIT	DEFINITION
A0	R/W bit 0: Write data from master to TPS2341 1: Read data from TPS2341 to master
A1	Device address bit 1 (LSB) compared with pin ADDR1
A2	0 internally defined
A3	0 internally defined
A4	0 internally defined
A5	0 internally defined
A6	1 internally defined
A7	0 internally defined

Table 3. Test Mode Functions for Adddress Bits

BIT	VOLTAGE LEVEL (V)	ADDRESS FUNCTION	TEST MODE FUNCTION
A1	< 0.8	Low	OFF
	0.8 < V_{A1} < 2.5	High	OFF
	> 2.5	High	Mask fault active

APPLICATION INFORMATION

Layout Considerations

It is important to use good layout practices regarding device placement and etch routing of the backplane/system board to optimize the performance of the hot plug circuit. Some of the key considerations are listed here:

- Decoupling capacitors should be located close to the device.
- Any protection devices (e.g. zener clamps) should be located close to the device.
- To reduce insertion loss across the hot plug interface, use wide traces for the supply and return current paths. A power plane can be used for the supply return or PWRGND nodes.
- Additional copper placed at the land patterns of the sense resistors and pass FETs can significantly reduce the thermal impedance of these devices, reducing temperature rise in the module and improving overall reliability.
- Because typical values for current sense resistors can be very low (6 mΩ typical), board trace resistance between elements in the supply current paths becomes significant. To achieve maximum accuracy of the overload thresholds, good Kelvin connections to the resistors should be used for the current sense inputs to the device. The current sense traces should connect symmetrically to the sense resistor land pattern, in close proximity to the element leads, not upstream or downstream from the device.
- For best noise immunity, provide separate ground planes for the analog, digital, and power circuitry. These ground planes should tie together at a single point in the system.

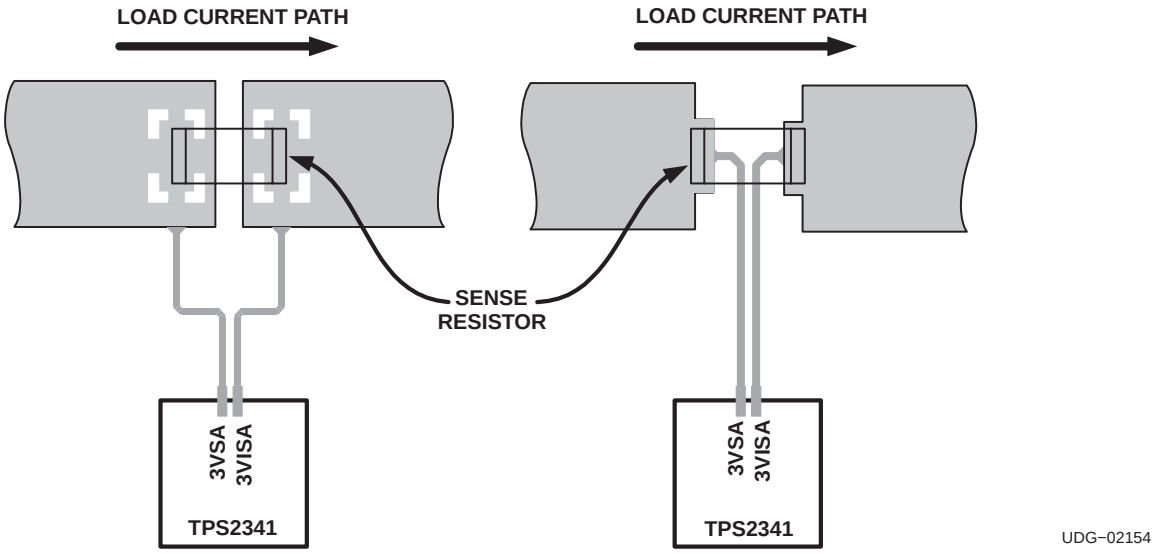


Figure 11. Connecting the Sense Resistors

These recommended layouts provide force-and-sense (Kelvin) connection to the current sense resistor to minimize circuit board trace resistance.

APPLICATION INFORMATION

Thermal Model

The TPS2341 is packaged in the HTQFP-48 PowerPad™ quad flat-pack package. The PowerPad package is a thermally enhanced standard size device package designed to eliminate the use of bulky heatsinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard printed circuit board (PCB) assembly techniques, and can be removed and replaced using standard repair procedures.

The PowerPad package is designed so that the leadframe die pad is exposed on the bottom of the device. This provides an extremely low thermal resistance between the die and the thermal pad. The thermal pad can be soldered directly to the PCB for heatsinking. In addition, through the use of thermal vias, the thermal pad can be directly connected to a power/ground plane or special heat sink structure designed into the PCB. On the TPS2341, the die substrate is internally connected to the −12 V input supply. and therefore the power plane or heatsink connected to the thermal pad on the bottom of the device must also connect to the −12 V input supply (recommended) or float independent of any supply (acceptable).

The thermal performance can be modeled by determining the thermal resistance between the die and the ambient environment. Thermal resistances are measures of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the object's thermal resistance. Figure 12 illustrates the thermal path and resistances from the die, T_J through the printed circuit board to the ambient air.

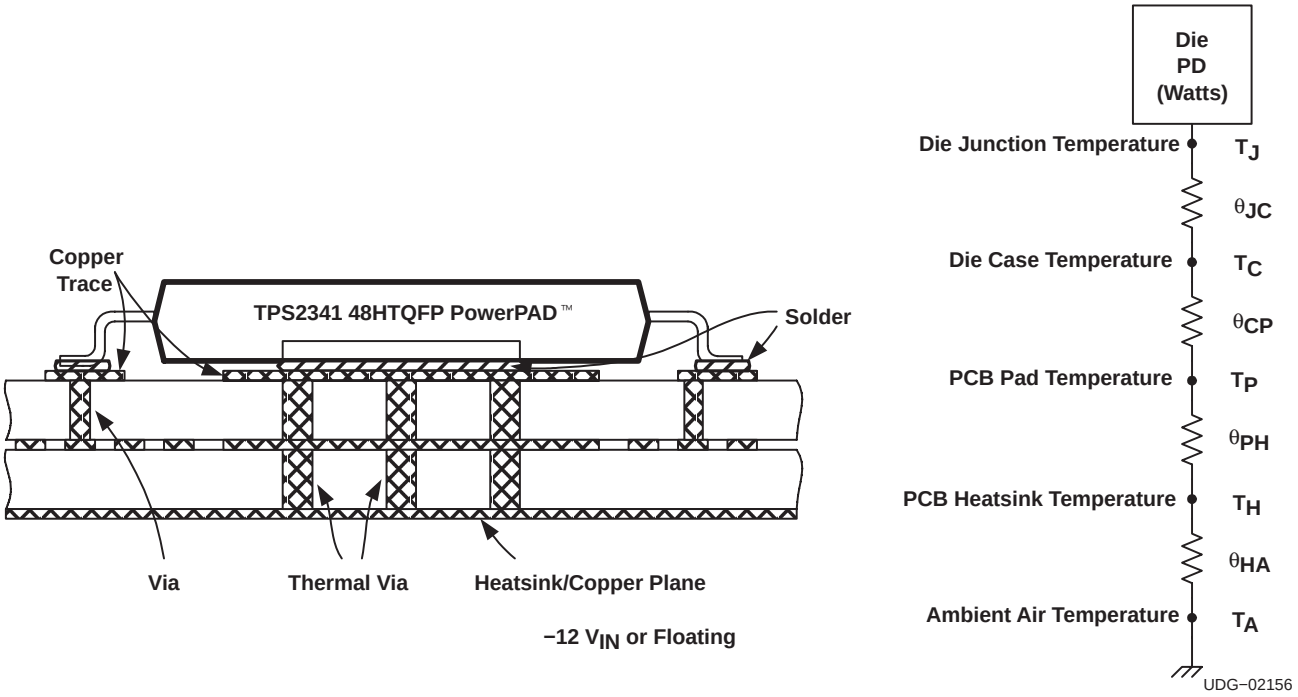


Figure 12. PowerPAD™ Thermal Model

Technical Brief *PowerPAD ™ Thermally Enhanced Package* (SLMA002) can be used as a guide to model the TPS2341 thermal resistance. The following example assumes the conditions as described in the technical brief. The TPS2341, mounted to a copper pad with solder on a PCB and two ounce traces, should exhibit a thermal resistance from junction temperature to ambient temperature of 29°C/W.

APPLICATION INFORMATION

Table 4. TPS2341 Continuous Maximum Load Power Consumption (All Drivers On)

SUPPLY DRIVER	$R_{DS(on)}$ (Ω)	POWER PER SLOT (W)	TOTAL POWER (W)
+12 V @ 0.5 A	0.5	0.1	0.2
−12 V @ 100 mA	0.9	0.01	0.02
+3VAux @ 375 mA	0.425	0.06	0.12
+12 V @ 3 mA		0.04	0.08
+5 V @1 mA			0.005
+3 V @ 0.5 mA			0.002
−12 V @ 0.25 mA		0.003	0.006
3VSTBY @ 0.2 mA			0.001
DIGVCC @ 0.2 mA			0.001
Total Power Consumption			0.435

$$T_{RISE} = P_{TOTAL} \times \theta_{JA} = (0.435\ W) \times (29\ deg\,C/W) \quad (1)$$

= 12.7 °C

$$T_J = T_A + T_{RISE} = 50°C + 12.7 \quad (2)$$

= 62.7°C

This example indicates that with the ambient air at 50°C the TPS2341 junction temperature rises to 63°C which is below the absolute maximum junction temperature of 85°C and ensures the device operates properly and within design specifications. The transient power consumption must also be considered for the conditions during initial ramp-up of the output supplies, however, this varies significantly depending upon output load impedance for each application and each supply.

Refer to Technical Briefs *PowerPAD ™Thermally Enhanced Package* (TI Literature No. SLMA003) and *PowerPAD ™ Made Easy* (TI Literature No. SLMA004) for more information.

APPLICATION INFORMATION

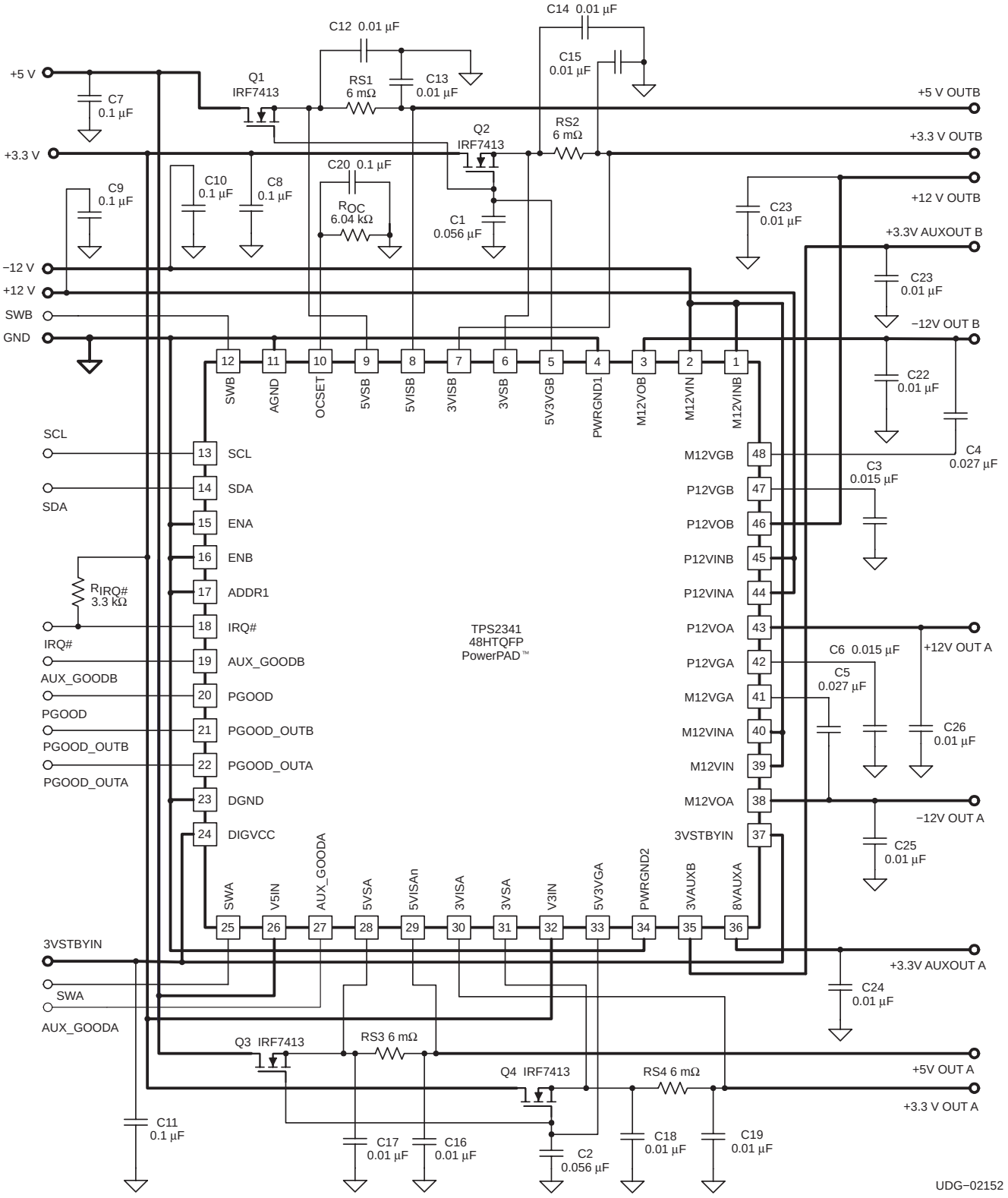


Figure 13. Typical Applications Diagram

Determining Component Values

Load Conditions

Table 5. Load Conditions for Determining Component Values

SUPPLY DRIVER	I_{LOAD} (A)	I_{TRAP} (A)	C_{LOAD} (μF)	SR (V/s)
+12 V	0.5	0.94	300	250
+5 V	5	7.0	3000	200
+3.3 V	7.6	10.0	3000	200
−12 V	0.1	0.19	150	200
+3.3 Vaux	0.375	1.0	150	5000
+3.3 Vaux(1)	0.02	0.04	150	100

(1) +3.3Vaux turn-on from stand-by power.

+3.3-V Supply

Overload Trip Point

Desired I_{TRIP} (nom) ≅ 10 A

$$R_{SENSE} = \frac{V_{RTRIP\ (nom)}}{I_{TRIP\ (nom)}} = \frac{52\ mV}{10\ A} = 0.0052\ \Omega \quad \therefore \text{Choose 5 m}\Omega,\ 2\%\ \text{sense resistor} \tag{3}$$

$$I_{TRIP(min)} = \frac{V_{TRIP\ (min)}}{R_{SENSE\ (max)}} = \frac{44\ mV}{5.1\ m\Omega} = 8.63\ A \tag{4}$$

$$I_{TRIP(max)} = \frac{V_{TRIP\ (max)}}{R_{SENSE\ (min)}} = \frac{60\ mV}{4.9\ m\Omega} = 12.2\ A \tag{5}$$

Gate Capacitance

$I_{INRUSH} \leq 8.6\ A$

$I_{CLOAD} = I_{INRUSH} - I_{LOAD} = 8.6\ A - 7.6\ A = 1\ A$

from i = C dV/dt for the load capacitance and charge current: $\Delta T = \Delta V\ (C/i)$

$$= 3.3\ V \times \left(\frac{3000\ \mu F}{1\ A}\right) = 9.9\ ms \tag{6}$$

from i = C dV/dt for the gate capacitance and charge current: $C = i \times (\Delta T/\Delta V)$

$$= 25\ \mu A \left(\frac{9.9\ ms}{3.3\ V}\right) \text{ using the maximum gate capacitance and charge current} \tag{7}$$

$= 0.075\ \mu F \therefore$ choose 0.1 μF, 10% capacitor.

The nominal load turn-on time is calculated in equation (8).

$$\Delta T = \Delta V\ (C/i) = 3.3\ V \times \left(\frac{0.1\ \mu F}{20\ \mu A}\right) = 16.5\ ms \tag{8}$$

$$SR = \frac{3.3\ V}{16.5\ ms} = 200\ V/s \tag{9}$$

APPLICATION INFORMATION

+5-V Supply

Overload Trip Point

Desired I_{TRIP} (nom) ≅ 7 A

$$R_{SENSE} = \frac{V_{RTRIP\ (nom)}}{I_{TRIP\ (nom)}} = \frac{42\ mV}{7\ A} = 0.006\ \Omega \quad \therefore \text{Choose 6 m}\Omega,\ 2\%\ \text{sense resistor.} \tag{10}$$

$$I_{TRIP(min)} = \frac{V_{TRIP\ (min)}}{R_{SENSE\ (max)}} = \frac{35\ mV}{6.12\ m\Omega} = 5.72\ A \tag{11}$$

$$I_{TRIP(max)} = \frac{V_{TRIP\ (max)}}{R_{SENSE\ (min)}} = \frac{48\ mV}{5.88\ m\Omega} = 8.16\ A \tag{12}$$

Gate Capacitance

$I_{INRUSH} \leq 5.72$ A

$I_{CLOAD} = I_{INRUSH} - I_{LOAD} = 5.72\ A - 5\ A = 720$ mA

from the chosen gate capacitance (shared with the 3.3-V MOSFET).

$$I_{CLOAD} = C \times (\Delta V/\Delta T) = 3000\ \mu F \times (200V/s) = 600\ mA\ (max) \tag{13}$$

$I_{INRUSH} = I_{CLOAD} + I_{LOAD} = 600\ mA + 5\ A = 5.6\ A$

The nominal load turn on time is calculated in equation (14).

$$\Delta T = \Delta V\ (C/i) = 5\ V \times \left(\frac{0.1\ \mu F}{20\ \mu A}\right) = 25\ ms \tag{14}$$

APPLICATION INFORMATION

+12-V Supply

Gate Capacitance

$I_{INRUSH} \leq 0.79$ A from a minimum +12-V overcurrent threshold voltage.

$I_{CLOAD} = I_{INRUSH} - I_{LOAD} = 0.79\ A - 0.5\ A = 290\ mA$

from i = C dV/dt for the load capacitance and charge current: $\Delta T = \Delta V\ (C/i)$

$$= 12\ V \times \left(\frac{300\ \mu F}{290\ mA}\right) = 12.4\ ms \quad (15)$$

from i = C dV/dt for the gate capacitance and charge current: $C = i \times (\Delta T/\Delta V)$

$$= 14\ \mu A \left(\frac{12.4\ ms}{12\ V}\right) \text{ using the maximum gate capacitance and charge current} \quad (16)$$

$= 0.014\ \mu F \therefore$ choose 0.02 μF, 10% capacitor.

The nominal load turn-on time is calculated in equation (17).

$$\Delta T = \Delta V\ (C/i) = 12\ V \times \left(\frac{0.02\ \mu F}{5\ \mu A}\right) = 48\ ms \quad (17)$$

$$SR = \frac{12\ V}{48\ ms} = 250\ V/s \quad (18)$$

−12-V Supply

Gate Capacitance

$I_{INRUSH} \leq 150$ mA from minimum −12-V overcurrent threshold voltage.

$I_{CLOAD} = I_{INRUSH} - I_{LOAD} = 150\ mA - 100\ mA = 50\ mA$

from i = C dV/dt for the load capacitance and charge current: $\Delta T = \Delta V\ (C/i)$

$$= 12\ V \times \left(\frac{150\ \mu F}{50\ mA}\right) = 36\ ms \quad (19)$$

from i = C dV/dt for the gate capacitance and charge current: $C = i \times (\Delta T/\Delta V)$

$$= 25\ \mu A \left(\frac{36\ ms}{12\ V}\right) \text{ using the maximum gate capacitance and charge current} \quad (20)$$

$= 0.075\ \mu F \therefore$ choose 0.1 μF, 10% capacitor.

The nominal load turn-on time is calculated in equation (21).

$$\Delta T = \Delta V\ (C/i) = 12\ V \times \left(\frac{0.1\ \mu F}{20\ \mu A}\right) = 60\ ms \quad (21)$$

$$SR = \frac{12\ V}{60\ ms} = 200\ V/s \quad (22)$$

APPLICATION INFORMATION

+3.3-V Auxiliary Supply

Inrush Current

I_{INRUSH} = C dV/dt + I_{LOAD} for the load capacitance

$$= 150\ \mu F \left(\frac{5\ V}{1\ ms}\right) + 375\ mA = 1125\ mA \quad (23)$$

The nominal load turn-on time is calculated in equation (24).

$$T = \frac{\Delta V}{\left(\frac{dV}{dt}\right)} = \frac{3.3\ V}{\left(\frac{5\ V}{1\ ms}\right)} = 660\ \mu s \quad (24)$$

Standby Inrush Current

I_{INRUSH} = C dV/dt + I_{LOAD} for the load capacitance

$$= 150\ \mu F \left(\frac{0.1\ V}{1\ ms}\right) + 20\ mA = 35\ mA \quad (25)$$

The nominal load turn-on time is calculated in equation (26).

$$T = \frac{\Delta V}{\left(\frac{dV}{dt}\right)} = \frac{3.3\ V}{\left(\frac{0.1\ V}{1\ ms}\right)} = 33\ ms \quad (26)$$

Thermal Shutdown

Under normal operating consitions, the power dissipation in the TS2341 is low enough that the junction temperature (T_J) is not more than 15°C above air temperature (T_A). However, in the case of a load that exceeds PCI specifications (but remains under the TPS2341 overcurrent threshold) power dissipation can be higher. To prevent any damage from an out-of-specification load or severe rise in ambient temperature, the TPS2341 contains two independent thermal shutdown circuits, one for each main supply slot.

The highest power dissipation in the TPS2341 is from the 12-V power FET so that TPS2341 temperature sense elements are integrated closely with these FETs. These sensors indicate when the temperature at these transistors exceeds approximately 150°C, due either to average device power dissipation, 12-V power FET power dissipation, or a combination of both.

When excessive junction temperature is detected in one slot, that slot's fault latch is set and remains set until the junction temperature drops by approximately 10°C and the slot is then restarted through the serial interface or supply dropping. The other slot is not affected by this event.

Digital Circuits

The I^2C serial interface is available once DIGVCC is stable. However, data in the main power registers is accurate only if the main supply voltages are within specification. Data in the AUXFAULTx register is accurate only if the 3VSTBYIN supply voltage is within specifications.

PACKAGING INFORMATION

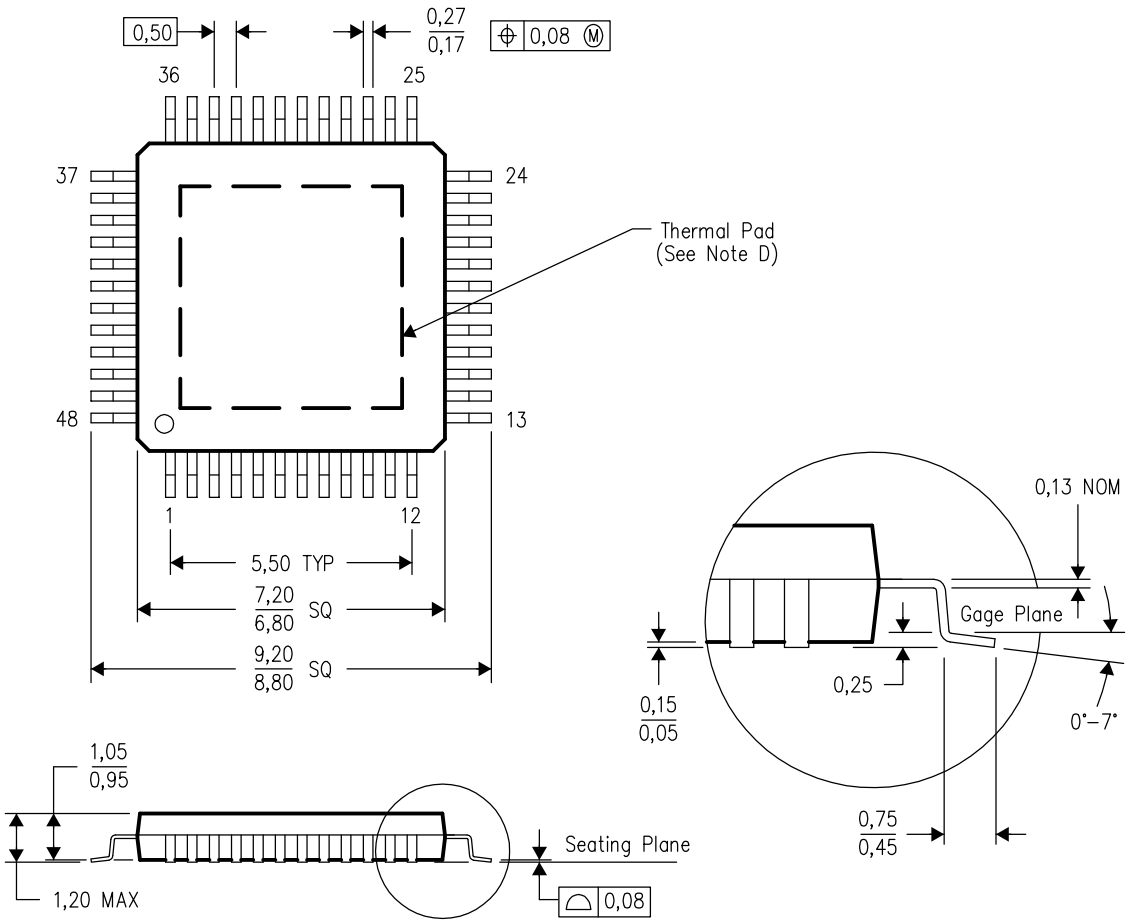
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS2341PHP	ACTIVE	HTQFP	PHP	48	250	None	CU NIPDAU	Level-3-220C-168 HR
TPS2341PHPR	ACTIVE	HTQFP	PHP	48	1000	None	CU NIPDAU	Level-3-220C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

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