

TOSHIBA Bi- CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

## TB62706BNG, TB62706BFG

16BIT SHIFT REGISTER, LATCHES & CONSTANT CURRENT DRIVERS

The TB62706BNG, TB62706BFG are specifically designed for LED and LED DISPLAY constant current drivers.

This constant current output circuits are able to set up external resistor ( $I_{OUT} = 5\text{--}90\text{ mA}$ ). (Note)

These devices are monolithic integrated circuit designed to be used together with Bi- CMOS process.

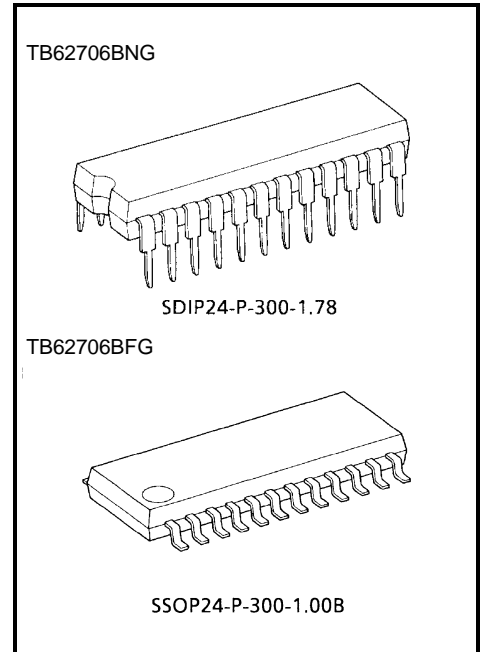
The devices consist of 16bit shift register, latch, AND- GATE and Constant Current Drivers.

These products are Pb free.

### FEATURES

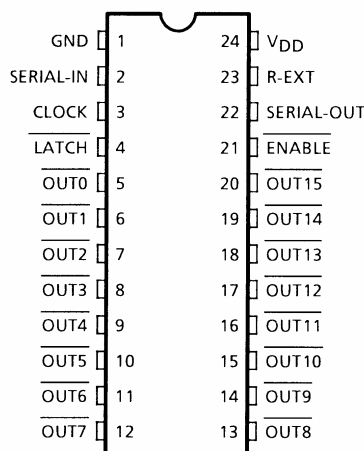
- Constant Current Output : Can set up all output current with one resistor for 5 to 90 mA.
- Maximum Clock Frequency :  $f_{CLK} = 15\text{ (MHz)}$  (Cascade Connected Operate,  $T_{opr} = 25^{\circ}\text{C}$ )
- 5 V C- MOS Compatible Input
- Package: SDIP24- P- 300- 1.78 (TB62706BNG)  
SSOP24- P- 300- 1.00B (TB62706BFG)
- Constant Output Current Matching:

OUTPUT- GND VOLTAGE	CURRENT MATCHING	OUTPUT CURRENT
$\approx 0.4\text{ V}$	$\pm 6.0\%$	5~40 mA
$\approx 0.7\text{ V}$	$\pm 6.0\%$	5~90 mA

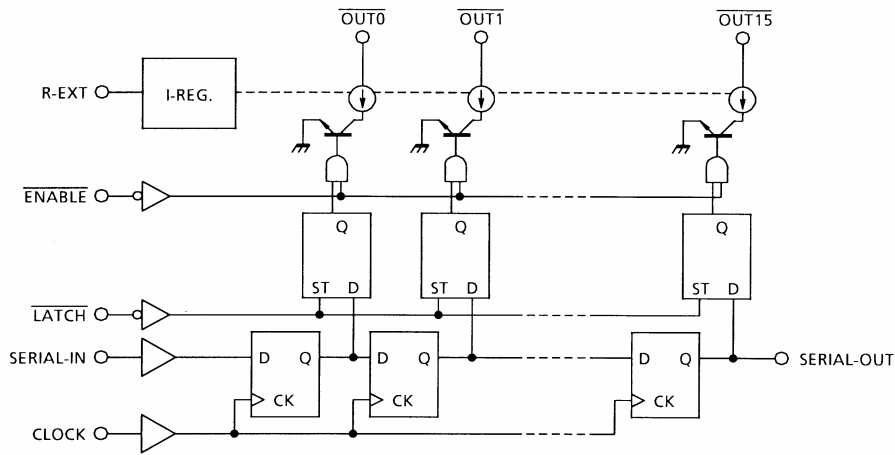


Weight  
 SDIP24-P-300-1.78 : 1.22 g (typ.)  
 SSOP24-P-300-1.00B : 0.32 g (typ.)

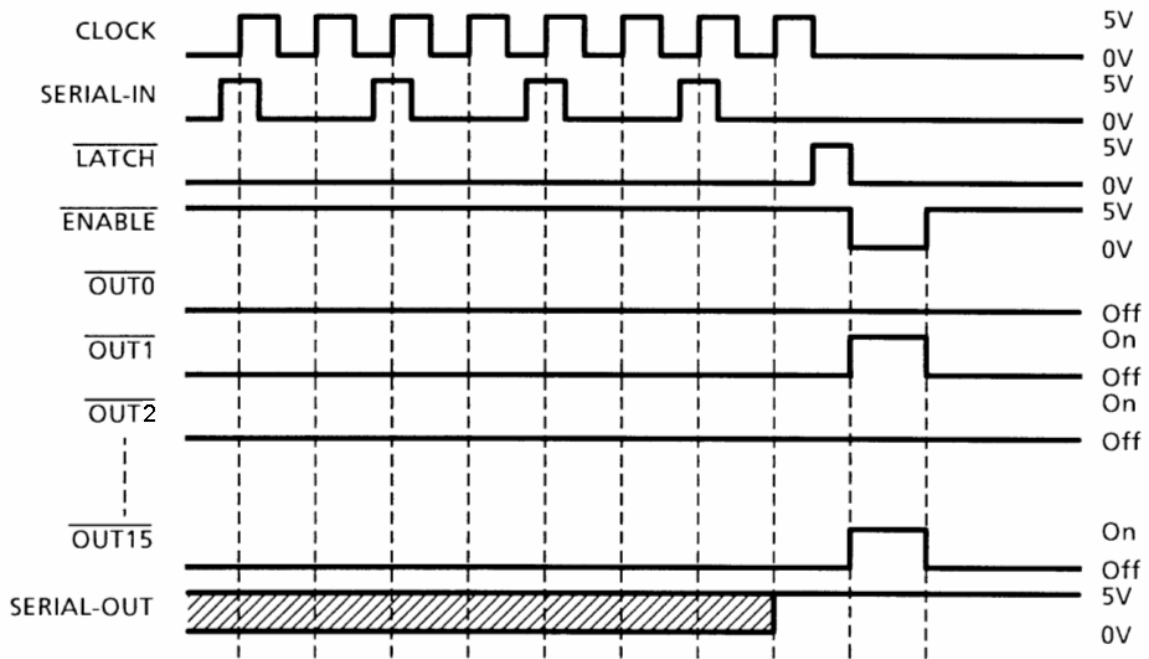
### PIN CONNECTION (Top view)



**BLOCK DIAGRAM**



**TIMING DIAGRAM**



Note: Latches are level sensitive, not rising edges sensitive and not synchronous CLOCK.  
 Input of LATCH- terminal to H Level, data passes latches, and input to L level, data hold latches.  
 Input of ENABLE- terminal to H level, all output (OUT0~15) do off.

## TERMINAL DISCRPTION

PIN No.	PIN NAME	FUNCTION
1	GND	GND terminal for control logic.
2	SERIAL- IN	Input terminal of a serial- data for shift- register.
3	CLOCK	Input terminal of a clock for data shift to up- edge.
4	$\overline{\text{LATCH}}$	Input terminal of a data strobe. Latches passes data with "H" level input of LATCH - terminal, and hold data with "L" level input.
5~20	$\overline{\text{OUT0}} \sim \overline{\text{15}}$	Output terminals.
21	$\overline{\text{ENABLE}}$	Input terminal of output enable. All outputs ( $\overline{\text{OUT0}} \sim \overline{\text{15}}$ ) do off with "H" level input of ENABLE - terminal, and do on with "L" level input.
22	SERIAL- OUT	Output terminal of a serial- data for next SERIAL- IN terminal.
23	R- EXT	Input terminal of connects with a resistor for to set up all output current.
24	V <sub>DD</sub>	5 V Supply voltage terminal.

## TRUTH TABLE

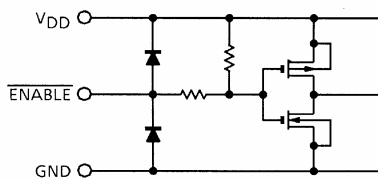
CLOCK	$\overline{\text{LATCH}}$	$\overline{\text{ENABLE}}$	SERIAL- IN	$\overline{\text{OUT0}} \dots \overline{\text{OUT7}} \dots \overline{\text{OUT15}}$	SERIAL- OUT
UP	H	L	D <sub>n</sub>	D <sub>n</sub> ... D <sub>n-7</sub> ... D <sub>n-15</sub>	D <sub>n-15</sub>
UP	L	L	D <sub>n+1</sub>	No change	D <sub>n-14</sub>
UP	H	L	D <sub>n+2</sub>	D <sub>n+2</sub> ... D <sub>n-5</sub> ... D <sub>n-13</sub>	D <sub>n-13</sub>
DOWN	X	L	D <sub>n+3</sub>	D <sub>n+2</sub> ... D <sub>n-5</sub> ... D <sub>n-13</sub>	D <sub>n-13</sub>
DOWN	X	H	D <sub>n+3</sub>	Off	D <sub>n-13</sub>

Note:  $\overline{\text{OUT0}} \sim \overline{\text{15}}$  = on in case of D<sub>n</sub> = H level and  $\overline{\text{OUT0}} \sim \overline{\text{15}}$  = off in case of D<sub>n</sub> = L level.

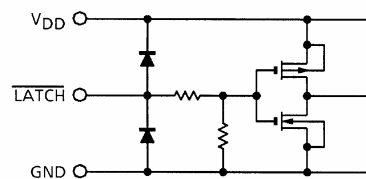
A resistor is connected with R- EXT and GND accompanied with outside, and it is necessary that a correct power supply voltage is supplied.

## EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

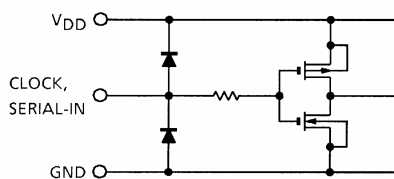
### 1. $\overline{\text{ENABLE}}$ terminal



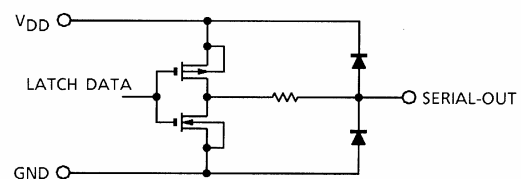
### 2. $\overline{\text{LATCH}}$ terminal



### 3. CLOCK, SERIAL- IN terminal



### 4. SERIAL- OUT terminal



## MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>DD</sub>	0~7.0	V
Input Voltage	V <sub>IN</sub>	- 0.4~V <sub>DD</sub> + 0.4	V
Output Current	I <sub>OUT</sub>	90	mA
Output Voltage	V <sub>OUT</sub>	- 0.5~17.0	V
Clock Frequency	f <sub>CK</sub>	15	MHz
GND Terminal Current	I <sub>GND</sub>	1440	mA
Power Dissipation	P <sub>D</sub>	1.78 (BNG- type : ON PCB, Ta = 25°C )	W
		1.00 (BFG- type : ON PCB, Ta = 25°C )	
Thermal Resistance	R <sub>th (j- a)</sub>	BNG : 70 (BN- type : ON PCB)	°C / W
		BFG : 120 (BF- type : ON PCB)	
Operating Temperature	T <sub>opr</sub>	- 40~85	°C
Storage Temperature	T <sub>stg</sub>	- 55~150	°C

Note: BN- type : Ambient temperature delated above 25°C in the proportion of 14.2 mW / °C

BF- type : Ambient temperature delated above 25°C in the proportion of 8.3 mW / °C

## RECOMMENDED OPERATING CONDITION (Ta = - 40~85°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage	V <sub>DD</sub>	-	4.5	5.0	5.5	V
Output Voltage	V <sub>OUT</sub>	-	-	-	15.0	V
Output Current	I <sub>O</sub>	OUTn, DC 1 circuit	5	-	88	mA
	I <sub>OH</sub>	SERIAL- OUT	-	-	1.0	
	I <sub>OL</sub>	SERIAL- OUT	-	-	- 1.0	
Input Voltage	V <sub>IH</sub>	-	0.7 V <sub>DD</sub>	-	V <sub>DD</sub> +0.3	V
	V <sub>IL</sub>	-	- 0.3	-	0.3 V <sub>DD</sub>	
LATCH Pulse Width	t <sub>w</sub> LATCH	V <sub>DD</sub> = 4.5~5.5 V	100	-	-	ns
CLOCK Pulse Width	t <sub>w</sub> CLK		50	-	-	ns
ENABLE Pulse Width	t <sub>w</sub> EN		4500	-	-	ns
Set- Up Time for DATA	t <sub>setup</sub> (D)		60	-	-	ns
Hold Time for DATA	t <sub>hold</sub> (D)		20	-	-	ns
Set- Up Time for LATCH	t <sub>setup</sub> (L)		100	-	-	ns
Hold Time for LATCH	t <sub>hold</sub> (L)		60	-	-	ns
Clock Frequency	f <sub>CLK</sub>		Cascade operation	-	-	10.0
Power Dissipation	P <sub>D</sub>	Ta = 85°C (BNG- type)	-	-	0.92	W
		Ta = 85°C (BFG- type)	-	-	0.50	

## ELECTRICAL CHARACTERISTICS (V<sub>DD</sub> = 5.0 V, Ta = 25°C unless otherwise noted)

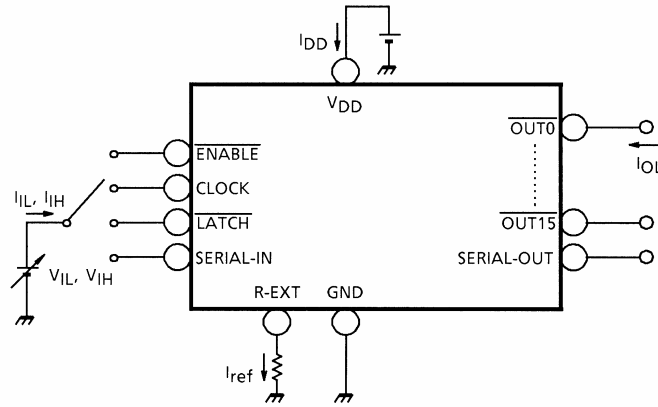
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	CONDITION	MIN	TYP.	MAX	UNIT	
Input Voltage	"H" Level	V <sub>IH</sub>	—	Ta = - 40~85°C	0.7 V <sub>DD</sub>	—	V <sub>DD</sub>	V	
	"L" Level	V <sub>IL</sub>	—	Ta = - 40~85°C	GND	—	0.3 V <sub>DD</sub>		
Output Leakage Current		I <sub>OH</sub>	—	V <sub>OH</sub> = 15.0 V	—	—	10	μA	
Output Voltage	SERIAL- OUT	V <sub>OL</sub>	—	I <sub>OL</sub> = 1.0 mA	—	—	0.4	V	
		V <sub>OH</sub>	—	I <sub>OH</sub> = - 1.0 mA	4.6	—	—		
Output Current 1		I <sub>OL1</sub>	—	V <sub>CE</sub> = 0.7 V	R <sub>EXT</sub> = 470 Ω (Include current matching)	34.1	40.0	45.9	mA
		I <sub>OL2</sub>	—	V <sub>CE</sub> = 0.4 V		33.7	39.5	45.3	
	Current Skew	D I <sub>OL1</sub>	—	I <sub>O</sub> = 40 mA, V <sub>CE</sub> = 0.4 V	R <sub>EXT</sub> = 470 Ω	—	±1.5	±6.0	%
Output Current 2		I <sub>OL3</sub>	—	V <sub>CE</sub> = 1.0 V	R <sub>EXT</sub> = 250 Ω (Include current matching)	64.2	75.5	86.8	mA
		I <sub>OL4</sub>	—	V <sub>CE</sub> = 0.7 V		63.8	75.0	86.2	
	Current Skew	D I <sub>OL2</sub>	—	I <sub>O</sub> = 75 mA, V <sub>CE</sub> = 0.7 V	R <sub>EXT</sub> = 250 Ω	—	±1.5	±6.0	%
Supply Voltage Regulation		% / V <sub>DD</sub>	—	R <sub>EXT</sub> = 470 Ω, Ta = - 40~85°C	—	1.5	5.0	% / V	
Pull- Up Resistor		R <sub>IN</sub> (up)	—	—	150	300	600	Ω	
Pull- Down Resistor		R <sub>IN</sub> (down)	—	—	100	200	400	Ω	
Supply Current	"OFF"	I <sub>DD</sub> (off) 1	—	R <sub>EXT</sub> = Open, OUT0 ~ 15 = off	—	0.6	1.2	mA	
		I <sub>DD</sub> (off) 2	—	R <sub>EXT</sub> = 470 Ω, $\overline{\text{OUT0}} \sim \overline{\text{15}} = \text{off}$	3.5	5.8	8.0		
		I <sub>DD</sub> (off) 3	—	R <sub>EXT</sub> = 250 Ω, $\overline{\text{OUT0}} \sim \overline{\text{15}} = \text{off}$	6.5	10.7	15.0		
	"ON"	I <sub>DD</sub> (on) 1	—	R <sub>EXT</sub> = 470 Ω, $\overline{\text{OUT0}} \sim \overline{\text{15}} = \text{on}$	10.0	16.0	22.0		
		I <sub>DD</sub> (on) 2	—	R <sub>EXT</sub> = 250 Ω, $\overline{\text{OUT0}} \sim \overline{\text{15}} = \text{on}$	18.0	28.3	38.5		

## SWITCHING CHARACTERISTICS (Ta = 25°C unless otherwise noted)

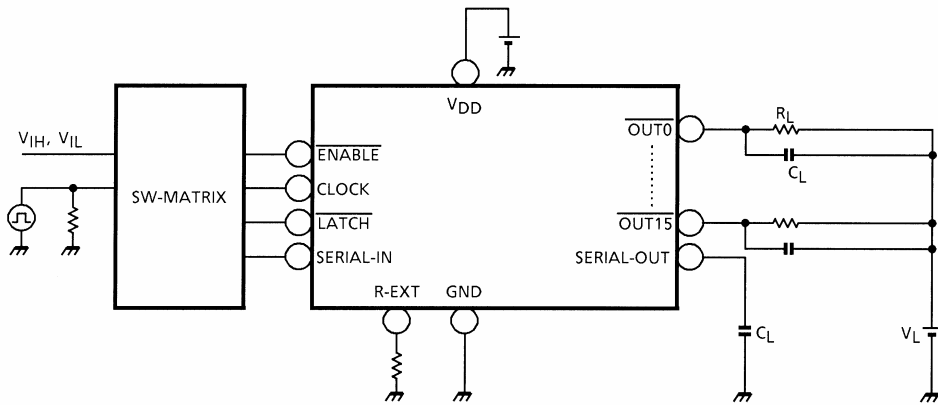
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	CONDITION	MIN	TYP	MAX	UNIT
Propagation Delay Time ("L" to "H")	CLK- $\overline{\text{OUTn}}$	$t_{\text{pLH}}$	-	$V_{\text{DD}} = 5.0 \text{ V}$ $V_{\text{CE}} = 0.4 \text{ V}$ $V_{\text{IH}} = V_{\text{DD}}$ $V_{\text{IL}} = \text{GND}$ $R_{\text{EXT}} = 470 \Omega$ $V_{\text{L}} = 3.0 \text{ V}$ $R_{\text{L}} = 65 \Omega$ $C_{\text{L}} = 10.5 \text{ pF}$	-	1200	1500	ns
	$\overline{\text{LATCH}} - \overline{\text{OUTn}}$				-	1200	1500	
	$\overline{\text{ENABLE}} - \overline{\text{OUTn}}$				-	1200	1500	
	CLK- SOUT				15	30	70	
Propagation Delay Time ("H" to "L")	CLK- $\overline{\text{OUTn}}$	$t_{\text{pHL}}$	-		-	700	1000	ns
	$\overline{\text{LATCH}} - \overline{\text{OUTn}}$				-	700	1000	
	$\overline{\text{ENABLE}} - \overline{\text{OUTn}}$				-	700	1000	
	CLK- SOUT				15	30	70	
Pulse Width	CLK	$t_{\text{w CLK}}$	-		-	20	30	ns
	$\overline{\text{LATCH}}$	$t_{\text{w LAT}}$	-		-	10	25	ns
Set-up Time	L- H	$t_{\text{setup (L)}}$	-	-	25	50	ns	
	H- L	$t_{\text{setup (C)}}$	-	-	25	50	ns	
Hold Time	L- H	$t_{\text{hold (L)}}$	-	-	0	15	ns	
	H- L	$t_{\text{hold (C)}}$	-	-	0	15	ns	
Maximum CLOCK Rise Time		$t_{\text{r}}$	-	-	-	10	$\mu\text{s}$	
Maximum CLOCK Fall Time		$t_{\text{f}}$	-	-	-	10	$\mu\text{s}$	
Output Rise Time		$t_{\text{or}}$	-	-	150	300	600	ns
Output Fall Time		$t_{\text{of}}$	-	-	150	300	600	ns

**TEST CIRCUIT**

**DC characteristic**



**AC characteristic**

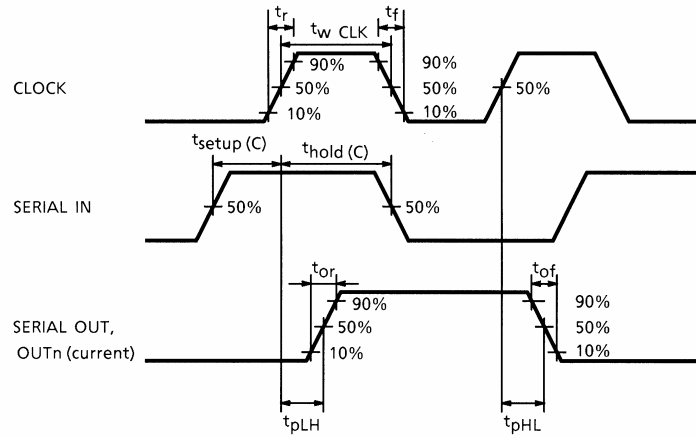


**PRECAUTIONS for USING**

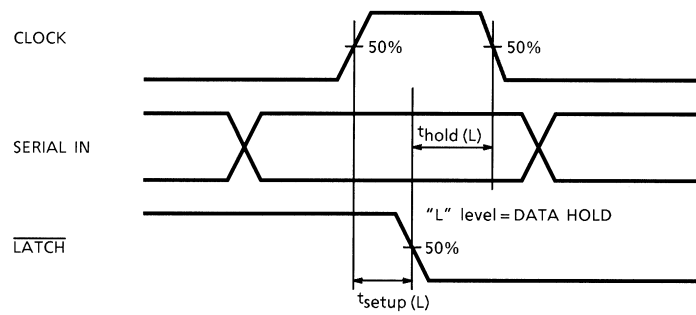
Utmost care is necessary in the design of the output line,  $V_{CC}$  ( $V_{DD}$ ) and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

**TIMING WAVEFORM**

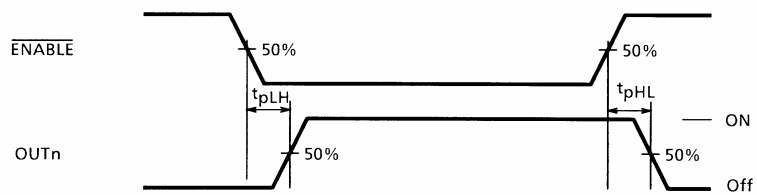
**1. CLOCK- SERIAL OUT, OUTn**



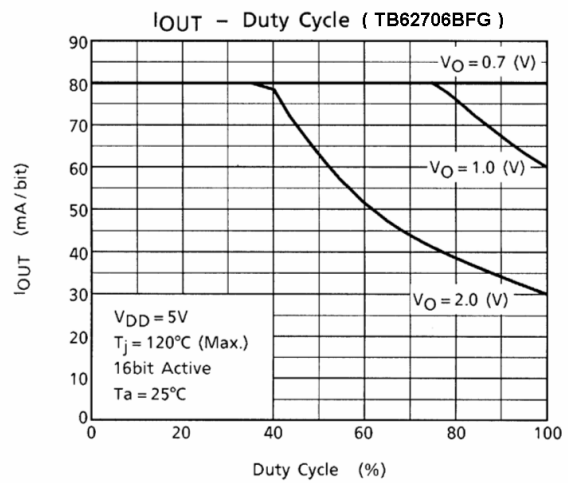
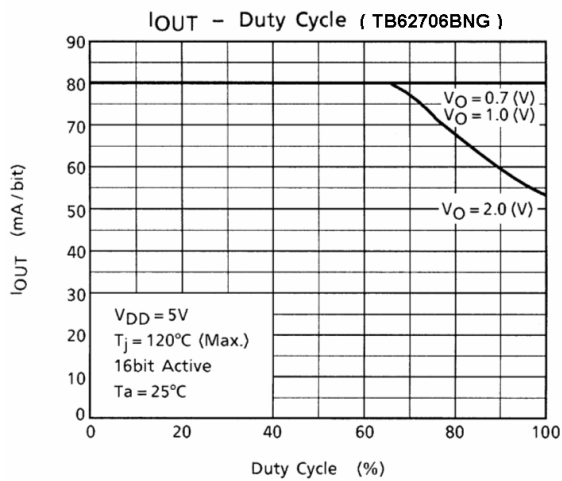
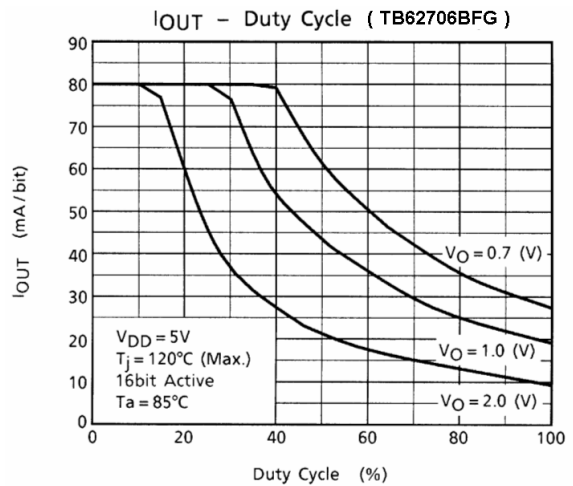
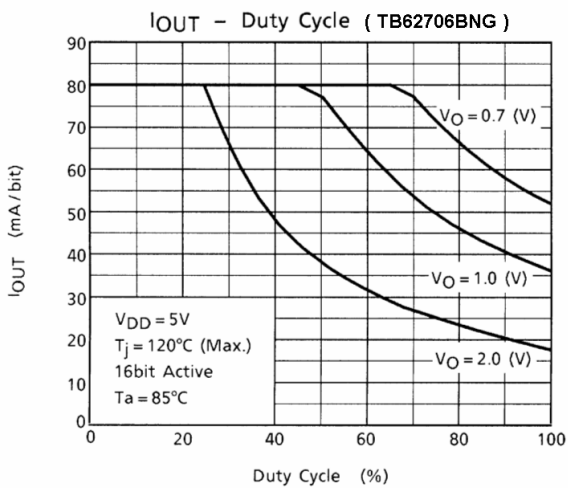
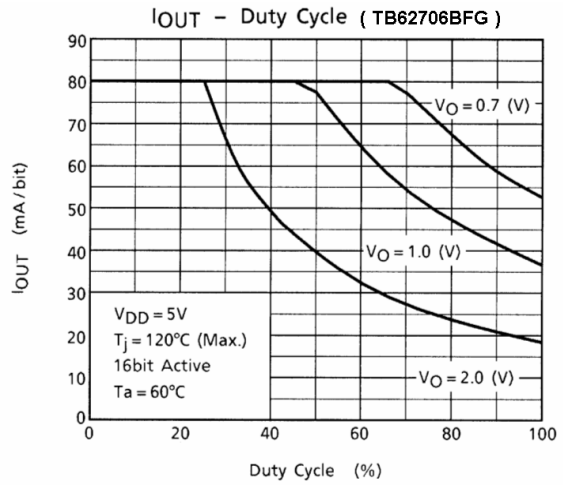
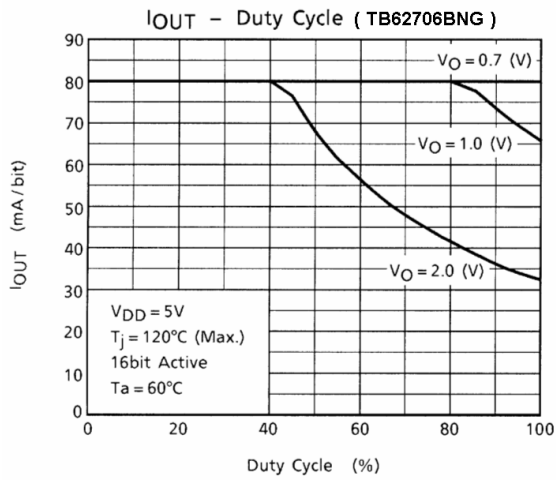
**2. CLOCK- LATCH**



**3. ENABLE - OUTn**







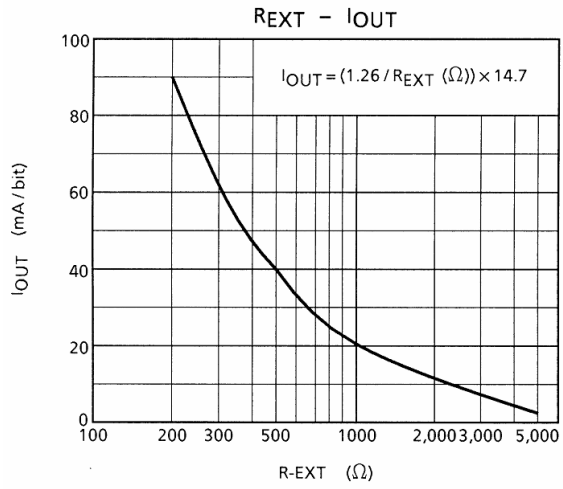
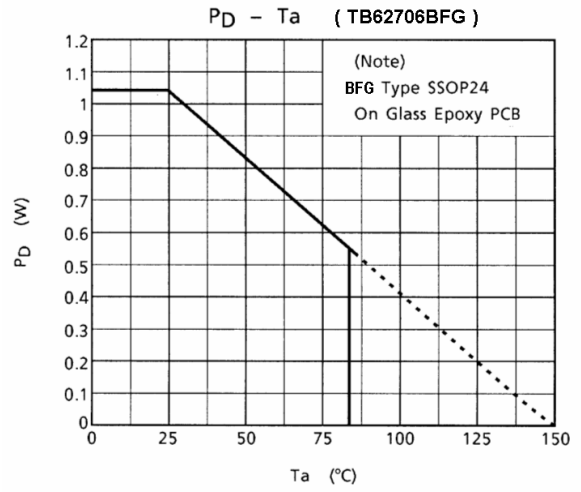
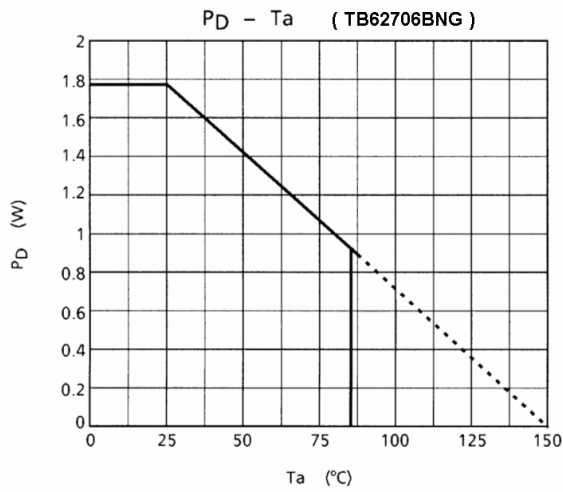


Fig.1



## LED DRIVER TB6270X SERIES APPLICATION NOTE

[1] Output current ( $I_{OUT}$ )

$I_{OUT}$  is set by the external resistor (R-EXT) as shown in Fig.1.

[2] Total supply voltage (VLED)

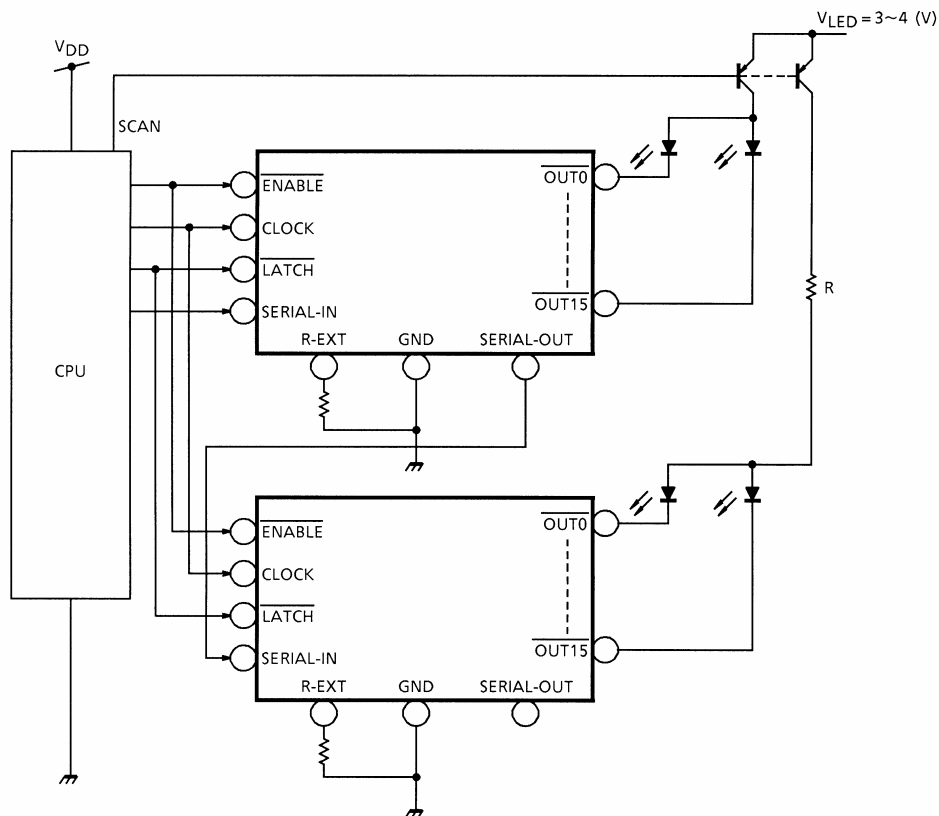
This device can operate 0.4~0.7V ( $V_O$ ).

When a higher voltage is input to the device, the excess voltage is consumed inside the device, that leads to power dissipation.

In order to minimize power dissipation and loss, we would like to recommend to set the total supply voltage as shown below,

$$V_{LED} \text{ (total supply voltage)} = V_{CE} (T_r V_{sat}) + V_f \text{ (LED Forward voltage)} + V_O \text{ (Ic supply voltage)}$$

When the total supply is too high considering the power dissipation of this device, an additional R can decrease the supply voltage ( $V_O$ ).



[3] Pattern layout

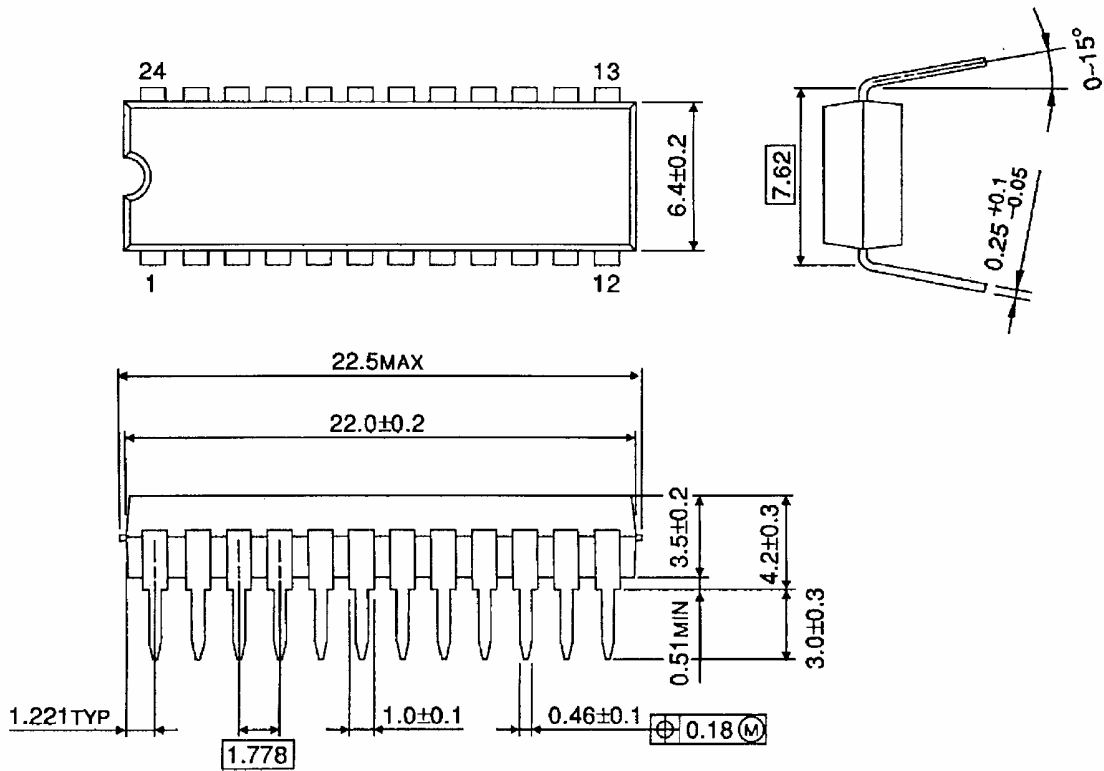
This device owns only one ground pin that means signal ground pin and power ground pin are common.

If ground pattern layout contains large inductance and impedance, and the voltage between ground and LATCH, CLOCK terminals exceeds 2.5 V by switching noise in operation, this device may miss-operate. So we would like you to pay attention to pattern layout to minimize inductance.

## Package Dimensions

SDIP24-P-300-1.78

Unit : mm

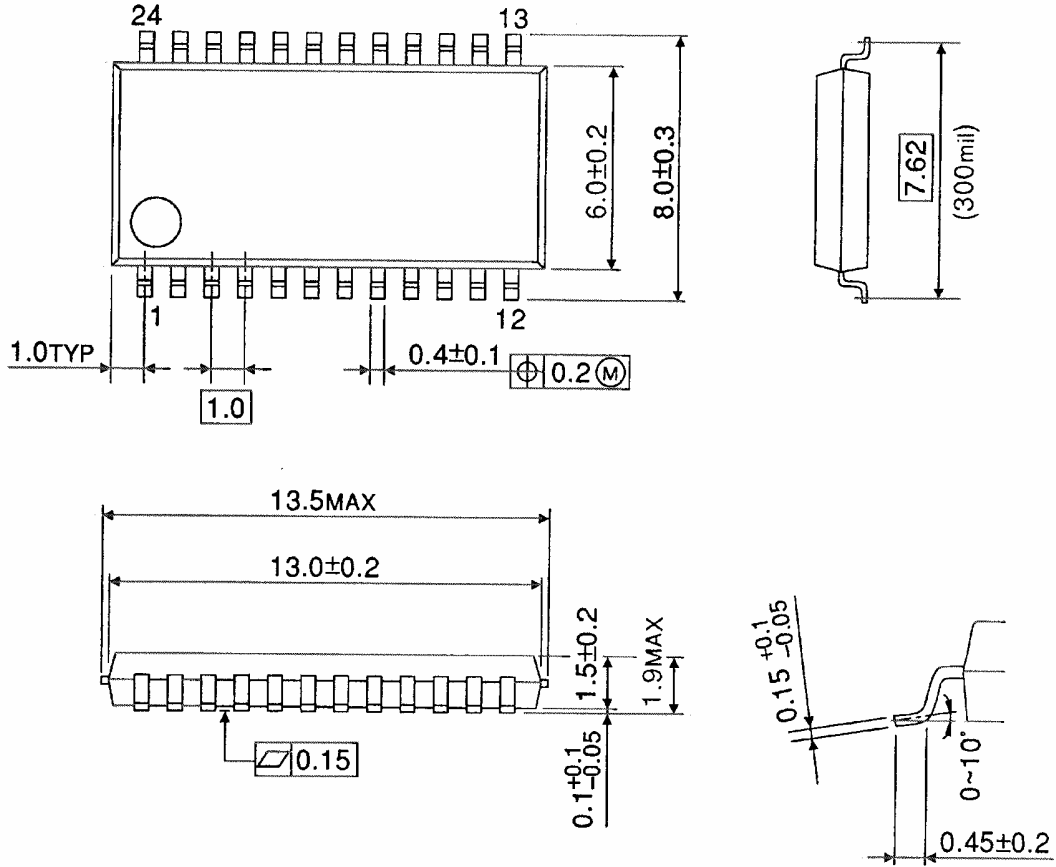


Weight: 1.22 g (typ.)

**Package Dimensions**

SSOP24-P-300-1.00B

Unit : mm



Weight: 0.32 g (typ.)

About solderability, following conditions were confirmed

- Solderability
  - (1) Use of Sn-63Pb solder Bath
    - solder bath temperature = 230°C
    - dipping time = 5 seconds
    - the number of times = once
    - use of R-type flux
  - (2) Use of Sn-3.0Ag-0.5Cu solder Bath
    - solder bath temperature = 245°C
    - dipping time = 5 seconds
    - the number of times = once
    - use of R-type flux

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000707EBA

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