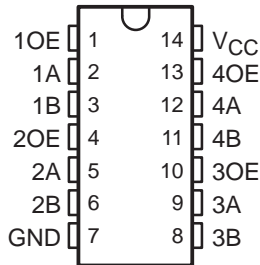


SN74CBTLV3126 LOW-VOLTAGE QUADRUPLE FET BUS SWITCH

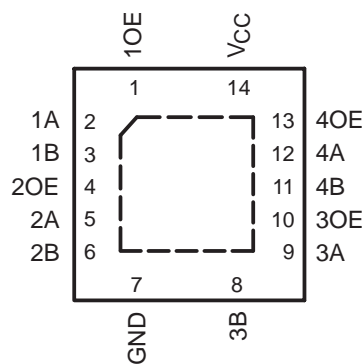
SCDS038I – DECEMBER 1997 – REVISED OCTOBER 2003

- Standard '126-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- Rail-to-Rail Switching on Data I/O Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-up Performance Exceeds 100 mA per JESD 78, Class II

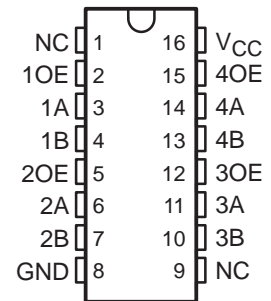
**D, DGV, OR PW PACKAGE
(TOP VIEW)**



**RGY PACKAGE
(TOP VIEW)**



**DBQ PACKAGE
(TOP VIEW)**



NC – No internal connection

description/ordering information

The SN74CBTLV3126 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (OE) input is low.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74CBTLV3126RGYR	CL126
	SOIC – D	Tube	SN74CBTLV3126D	CBTLV3126
		Tape and reel	SN74CBTLV3126DR	
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBTLV3126DBQR	CL126
	TSSOP – PW	Tape and reel	SN74CBTLV3126PWR	CL126
	TVSOP – DGV	Tape and reel	SN74CBTLV3126DGV	CL126

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE
(each bus switch)**

INPUT OE	FUNCTION
L	Disconnect
H	A port = B port



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

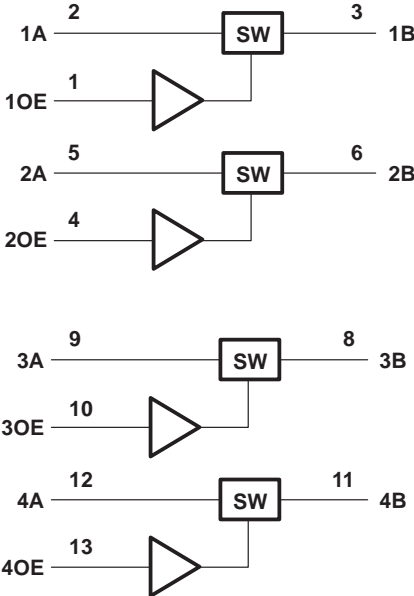
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated

SN74CBTLV3126 LOW-VOLTAGE QUADRUPLE FET BUS SWITCH

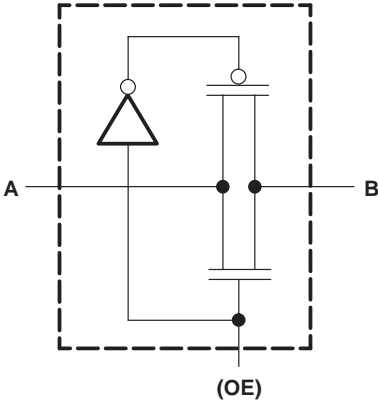
SCDS038I – DECEMBER 1997 – REVISED OCTOBER 2003

logic diagram (positive logic)



Pin numbers shown are for the D, DGV, PW, and RGY packages.

simplified schematic, each FET switch



SN74CBTLV3126

LOW-VOLTAGE QUADRUPLE FET BUS SWITCH

SCDS038I – DECEMBER 1997 – REVISED OCTOBER 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 4.6 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
(see Note 2): DBQ package	90°C/W
(see Note 2): DGV package	127°C/W
(see Note 2): PW package	113°C/W
(see Note 3): RGY package	47°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.
 3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.3	3.6	V
V_{IH}	High-level control input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2	
V_{IL}	Low-level control input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0.8	
T_A	Operating free-air temperature	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	$V_{CC} = 3\text{ V}$,	$I_I = -18\text{ mA}$			–1.2	V
I_I	$V_{CC} = 3.6\text{ V}$,	$V_I = V_{CC}$ or GND			±1	µA
I_{off}	$V_{CC} = 0$,	V_I or $V_O = 0$ to 3.6 V			10	µA
I_{CC}	$V_{CC} = 3.6\text{ V}$,	$I_O = 0$, $V_I = V_{CC}$ or GND			10	µA
ΔI_{CC} §	Control inputs	$V_{CC} = 3.6\text{ V}$, One input at 3 V, Other inputs at V_{CC} or GND			300	µA
C_i	Control inputs	$V_I = 3\text{ V}$ or 0			2.5	pF
$C_{io(OFF)}$		$V_O = 3\text{ V}$ or 0, OE = GND			7	pF
r_{on} ¶	$V_{CC} = 2.3\text{ V}$, TYP at $V_{CC} = 2.5\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$	5	8	Ω
			$I_I = 24\text{ mA}$	5	8	
		$V_I = 1.7\text{ V}$,	$I_I = 15\text{ mA}$	27	40	
	$V_{CC} = 3\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$	5	7	
			$I_I = 24\text{ mA}$	5	7	
		$V_I = 2.4\text{ V}$,	$I_I = 15\text{ mA}$	10	15	

‡ All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

§ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



SN74CBTLV3126

LOW-VOLTAGE QUADRUPLE FET BUS SWITCH

SCDS038I – DECEMBER 1997 – REVISED OCTOBER 2003

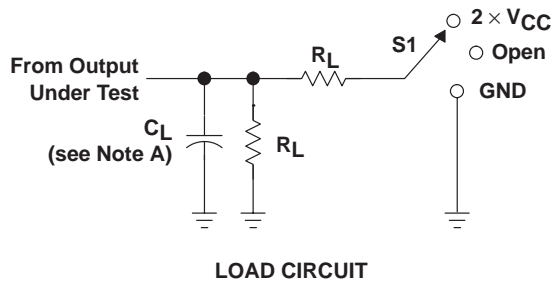
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd} [†]	A or B	B or A	0.15		0.25		ns
t _{en}	OE	A or B	1.6	4.5	1.9	4.2	ns
t _{dis}	OE	A or B	1.3	4.7	1	4.8	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

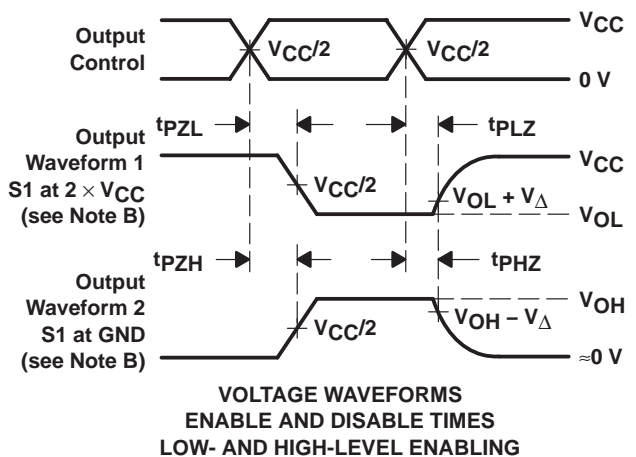
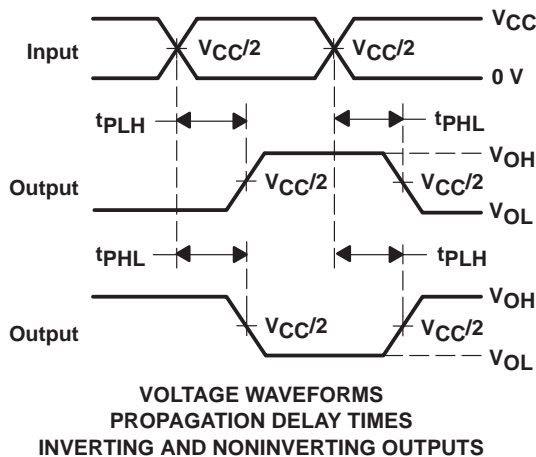
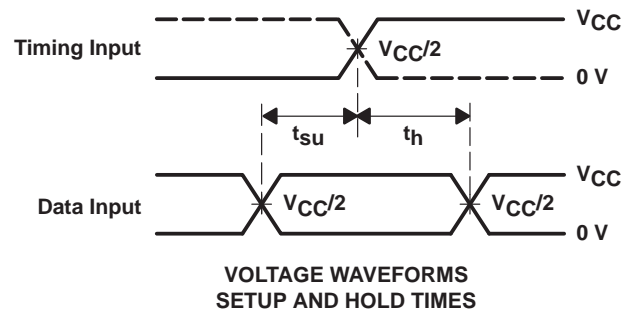
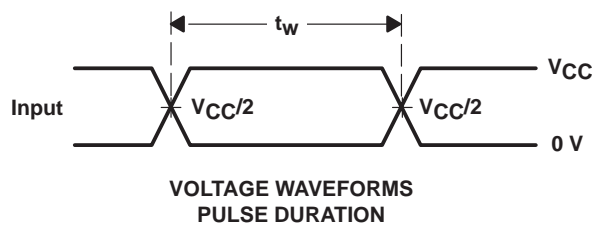


PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_{Δ}
$2.5\text{ V} \pm 0.2\text{ V}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	50 pF	500 Ω	0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

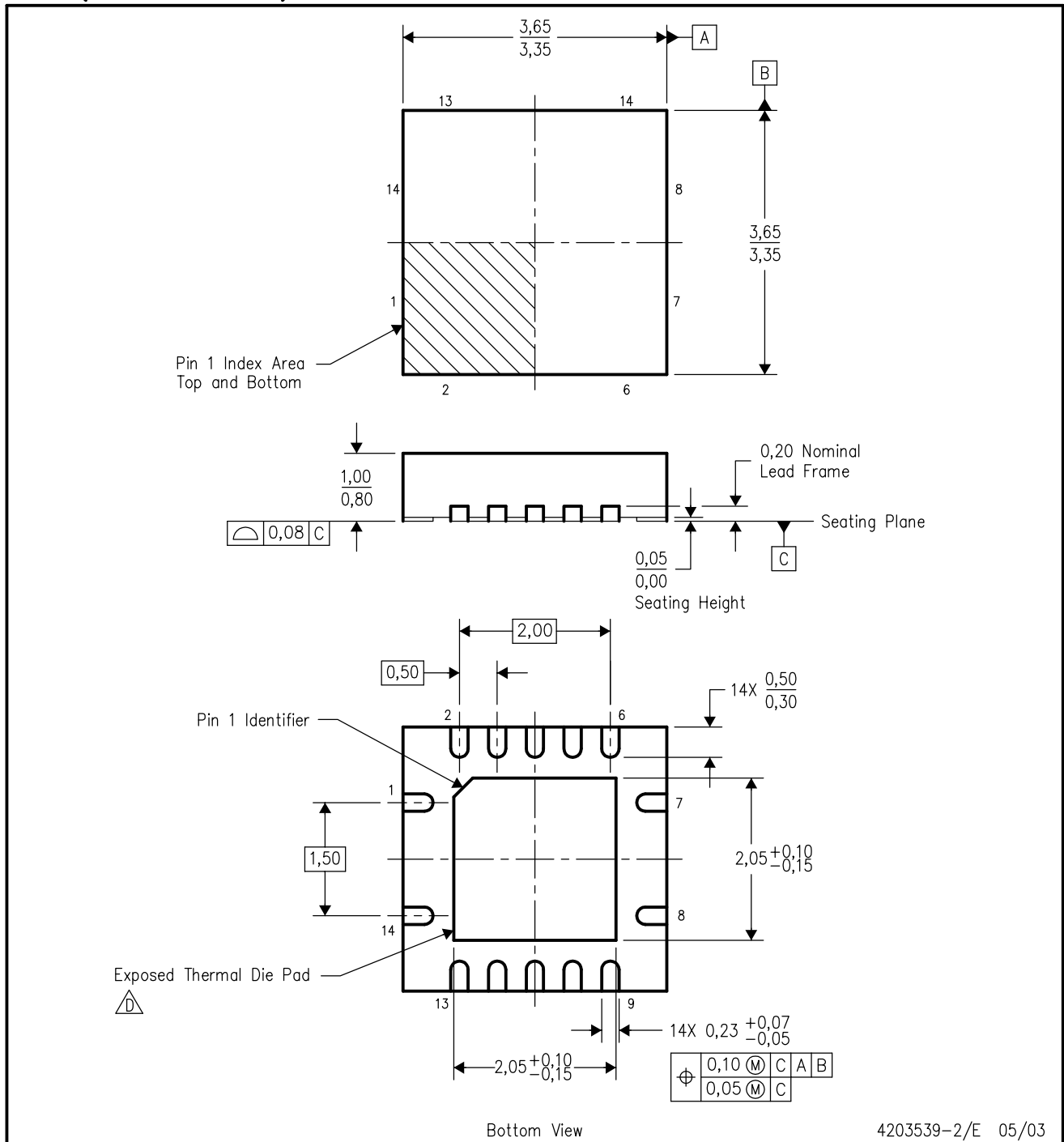
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



Bottom View

4203539-2/E 05/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - \triangle The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
 - E. Package complies to JEDEC MO-241 variation BA.

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

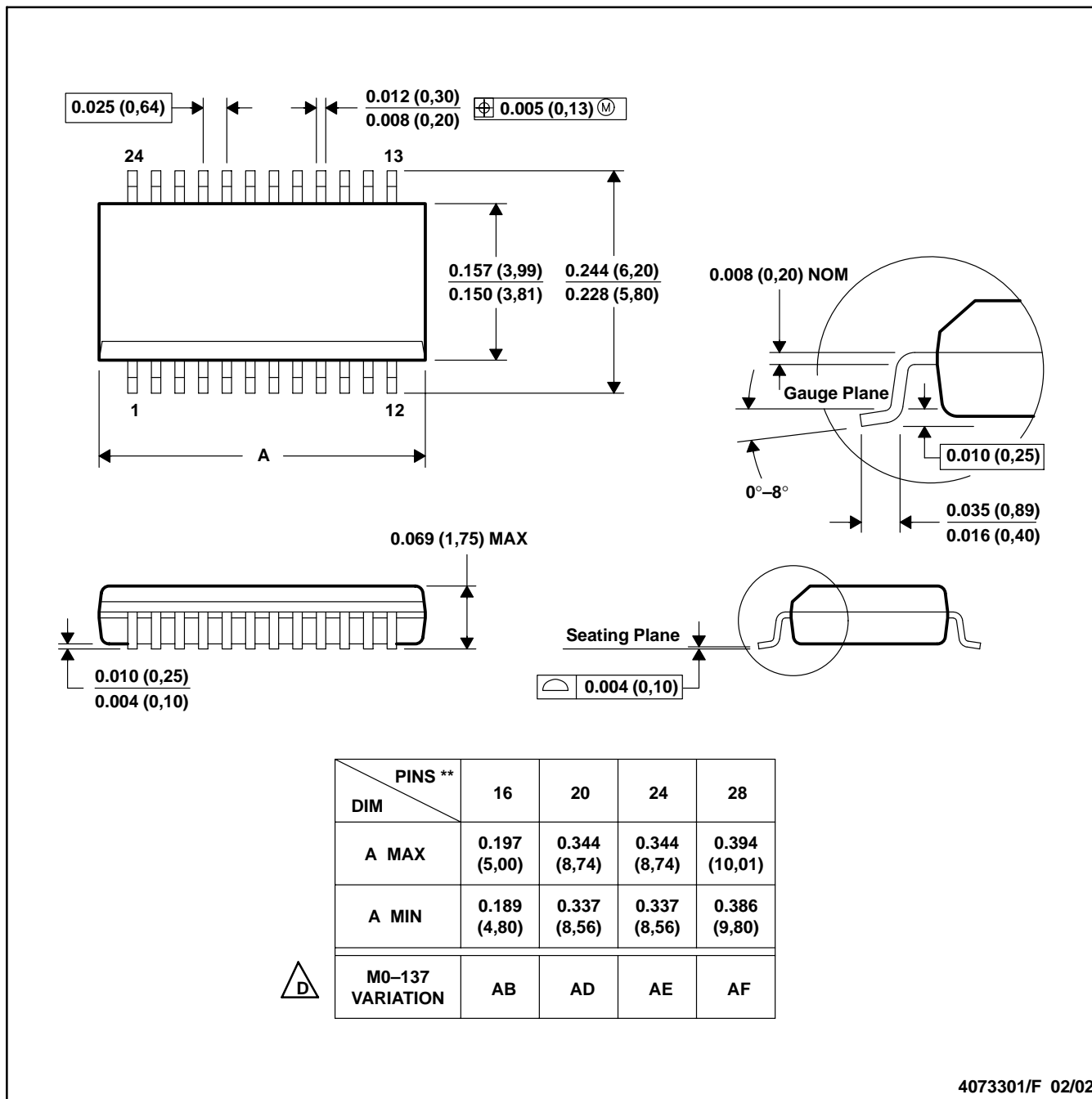
8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

DBQ (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE



4073301/F 02/02

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-137.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2003, Texas Instruments Incorporated