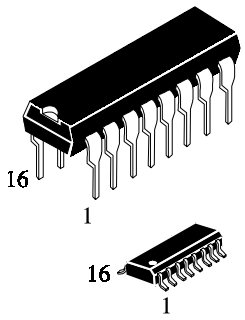
**IN74AC175**

# Quad D Flip-Flop with Common Clock and Reset

## High-Speed Silicon-Gate CMOS



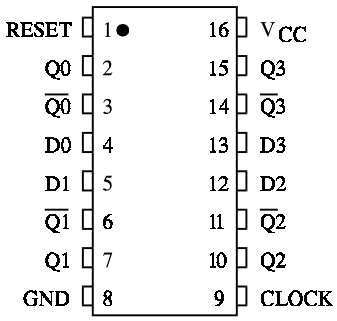

**ORDERING INFORMATION**
IN74AC175N Plastic
IN74AC175D SOIC
$T_A$ = -40° to 85° C for all packages

The IN74AC175 is identical in pinout to the LS/ALS175, HC/HCT175. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALS outputs.

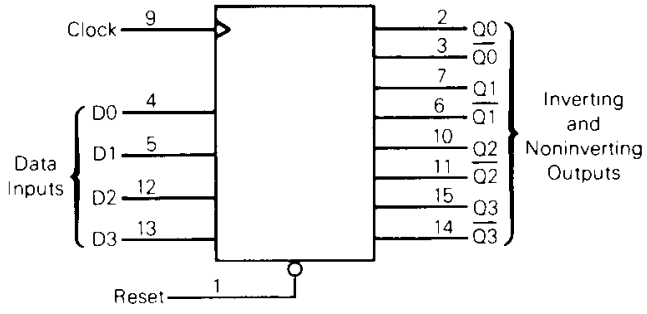
This device consists of four D flip-flops with common Reset and Clock inputs, and separate D inputs. Reset (active-low) is asynchronous and occurs when a low level is applied to the Reset input. Information at a D input is transferred to the corresponding Q output on the next positive-going edge of the Clock input.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA; 0.1 μA @ 25°C
- High Noise Immunity Characteristic of CMOS Devices
- Outputs Source/Sink 24 mA

### PIN ASSIGNMENT




### LOGIC DIAGRAM




PIN 16=$V_{CC}$
PIN 8 = GND

### FUNCTION TABLE

| Inputs | | | Outputs | |
|---|---|---|---|---|
| Reset | Clock | D | Q | $\overline{Q}$ |
| L | X | X | L | H |
| H | ↗ | H | H | L |
| H | ↗ | L | L | H |
| H | L | X | no change | |

X = Don't care



INTEGRAL

## MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| $V_{IN}$ | DC Input Voltage (Referenced to GND) | -0.5 to $V_{CC}$ +0.5 | V |
| $V_{OUT}$ | DC Output Voltage (Referenced to GND) | -0.5 to $V_{CC}$ +0.5 | V |
| $I_{IN}$ | DC Input Current, per Pin | ±20 | mA |
| $I_{OUT}$ | DC Output Sink/Source Current, per Pin | ±50 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ±50 | mA |
| $P_D$ | Power Dissipation in Still Air, Plastic DIP+<br>SOIC Package+ | 750<br>500 | mW |
| Tstg | Storage Temperature | -65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP or SOIC Package) | 260 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | | 2.0 | 6.0 | V |
| $V_{IN}$, $V_{OUT}$ | DC Input Voltage, Output Voltage (Referenced to GND) | | 0 | $V_{CC}$ | V |
| $T_J$ | Junction Temperature (PDIP) | | | 140 | °C |
| $T_A$ | Operating Temperature, All Package Types | | -40 | +85 | °C |
| $I_{OH}$ | Output Current - High | | | -24 | mA |
| $I_{OL}$ | Output Current - Low | | | 24 | mA |
| $t_r$, $t_f$ | Input Rise and Fall Time * | $V_{CC}$ =3.0 V | 0 | 150 | ns/V |
| | (except Schmitt Inputs) | $V_{CC}$ =4.5 V | 0 | 40 | |
| | | $V_{CC}$ =5.5 V | 0 | 25 | |

* $V_{IN}$ from 30% to 70% $V_{CC}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, $V_{IN}$ and $V_{OUT}$ should be constrained to the range GND≤($V_{IN}$ or $V_{OUT}$)≤$V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limits | | Unit |
|---|---|---|---|---|---|---|
| | | | | 25 °C | -40°C to 85°C | |
| $V_{IH}$ | Minimum High-Level Input Voltage | $V_{OUT}$=0.1 V or $V_{CC}$-0.1 V | 3.0<br>4.5<br>5.5 | 2.1<br>3.15<br>3.85 | 2.1<br>3.15<br>3.85 | V |
| $V_{IL}$ | Maximum Low - Level Input Voltage | $V_{OUT}$=0.1 V or $V_{CC}$-0.1 V | 3.0<br>4.5<br>5.5 | 0.9<br>1.35<br>1.65 | 0.9<br>1.35<br>1.65 | V |
| $V_{OH}$ | Minimum High-Level Output Voltage | $I_{OUT} \leq$ -50 μA | 3.0<br>4.5<br>5.5 | 2.9<br>4.4<br>5.4 | 2.9<br>4.4<br>5.4 | V |
| | | *$V_{IN}$=$V_{IH}$ or $V_{IL}$<br>$I_{OH}$=-12 mA<br>$I_{OH}$=-24 mA<br>$I_{OH}$=-24 mA | <br>3.0<br>4.5<br>5.5 | <br>2.56<br>3.86<br>4.86 | <br>2.46<br>3.76<br>4.76 | |
| $V_{OL}$ | Maximum Low-Level Output Voltage | $I_{OUT} \leq$ 50 μA | 3.0<br>4.5<br>5.5 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | V |
| | | *$V_{IN}$=$V_{IH}$ or $V_{IL}$<br>$I_{OL}$=12 mA<br>$I_{OL}$=24 mA<br>$I_{OL}$=24 mA | <br>3.0<br>4.5<br>5.5 | <br>0.36<br>0.36<br>0.36 | <br>0.44<br>0.44<br>0.44 | |
| $I_{IN}$ | Maximum Input Leakage Current | $V_{IN}$=$V_{CC}$ or GND | 5.5 | ±0.1 | ±1.0 | μA |
| $I_{OLD}$ | +Minimum Dynamic Output Current | $V_{OLD}$=1.65 V Max | 5.5 | | 75 | mA |
| $I_{OHD}$ | +Minimum Dynamic Output Current | $V_{OHD}$=3.85 V Min | 5.5 | | -75 | mA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{IN}$=$V_{CC}$ or GND | 5.5 | 8.0 | 80 | μA |

* All outputs loaded; thresholds on input associated with output under test.
+Maximum test duration 2.0 ms, one output loaded at a time.
Note: $I_{IN}$ and $I_{CC}$ @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V $V_{CC}$

## AC ELECTRICAL CHARACTERISTICS($C_L$=50pF,Input $t_r$=$t_f$=3.0 ns)

| Symbol | Parameter | $V_{CC}$* V | Guaranteed Limits | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | 25 °C | | -40°C to 85°C | | |
| | | | Min | Max | Min | Max | |
| $f_{max}$ | Maximum Clock Frequency (Figure 1) | 3.3<br>5.0 | 149<br>187 | | 139<br>187 | | MHz |
| $t_{PLH}$ | Propagation Delay, Clock to Q or $\overline{Q}$ (Figure 1) | 3.3<br>5.0 | 2.0<br>1.5 | 12.0<br>9.0 | 2.0<br>1.0 | 13.5<br>9.5 | ns |
| $t_{PHL}$ | Propagation Delay, Clock to Q or $\overline{Q}$ (Figure 1) | 3.3<br>5.0 | 2.5<br>1.5 | 13.0<br>9.5 | 2.0<br>1.5 | 14.5<br>10.5 | ns |
| $t_{PLH}$ | Propagation Delay, Reset to $\overline{Q}$ (Figure 2) | 3.3<br>5.0 | 3.0<br>2.0 | 12.5<br>9.0 | 2.5<br>1.5 | 13.5<br>10.0 | ns |
| $t_{PHL}$ | Propagation Delay, Reset to Q (Figure 2) | 3.3<br>5.0 | 3.0<br>2.0 | 11.0<br>8.5 | 2.5<br>1.5 | 12.5<br>9.0 | ns |
| $C_{IN}$ | Maximum Input Capacitance | 5.0 | 4.5 | | 4.5 | | pF |

| | | Typical @25°C,$V_{CC}$=5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance | 45 | pF |

*Voltage Range 3.3 V is 3.3 V ±0.3 V
Voltage Range 5.0 V is 5.0 V ±0.5 V

## TIMING REQUIREMENTS($C_L$=50pF,Input $t_r$=$t_f$=3.0 ns)

| Symbol | Parameter | $V_{CC}$* V | Guaranteed Limits | | Unit |
|---|---|---|---|---|---|
| | | | 25 °C | -40°C to 85°C | |
| $t_{su}$ | Minimum Setup Time, Data to Clock (Figure 3) | 3.3<br>5.0 | 4.5<br>3.0 | 4.5<br>3.0 | ns |
| $t_h$ | Minimum Hold Time, Clock to Data (Figure 3) | 3.3<br>5.0 | 1.0<br>1.0 | 1.0<br>1.0 | ns |
| $t_w$ | Minimum Pulse Width, Reset (Figure 2) | 3.3<br>5.0 | 4.5<br>3.5 | 4.5<br>3.5 | ns |
| $t_w$ | Minimum Pulse Width, Clock (Figure 1) | 3.3<br>5.0 | 4.5<br>3.5 | 5.0<br>3.5 | ns |
| $t_{rec}$ | Minimum Recovery Time, Reset to Clock (Figure 2) | 3.3<br>5.0 | 0<br>0 | 0<br>0 | ns |

*Voltage Range 3.3 V is 3.3 V ±0.3 V
Voltage Range 5.0 V is 5.0 V ±0.5 V

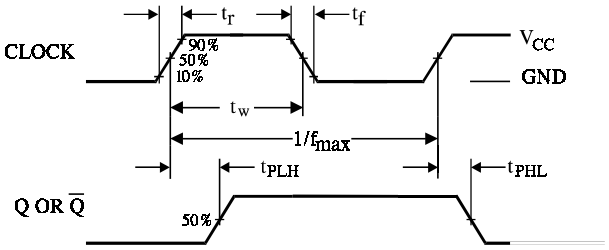



**Figure 1. Switching Waveforms**

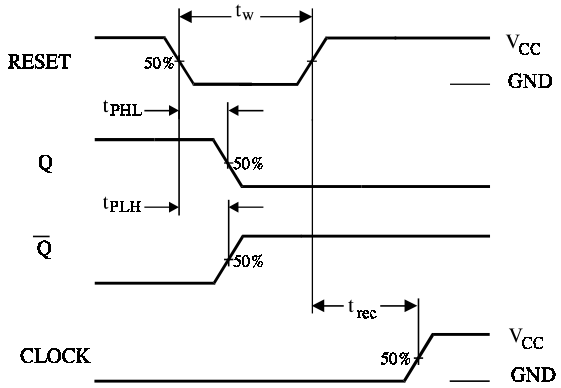



**Figure 2. Switching Waveforms**

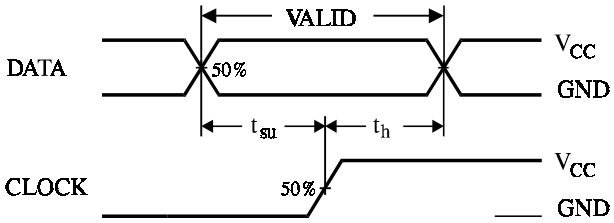



**Figure 3. Switching Waveforms**

## EXPANDED LOGIC DIAGRAM